ThinkPad 760XD/760XL/765D/765L Technical Reference

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Note

Before using this information and the product it supports, be sure to read the general information under Appendix C, “Notices” on page C-1.

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Contents

Figures

Preface

This technical reference contains hardware and software interface information specific to the IBM ThinkPad 760XD, 760XL, 765D, and 765L computers. This technical reference is intended for those who develop hardware and software products for the computer. Users should understand computer architecture and programming concepts.

This publication consists of the following sections and appendixes:

Section 1, “System Overview,” describes the system, features, and specifications.

Section 2, “Programmable Option Select (POS),” describes the registers used for configuration.

Section 3, “System Board,” describes the system-specific hardware implementations.

Section 4, “Subsystems,” describes the hardware functions specific to the ThinkPad 760XD, 760XL, 765D, and 765L computers.

Appendix A, “System Resources,” describes the available system resources for the computer and docking stations.

Appendix B, “System Management API (SMAPI) BIOS Overview,” describes the system software interface built into the system, called the System Management Application Program Interface (SMAPI) BIOS, which controls the system information, system configuration, and power management features of the ThinkPad computer.

Appendix C, “Notices,” contains special notices and trademark information.

An index is also included.

This technical reference should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference

IBM Personal System/2 and Personal Computer BIOS Interface

These publications contain additional information on many of the subjects discussed in this technical reference. Information about

diskette drives, hard disk drives, adapters, and external options are in separate technical references.

Attention
The term *Reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. Read the register first and change only the bits that must be changed.

Section 1. System Overview

Description

The *IBM Personal System/2 Hardware Interface Technical Reference* describes devices common to the PS/2 AT-bus system family.

The IBM ThinkPad 760XD, 760XL, 765D, or 765L computers (hereafter called the *ThinkPad computer* or the *computer*) are notebook-size computers that feature the AT bus architecture. Each computer supports one internal diskette drive and one internal hard disk drive. The 760XD or 765D also supports an internal CD-ROM drive.

Programs can distinguish the foregoing models of computers from other ThinkPad models by reading the system ID:

- Interrupt 15H
- Function code (AH)=23H and (AL)=10H.
- Returns
  (AL)=18H (for the model with 800x600 LCD containing the video chip Trident 9385)
  (AL)=21H (for the model with 1024x768 LCD containing the video chip Trident 9385)

The system microprocessor contains an internal cache and cache controller.

Figure 1-1 lists the model bytes, submodel bytes, and system clock speed of the system board for each model.

Model	Model Byte (Hex)	Submodel Byte (Hex)	System Clock
760XD or 760XL	FC	01	33 MHz
765D or 765L	FC	01	33 MHz

Figure 1-1. Model and Submodel Bytes

For a listing of the other systems, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface*.

System Board Devices and Features

Figure 1-2 lists the system board devices and their features. The *IBM Personal System/2 Hardware Interface Technical Reference* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	–	Intel** Pentium** processor with the MMX technology • 166MHz • 32KB on-chip cache
External cache	–	256KB (write back) (for not all models)
System timers	1	Channel 0: system timer Channel 1: refresh generation Channel 2: tone generator for speaker
ROM subsystem	–	128KB by 4 banks (1KB equals 1024 bytes)
RAM subsystem	–	8 to 104MB (1MB equals 1,048,576 bytes)
CMOS RAM subsystem	–	128 bytes CMOS RAM with real-time clock/calendar + 4K byte NVRAM
EEPROM subsystem	–	1K bits
Video subsystem	–	SVGA or XGA video functions: • **ThinkPad 760XL** – Up to 262,144 colors on the TFT SVGA (800x600) LCD • **ThinkPad 760XD, 765D, or 765L** – Up to 65,536 colors on the TFT XGA (1024x768) LCD – Up to 16,777,216 colors on an external display See “Video Subsystem” on page 4-2 for more details of the video subsystem.
DMA controller	1	Seven DMA channels (AT compatible) Four 8-bit channels and three 16-bit channels

Figure 1-2 (Part 1 of 2). System Board Devices and Features

Device	Type	Features
Interrupt controller	1	15 levels of system interrupts (interrupts are edge-triggered)
Keyboard/auxiliary device controller	1	Internal keyboard TrackPoint III Auxiliary device connector Password security
Diskette drive controller	2	Supports: • 3.5-in. diskette (2.88MB[1]) • 3.5-in. diskette (1.44MB) • 3.5-in. diskette (1.2MB) • 3.5-in. diskette (720KB)
Serial controller port	2	EIA-232-E interface (16550 compatible) Programmable as serial port 1, 2, 3, or 4 One 9-pin, D-sub connector
Parallel controller port	1	Programmable as parallel port 1, 2, or 3 IEEE P1284-A compatible Supports bidirectional input and output Enhanced Parallel Port (EPP) compatible Extended Capabilities Port (ECP) compatible
Expansion bus adapter (AT-bus and PCI-bus)	–	Supports externally attached devices: • ThinkPad Dock I and Dock II with AT-bus I/O channel (760XD or 760XL only) • SelectaDock • Port replicator
PCMCIA[2] slots**	–	Conforms to the standards and specifications listed in Figure 4-3 on page 4-13. • CardBus • Two Type I or II PC cards • One Type III PC card
DSP subsystem	–	Is driven by: • Mwave DSP; MDSP 2780 • Mwave SRAM 32 Kb by 40 bits • 44 KHz, 16-bit audio CODEC • Voice band CODEC for modem • Internal DAA for some countries • Internal omnidirectional microphone
Infrared subsystem	–	Supports: • ThinkPad IR/SIR/D-ASK (500 KHz) IR

[1] The 2.88MB format size is available as an option.
[2] Personal Computer Memory Card International Association

Figure 1-2 (Part 2 of 2). System Board Devices and Features

System Board I/O Address Map

Figure 1-3 shows the I/O address map.

Address (Hex)	Device
0000–001F	DMA Controller (0–3)
0020, 0021	Interrupt Controller (Master)
0022–002F	Reserved
0030–003F	Audio Subsystem 2 (DCR 3006)
0040–0043	System Timer 1
0048–004B	Reserved
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0074, 0075, 0076	Reserved
0078–007C	EEPROM for Security
0081–0083, 0087	DMA Page Registers (0–3)
0089–008B, 008F	DMA Page Registers (4–7)
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Reserved
0098	System Flash ROM Control Register (DCR 2282)
00A0, 00A1	Interrupt Controller (slave)
00C0–00DF	DMA Controller (4–7)
00F0–00FF	Reserved
0102–0107	Programmable Option Select
0170–0177	Secondary IDE Registers
01A0–01AF	IR Controller 1
01B0–01BF	IR Controller 2
01C0–01CF	IR Controller 3
01D0–01DF	IR Controller 4
01F0–01F7	Primary IDE Registers
0201	Joystick Port
0220–0233	Audio Subsystem - Sound Blaster 1
0240–0253	Audio Subsystem - Sound Blaster 2
026E, 026F	Super I/O Configuration Registers
0278–027A	Parallel Port 3
027B–027F	Reserved
02E8–02EF	Serial Port 4
02F8–02FF	Serial Port 2
0300–0302	MIDI Port 1 EVD model
0330–0332	MIDI Port 2 EVD model
0376, 0377	Secondary IDE Registers
0378–037A	Parallel Port 2
037B–037F	Reserved
0388–038B	Audio Subsystem - FM synthesizer
0398–0399	Reserved

Figure 1-3 (Part 1 of 2). System Board I/O Address Map

Address (Hex)	Device
03B4, 03B5, 03BA	Video Subsystem
03BC–03BE	Parallel Port 1
03C0–03C5	Video Subsystem
03C6–03C9	Video DAC
03CA, 03CC, 03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA, 03D8–03DA	Video Subsystem
03E0–03E1	PCMCIA Interface (DCR 2959)
03E8–03EF	Serial Port 3
03F0–03F5, 03F7	Diskette-Drive Controller
03F6, 03F7	Primary IDE Registers
03F8–03FF	Serial Port 1
0CF8	PCI Configuration Address Register
0CFC	PCI Configuration Data Register
0D00, 0D01	Flat Panel Controller
15E8–15EF	Power Management Register
2120–21FF	Reserved
23C0–23C7	Reserved
43C6–43C9	Video Subsystem
46E8	Video Subsystem Enable
4E30–4E3F	Audio Subsystem 1 (DCR 3006)
83C6–83C8	Video Subsystem
8E30–8E3F	Audio Subsystem 3 (DCR 3006)
CE30–CE3F	Audio Subsystem 4 (DCR 3006)
F104	Reserved

Figure 1-3 (Part 2 of 2). System Board I/O Address Map

Specifications

Figure 1-4 to Figure 1-7 on page 1-9 list the specifications for the computers.

Performance Specifications

Device/Cycle	Clock Counts (66MHz)
Microprocessor	66/166MHz
L1 cache (64bit)	
read/write hit	1 CPUCLK
L2 cache (64bit) (for not all models)	90ns (60ns)
read hit (back-to-back)	90ns (60ns)
write hit (back-to-back)	
Memory (64bit) (*1)	
read, page hit	240ns
read, raw miss	285ns
read, page miss	345ns
posted write	90ns
write retire rate from write buffer	135ns

Note:

***1** The cycle times shown for access to system board RAM are based on 70ns EDO memory.

Figure 1-4. Performance Specifications

Physical Specifications

Size

Width: 297 mm (11.7 in.)
Depth: ThinkPad 760XD and 760XL:
210 mm (8.3 in.)
ThinkPad 765D and 765L:
236 mm (9.3 in.)
Height: ThinkPad 760XD:
50.7 mm (2.00 in.)
ThinkPad 760XL:
54.3 mm (2.14 in.)
ThinkPad 765D and 765L:
56.2 mm (2.2 in.)

Weight[1] (approximate value)

ThinkPad 760XD:
3.18 kg (7.0 lb) (with Li ion battery & CD-ROM)
ThinkPad 760XL:
3.05 kg (6.7 lb) (with Li ion battery & FDD)
ThinkPad 765D:
3.49 kg (7.7 lb) (with Li ion battery & CD-ROM)
ThinkPad 765L:
3.34 kg (7.4 lb) (with Li ion battery & FDD)

Air Temperature

System on (without diskette)
5.0°C to 35.0°C (41°F to 95°F)

System on (with diskette)
10.0°C to 35.0°C (50°F to 95°F)

System off
5.0°C to 43.0°C (41°F to 110°F)

Humidity

System (without diskette)
8% to 95%

System (with diskette)
8% to 80%

Maximum altitude[2]: 3,048 m (10,000 ft) in unpressurized conditions

Heat output: 40 W (136.5 BTUs/hour) at maximum configuration

Acoustical readings (see Figure 1-7 on page 1-9)

Electrical (see Figure 1-6 on page 1-9)

Electromagnetic compatibility: FCC class B

[1] With battery pack installed.
[2] This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.

Figure 1-5. Physical Specifications

Electrical Specifications

	(35 W)	(40 W)	(56 W)
Input voltage[1] (V ac)	100–240	100–240	100–240
Frequency (Hz)	50/60	50/60	50/60
Input[2] (kVA)	0.12	0.12	0.17

[1] Range is automatically selected; sine wave input is required.
[2] At maximum configuration.

Figure 1-6. Electrical Specifications

Acoustical Readings

	L_{WAd} in bels		L_{pAm} in dB		$<L_{pA}>_m$ in dB	
	Operate	**Idle**	**Operate**	**Idle**	**Operate**	**Idle**
760XL or 765L	4.0	3.4	34	30	27	22
760XD or 765D (with SelectaDock I)	4.4	4.4	35.5	35.5	29.5	29

Notes:

L_{WAd}	Is the declared sound power level for the random sample of machines.
L_{pAm}	Is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.
$<L_{pA}>_m$	Is the mean value of the A-weighted sound pressure levels at the one-meter position for the random sample of machines.
Operate	Shows the value while using the hard disk drive.

All measurements made in accordance with ANSI S12.10 and reported in conformance with ISO 9296.

Figure 1-7. Acoustical Readings

Power Supply

The power supply converts the ac voltage to dc voltage and provides power for the following:

- System board set
- Diskette drive
- Hard disk drive
- CD-ROM drive
- Auxiliary devices
- Keyboard
- LCD panel
- PCMCIA cards

Voltages

The power supply generates six different dc voltages: VCCCPU, VCC3A, VCC5M, AVCC, VCCSW, and VCC12M. Figure 1-8 shows the maximum current for each voltage.

Output	Voltage (V dc)	Current (A)
VCCCPU	+2.5	4.2
VCC3A	+3.3	3.80
VCC5M	+5.0	5.80
AVCC	+5.0	0.01
VCCSW	+5.0	0.01
VCC12M	+12.0	0.12

Figure 1-8. Power Supply Maximum Current

Output Protection

A short circuit placed on any dc output (between two outputs or between an output and a dc return) latches all dc outputs into a shutdown state, with no hazardous condition to the power supply.

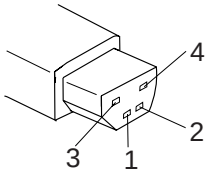
If an overvoltage fault occurs in the power supply, the power supply latches all dc outputs into a shutdown state before any output exceeds 135% of the nominal value of the power supply.

Voltage Sequencing

When power is turned on, the output voltages reach their operational voltages within 2 seconds.

Power Supply Connector

The following connector is used with the AC adapters and the Car Battery Adapter. The total power capacity of this connector must not exceed 4.0 A.



Refer to Figure 1-9 and Figure 1-10 on page 1-12 for the appropriate adapter pin assignments.

Pin	Voltage
1	+8.0 V dc to +20.0 V dc (depending on charging conditions)
2	Charge mode select signal
3	Ground
4	Communication ground

Figure 1-9. Voltage Pin Assignments for the 40W AC Adapter and Car Battery Adapter

Pin	Voltage
1	+7.0 V dc to +16.0 V dc (depending on charging conditions)
2	N/C
3	Ground
4	Ground

Figure 1-10. Voltage Pin Assignments for the 35W or 56W AC Adapter

Battery Pack

The ThinkPad computer uses a lithium-ion (Li-ion) or nickel metal hydride (NiMH) battery pack that meets the following electrical specifications:

Nominal Voltage	+10.8 V dc
Capacity (average)	3.0 ampere hours (AH)
Protection	Overcurrent protection Overvoltage protection Overdischarge protection Thermal protection

Figure 1-11. Li-ion Battery Pack Specifications

Nominal Voltage	+8.4 V dc
Capacity (average)	3.5 ampere hours (AH)
Protection	Overcurrent protection Overvoltage protection Thermal protection

Figure 1-12. NiMH Battery Pack Specifications

Section 2. Programmable Option Select (POS)

Description

Programmable Option Select (POS) uses programmable registers rather than switches. This section describes the POS information used on the system board. For additional POS information, refer to the setup information in *IBM Personal System/2 Hardware Interface Technical Reference*.

Attention

- Set programmable options only through the system configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters may cause multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.
- Application programs should not use the adapter identification unless absolutely necessary; compatibility problems can result.
- After setup operations are complete, the system board enable/setup register (hex 0094) should be set to hex FF.

Setup functions respond to I/O addresses hex 0100 through hex 0107 only when their unique setup signal is active.

System Board POS I/O Address Map

Figure 2-1 shows the organization of the I/O address space used by the system board POS.

Address (Hex)	Function
0094	Enable/Setup register
0096	Reserved
0100	Reserved
0101	Reserved
0102	POS register 2: Option select data byte 1
0103	POS register 3: Option select data byte 2
0104	POS register 4: Option select data byte 3
0105	POS register 5: Option select data byte 4
0106	POS register 6: Option select data byte 5
0107	POS register 7: Option select data byte 6

Figure 2-1. System Board POS I/O Address Map

System Board and Subsystem Setup

The integrated I/O functions on the system board use POS information during setup. The DSP subsystem and IR subsystem are integrated as part of the system board, but POS treats them as separate devices. The system board Enable/Setup register is used to put the DSP subsystem or IR subsystem in setup mode.

System Board Enable/Setup Register (Hex 0094)

The system board Enable/Setup register is a read/write register. All bits in this register default to 1 (enabled).

Bit	Function
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Enable/Setup DSP subsystem
2	Reserved
1	Reserved
0	Enable/Setup IR subsystem

Figure 2-2. System Board Enable/Setup Register (Hex 0094)

Bit 7 Reserved.

Bit 6 Reserved.

Bit 5 Reserved.

Bit 4 Reserved.

Bit 3 When this bit is set to 0, the DSP subsystem function is put in setup mode.

Bit 2 Reserved.

Bit 1 Reserved.

Bit 0 When this bit is set to 0, the IR subsystem function is put in setup mode.

System Board Setup

Take the following precautions before setting individual bits in the POS registers:

- Bit 3 in the DSP subsystem Enable/Setup register (hex 0094) must be put to 0 for the system board function to be set into setup mode.
- Other bits in the DSP subsystem Enable/Setup register must be set to 1 to prevent other subsystems from entering into setup mode.

After setup operations are complete, the following precaution must be taken:

- The system board Enable/Setup register (hex 0094) must be set to hex FF.

Section 3. System Board

Description

This section describes the microprocessor, connectors, memory subsystems, and miscellaneous system functions and ports for the ThinkPad computers. You can find additional information about these topics in *IBM Personal System/2 Hardware Interface Technical Reference–AT-Bus Subsystems*.

Microprocessor

The ThinkPad 760XD, 760XL, 765D, or 765L uses the Intel Pentium 166MHz processor with the MMX technology.

The Pentium has a 32-bit address bus and a 64-bit data bus. It is software-compatible with all previous microprocessors. The Pentium has an internal, split data and instruction, 32KB write-back cache. It includes pipelined math coprocessor functions and superscalar architecture (two execution units).

Cache Memory Operation

In addition to the 32KB of internal Level 1 (L1) cache memory in the microprocessor, the system board of the 760XD, 760XL, 765D, or 765L contains an additional 256KB of external Level 2 (L2) cache memory.

The cache memory in the Intel Pentium microprocessor and the L2 external cache memory enable the microprocessor to read instructions and data much faster than if the microprocessor had to access system memory. When an instruction is first used or data is first read or written, it is transferred to the cache memory from main memory. This enables future accesses to the instructions or data to occur much faster.

The cache is disabled and empty when the microprocessor comes out of the reset state. The cache is tested and enabled during the power-on self-test (POST).

The cache memory in the Intel Pentium microprocessor is loaded from system memory in 32-byte increments, each referred to as a *cache line*. A cache line is aligned on a paragraph boundary. A reference to any byte contained in a cache line results in the entire line being read into the cache memory (if the data was not already in

the cache). When the microprocessor gives up control of the system bus, the cache memory enters “snoop” mode and monitors all write and read operations. If memory data is written to a location in the cache and the cache line is in the “modified” state, the corresponding cache line is written back to system memory and invalidated.

When the microprocessor performs a memory read, the data address is used to find the data in the cache. If the data is found (a hit), it is read from the cache memory and no external bus cycle occurs. If the data is not found (a miss), an external bus cycle is used to read the data from system memory. If the address of the missed data is in cacheable address space, the data is stored in the cache memory and the remainder of the cache line is read.

When the microprocessor performs a memory write, the data address is used to search the cache. If the address is found (hit), the data is written to the cache and no external bus cycle is used to write the data to system memory. (If the address of the write operation was not in the cache memory but was in cacheable address space, the data is read back into the cache memory and the remainder of the cache line is read.)

Cacheable Address Space

Cacheable address space is defined as system memory that resides on the system board (0–640KB and 1MB–104MB). Cacheability of system memory is up to 64MB in the L2 cache. Nothing in address range hex A0000–BFFFF, I/O address space, or memory in any AT slot is cached.

ROM address space (hex C0000–C7FFF) is L1 cacheable for *code read operations only*. If data in this address range is already in cache memory and the address range is written to, the cached line is invalidated and is read again from RAM, where the BIOS is shadowed.

Bus Adapter

When the computer is attached to the ThinkPad Dock I or Dock II, the AT-bus adapters can be used through the Dock I or Dock II. When the computer is attached to the ThinkPad SelectaDock, the PCI adapters or AT-bus adapters can be used through the SelectaDock. ThinkPad 765D and 765L do not support ThinkPad Doc I or Dock II.

Keyboard/Mouse Connector

Each ThinkPad computer has a keyboard/mouse connector, where the IBM mouse, keyboard, or numeric keypad is connected.

Signals

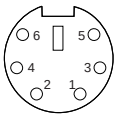
The keyboard and mouse signals are driven by open-collector drivers pulled to 5 V dc through a pull-up resistor. Figure 3-1 lists the signals.

Sink current	1 mA	Maximum
High-level output voltage	5.0 V dc minus pullup	Minimum
Low-level output voltage	0.5 V dc	Maximum
High-level input voltage	2.0 V dc	Minimum
Low-level input voltage	0.8 V dc	Maximum

Figure 3-1. Keyboard and Mouse Signals

Connector

The keyboard/mouse connector uses a 6-pin, miniature DIN connector.



Pin	I/O	Signal Name
1	I/O	Mouse Data
2	I/O	Keyboard Data
3	–	Ground
4	–	+5 V dc
5	I/O	Mouse Clock
6	I/O	Keyboard Clock

Figure 3-2. Keyboard/Mouse Connector Pin Assignments

Note: The maximum current for +5 V dc (pin 4) is 0.5 A for both the mouse and the numeric keypad.

Scan Codes

Figure 3-3 shows the key numbers assigned to keys on the 84-key keyboard (for the U.S. and Japan). Figure 3-4 on page 3-7 shows the key numbers assigned to keys on the 85-key keyboard (for countries other than the U.S. and Japan). For scan codes assigned to each numbered key, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

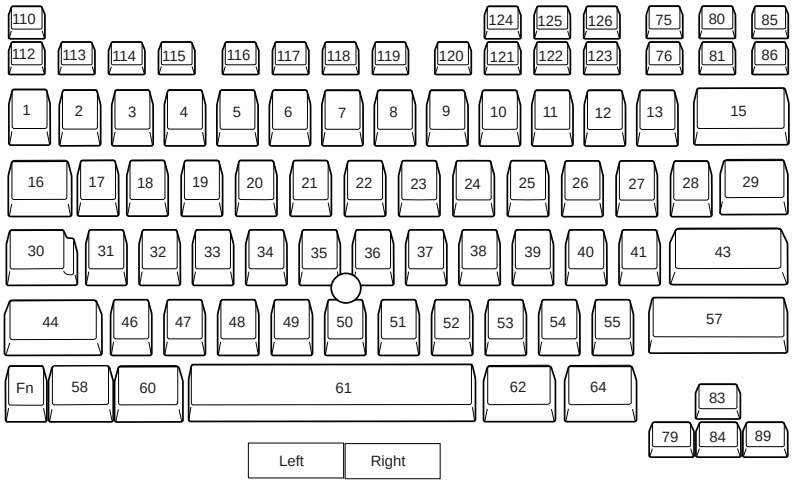


Figure 3-3. Key Numbers for the 84-Key Keyboard

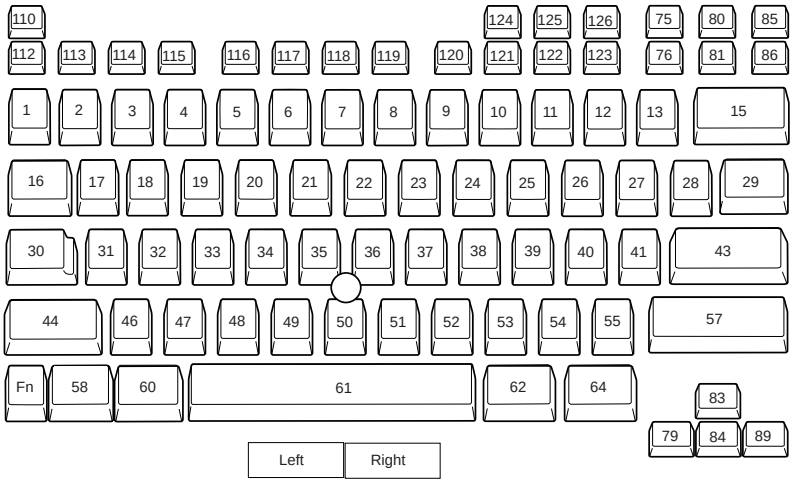


Figure 3-4. Key Numbers for the 85-Key Keyboard

Keyboard ID

The keyboard ID consists of 2 bytes: hex 83AB (the built-in keyboard with the external numeric keypad) or hex 84AB (the built-in keyboard only). Interrupt 16H, function code (AH)=0AH, returns the keyboard ID.

Figure 3-5 shows the key numbers assigned to keys on the external numeric keypad. For scan codes assigned to each numbered key, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

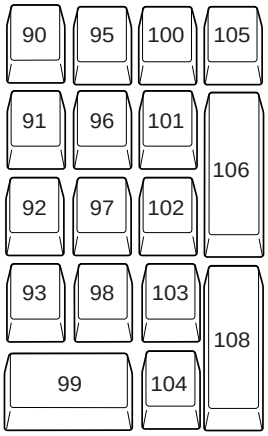


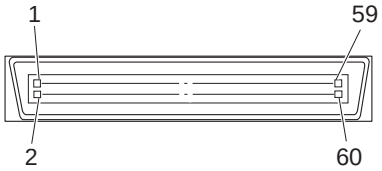
Figure 3-5. Key Numbers for the External Numeric Keypad

Displayable Characters and Symbols

For displayable characters and symbols that are keyable from the keyboard, refer to the *IBM Personal System/2 Hardware Interface Technical Reference*.

Hard Disk Drive Connector

The hard disk drive connected to the system board is removable. Figure 3-6 shows the pin assignments for the connector on the system board.



Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	31	HDID	HDDID
2	GND	Ground	32	–HIOW	I/O write
3	GND	Ground	33	GND	Ground
4	GND	Ground	34	Reserved	Not used
5	GND	Ground	35	(NC)	Not connected
6	GND	Ground	36	GND	Ground
7	GND	Ground	37	HD15	Data 15
8	(NC)	Not connected	38	HD00	Data 0
9	(NC)	Not connected	39	HD14	Data 14
10	(NC)	Not connected	40	HD01	Data 1
11	Reserved	Not used	41	HD13	Data 13
12	GND	Ground	42	HD02	Data 2
13	+5V	+5 V dc	43	HD12	Data 12
14	+5V	+5 V dc	44	HD03	Data 3
15	GND	Ground	45	HD11	Data 11
16	–DASP	Drive (active/slave drive present)	46	HD04	Data 4
17	–HCS1	Chip select 1	47	HD10	Data 10
18	–HCS0	Chip select 0	48	HD05	Data 5
19	HA02	Address 2	49	HD09	Data 9
20	HA00	Address 0	50	HD06	Data 6
21	–PDIAG	Passed diagnostics	51	HD08	Data 8
22	HA01	Address 1	52	HD07	Data 7
23	–HIOCS16	I/O CS16	53	GND	Ground
24	HIRQ	Interrupt request	54	–HRESET	Reset
25	GND	Ground	55	(NC)	Not connected
26	Reserved	Not used	56	(NC)	Not connected
27	Reserved	Not used	57	JP2	Jumper (slave)
28	IORDY	I/O ready	58	JP2	Jumper (slave)
29	GND	Ground	59	JP1	Jumper (master)
30	–HIOR	I/O read	60	JP1	Jumper (master)

Figure 3-6. Hard Disk Drive Connector Pin Assignments

External Bus Connector

The docking station is connected through the 240-pin external bus connector on the rear panel. This connector is installed on the system board and has the following pin assignments:

Type Legend:

A: Audio signal	M: PCMCIA control signal
D: Power control signal	P: Parallel port signal
F: Diskette drive signal	S: Serial port signal
G: Ground	T: AT-bus signal
I: IDE hard disk drive signal	V: Video signal
K: Keyboard/mouse signal	W: Power line
L: LED control signal	X: Analog video interface

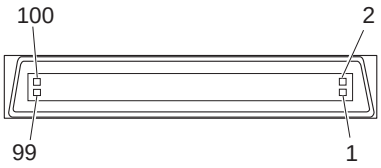
Figure 3-7. 240-Pin External Bus Connector Pin Assignments

	ISA Bus Mode	PCI Bus Mode		ISA Bus Mode	PCI Bus Mode
060	W DOCK_PWR	W <<	061	G GND	G <<
059	W DOCK_PWR	W <<	062	X R RETURN	X <<
058	W DOCK_PWR	W <<	063	X VIDEO R	X <<
057	W DOCK_PWR	W <<	064	X G RETURN	X <<
056	W DOCK_PWR	W <<	065	X VIDEO G	X <<
055	W DOCK_PWR	W <<	066	X B RETURN	X <<
054	W DOCK_PWR	W <<	067	X VIDEO B	X <<
053	W DOCK_PWR	W <<	068	G GND	G <<
052	I PDIAG#	I <<	069	X MONID0	X <<
051	D BATOP_DSBL#	D <<	070	X VSYNC	X <<
050	G GND	G <<	071	X MONID1	X <<
049	T IOCHCK#	P Reserve	072	X HSYNC	X <<
048	T SD6	M MIDIIN	073	X MONID2	X <<
047	T SD4	M MIDIOUT	074	T SD7	P INTD#
046	T SD2	P INTC#	075	T SD5	P INTB#
045	T SD0	P INTA#	076	T SD3	P AD(0)
044	G GND	G <<	077	T SD1	P AD(1)
043	T AEN	P AD(2)	078	G GND	G <<
042	T SA19	P AD(3)	079	T IOCHRDY	P Reserved
041	T SA17	P AD(4)	080	G GND	G <<
040	T SA15	P AD(5)	081	T SA18	P AD(6)
039	T SA14	P AD(7)	082	T SA16	P C/BE0#
038	T SA12	P AD(8)	083	T SA13	P AD(9)
037	T SA10	P AD(10)	084	T SA11	P AD(11)
036	T SA09	P AD(12)	085	T SA08	P AD(13)
035	T SA07	P AD(14)	086	T SA06	P AD(15)
034	T SA05	P PAR	087	T SA03	P C/BE1#
033	T SA04	P PERR#	088	T SA01	P SERR#
032	T SA02	P LOCK#	089	G GND	G <<
031	T SA00	P STOP#	090	T DACK6#	P Reserved
030	G GND	G <<	091	T DRQ6	P Reserved
029	T IRQ9	T <<	092	T RESETDRV	P DEVSEL#
028	T ZEROWS#	P Reserved	093	T DRQ2	P Reserved
027	G GND	G <<	094	T DACK3#	P Reserved
026	T SMEMW#	P TRDY#	095	T DRQ3	P Reserved
025	T SMEMR#	P IRDY#	096	T DACK1#	P Reserved
024	T IOW#	P FRAME#	097	T DRQ1	P Reserved
023	T IOR#	P C/BE2#	098	T DACK7#	P Reserved
022	G GND	G <<	099	T DRQ7	P Reserved
021	T REFRESH#	P AD(16)	100	T MASTER#	P AD(17)
020	T IRQ6	T <<	101	T SYSCLK	P Reserved
019	T IRQ4	T <<	102	T IRQ7	T <<
018	T DACK2#	P Reserved	103	T IRQ5	T <<
017	G GND	G <<	104	T IRQ3	T <<
016	T OSC	P AD(18)	105	T TC	P AD(19)
015	G GND	G <<	106	T BALE	P AD(20)
014	T LA23	P AD(21)	107	G GND	G <<
013	T LA21	P AD(22)	108	T SBHE#	P AD(23)
012	T LA19	P PHLDA_DOCK#	109	T LA22	P C/BE3#
011	T LA17	P ACK_DOCK#	110	T LA20	P PHLD_DOCK#
010	G GND	G <<	111	T LA18	P REQ_DOCK#
009	T MEMW#	P CLK	112	G GND	G <<
008	G GND	G <<	113	T MEMR#	P RST#
007	T SD09	P AD(24)	114	G GND	G <<
006	T SD11	P AD(26)	115	T SD08	P AD(25)
005	T SD13	P AD(28)	116	T SD10	P AD(27)
004	T SD15	P AD(30)	117	T SD12	P AD(29)
003	T IOCS16#	P Reserved	118	T SD14	P AD(31)
002	T DACK0#	P Reserved	119	T MEMCS16#	P Reserved
001	D PWRGOOD	D <<	120	D EVENT#	D <<

	ISA Bus Mode	PCI Bus Mode		ISA Bus Mode	PCI Bus Mode
180	G GND	G <<	181	D DOCK_ID#	D <<
179	D DOCKED_IN1#	G <<	182	G GND	G <<
178	G GNDA	G <<	183	G GNDA	G <<
177	G GNDA	G <<	184	G GNDA	G <<
176	A SYS_LINE_OUT(R)	A <<	185	A SYS_LINE_OUT(L)	A <<
175	G GNDA	G <<	186	G GNDA	G <<
174	X MONID3	X <<	187	S RI#	S <<
173	S RTS#	S <<	188	S CTS#	S <<
172	S DSR#	S <<	189	S DTR#	S <<
171	S DCD#	S <<	190	S RxD	S <<
170	S TxD	S <<	191	P AUTOFD#	P <<
169	D SUS_DSABL#	D <<	192	P ERROR#	P <<
168	P PD0	P <<	193	P INIT#	P <<
167	P PD1	P <<	194	P SLCTIN#	P <<
166	P PD2	P <<	195	P ACK#	P <<
165	P PD3	P <<	196	P BUSY	P <<
164	P PD4	P <<	197	P PE	P <<
163	P PD5	P <<	198	P SLCT	P <<
162	P PD6	P <<	196	P STROBE#	P <<
161	P PD7	P <<	200	D SUS_STAT#	D <<
160	D NOTE_ID0	D <<	201	- Reserved	- <<
159	L HF_LED#	L <<	202	D PWR ON#	D <<
158	- Reserved	L <<	203	F INDEX#	F <<
157	D SWITCH_ON	D <<	204	F DRVSEL0#	F <<
156	G GND	G <<	205	F DISKCHG#	F <<
155	- Reserved	D I2C_DATA	206	F DRIVEID0#	F <<
154	I HDCS0#	I <<	207	F MEDID0	F <<
153	I HDCS1#	I <<	208	F MOTEN0#	F <<
152	I HD7	I <<	209	F MOTEN1#	F <<
151	F FSTEP#	F <<	210	F DRATE1	F <<
150	F WRDATA	F <<	211	F FDIR#	F <<
149	F FWREN#	F <<	212	F DRIVEID1	F <<
148	F TRAK0#	F <<	213	F MEDID1	F <<
147	F DRVSEL1#	F <<	214	F DRATED0	F <<
146	F RDDATA	F <<	215	F FWPROTECT#	F <<
145	- Reserved	- <<	216	F FSIDE1SEL#	F <<
144	- Reserved	- <<	217	G GND	G <<
143	- Reserved	- <<	218	- Reserved	- <<
142	- Reserved	- <<	219	- Reserved	- <<
141	- Reserved	- <<	220	- Reserved	- <<
140	- Reserved	- <<	221	- Reserved	- <<
139	- Reserved	- <<	222	- Reserved	- <<
138	- Reserved	- <<	223	- Reserved	- <<
137	- Reserved	- <<	224	- Reserved	- <<
136	- Reserved	- <<	225	- Reserved	- <<
135	- Reserved	- <<	226	- Reserved	- <<
134	- Reserved	- <<	227	- Reserved	D S_HSYNC
133	- Reserved	- <<	228	- Reserved	D S_VSYNC
132	- Reserved	- <<	229	- Reserved	- <<
131	T IRQ10	T <<	230	- Reserved	D I2C_CLK
130	T IRQ12	T <<	231	- Reserved	- <<
129	T IRQ14	T <<	232	M PCMCIA_RI#	M <<
128	T DRQ5	P Reserved	233	M SPKROUT#	M <<
127	T DRQ0	P Reserved	234	K MOUSECLK	K <<
126	T IRQ11	T <<	235	K MOUSEDATA	K <<
125	T IRQ15	T <<	236	K KBDCLK	K <<
124	T DACK5#	P Reserved	237	K KBDDATA	K <<
123	D DOCK_SU#	D <<	238	K +SAFE5V	K <<
122	D DOCKED_IN2#	D <<	239	P VCC5B_EX	P <<
121	G GND	D <<	240	P VCC5B_EX	P <<

Diskette Drive Connector (UltraBay)

The removable diskette drive, secondary hard disk drive, secondary battery, PCMCIA adapter, or CD-ROM drive can be connected to the UltraBay connector on the system board. Here are the pin assignments:



The UltraBay connector has the following three types of pin assignments. The appropriate interface selection is automatically performed through two ID signals.

Each of the devices in the following figure can be connected to the UltraBay connector:

Device	Type	Bay ID 1	Bay ID 0	Interface
Removable diskette drive	Type A	Ground	Ground	FDD
PCMCIA adapter	Type B	Ground	–	PCMCIA
IDE device (CD-ROM, hard disk)	Type C	–	Ground	IDE

Figure 3-8 on page 3-14 to Figure 3-10 on page 3-18 show the pin assignments for each connector type.

Pin Assignments for Type A

Pin	Signal	Description
1	–	Reserved
2	–	Reserved
3	–	Reserved
4	–	Reserved
5	–	Reserved
6	–	Reserved
7	–	Reserved
8	–	Reserved
9	–	Reserved
10	GND	Ground
11	–	Reserved
12	–	Reserved
13	–	Reserved
14	–	Reserved
15	–	Reserved
16	–	Reserved
17	–	Reserved
18	GND	Ground
19	–	Reserved
20	GND	Ground
21	GND	Bay ID 0 (GND)
22	GND	Ground
23	GND	Bay ID 1 (GND)
24	–	Reserved
25	–	Reserved
26	–	Reserved
27	–	Reserved
28	–	Reserved
29	–	Reserved
30	GND	Ground
31	–	Reserved
32	–	Reserved
33	–	Reserved
34	–	Reserved
35	–	Reserved
36	–	Reserved
37	GND	Ground
38	–	Reserved
39	–	Reserved
40	–	Reserved
41	–	Reserved
42	–	Reserved
43	–	Reserved
44	GND	Ground
45	BATVCC	8–20 V
46	GND	Ground
47	BATVCC	8–20 V
48	GND	Ground
49	BATVCC	8–20 V
50	GND	Ground

Figure 3-8 (Part 1 of 2). Pin Assignments for Diskette Drive Connector—Type A

Pin	Signal	Description
51	BATVCC	8–20 V
52	–	Reserved
53	BATVCC	8–20 V
54	VCC5A	+5 V dc
55	–	Reserved
56	VCC5A	+5 V dc
57	–	Reserved
58	–	Reserved
59	–	Reserved
60	–	Reserved
61	–	Reserved
62	VCC12B	+12 V dc
63	VCC5A	+5 V dc
64	–	Reserved
65	–	Reserved
66	–	Reserved
67	–	Reserved
68	–	Reserved
69	GND	Ground
70	–	Reserved
71	–	Reserved
72	–	Reserved
73	–	Reserved
74	–	Reserved
75	VCC5B	+5 V dc
76	INDEX#	Index
77	VCC5B	+5 V dc
78	DRVSEL0#	Drive select 0
79	VCC5B	+5 V dc
80	DISKCHG#	Disk change
81	DRVID0	Drive ID 0
82	–	Reserved
83	MEDID0	Media ID 0
84	MOTEN0#	Motor enable 0
85	DRATE1	Data rate select 1
86	FDIR#	Direction In
87	DRVID1	Drive ID 1
88	FSTEP#	Step
89	GND	Ground
90	WRDATA	Write data
91	GND	Ground
92	FWREN#	Write enable
93	MEDID1	Media ID 1
94	TRAK0#	Track 0
95	DRATE0	Data rate select 0
96	FWPROTECT#	Write protect
97	GND	Bay ID 0 (GND)
98	RDDATA	Read data
99	GND	Bay ID 1 (GND)
100	FSIDE1SEL#	Side 1 select

Figure 3-8 (Part 2 of 2). Pin Assignments for Diskette Drive Connector—Type A

Pin Assignments for Type B

Pin	Signal	Description
1	–	Reserved
2	–	Reserved
3	–	Reserved
4	–	Reserved
5	A17	Address 17
6	F-VPP5	5V,12V power control
7	F-VPP12	5V,12V power control
8	F-VCC5#	5V power control
9	CD2#	Card detect2
10	GND	Ground
11	D10	Card data bit 10
12	D9	Card data bit 9
13	D8	Card data bit 8
14	IOIS16#	16Bit I/O Detect
15	STSCHG#	Card status change
16	–	Reserved
17	SPKR#	PCMCIA Speaker
18	GND	Ground
19	REG#	Register Access
20	GND	Ground
21	–	Bay ID 0 (N.C)
22	GND	Ground
23	GND	Bay ID 1 (GND)
24	D2	Card data bit 2
25	–	Reserved
26	D1	Card data bit 1
27	WAIT#	Extended cycle reg
28	D0	Card data bit 0
29	RESET	Card reset
30	GND	Ground
31	FDET5V	Detect 5V Card
32	A0	Card address bit 0
33	A25	Card address bit 25
34	A1	Card address bit 1
35	A24	Card address bit 24
36	A2	Card address bit 2
37	GND	Ground
38	A3	Card address bit 3
39	A23	Card address bit 23
40	A4	Card address bit 4
41	A22	Card address bit 22
42	A5	Card address bit 5
43	A21	Card address bit 21
44	GND	Ground
45	BATVCC	8–20 V
46	GND	Ground
47	BATVCC	8–20 V
48	GND	Ground
49	BATVCC	8–20 V
50	GND	Ground

Figure 3-9 (Part 1 of 2). Pin Assignments for Diskette Drive Connector—Type B

Pin	Signal	Description
51	BATVCC	8–20 V
52	A6	Card address bit 6
53	BATVCC	8–20 V
54	VCC5A	+5 V dc
55	A20	Card address bit 20
56	VCC5A	+5 V dc
57	A19	Card address bit 19
58	A7	Card address bit 7
59	A18	Card address bit 18
60	A12	Card address bit 12
61	–	Reserved (SMP_SPK)
62	VCC12B	+12 V dc
63	VCC5A	+5 V dc
64	–	Reserved (BATLOW#)
65	IOWR#	I/O write
66	A16	Card address bit 16
67	IORD#	I/O read
68	IREQ#	Interrupt request
69	GND	Ground
70	WE#	Write enable
71	A15	Card address bit 15
72	A14	Card address bit 14
73	CE2#	Card enable 2
74	A13	Card address bit 13
75	VCC5B	+5 V
76	A8	Card address bit 8
77	VCC5B	+5 V dc
78	A9	Card address bit 9
79	VCC5B	+5 V dc
80	A11	Card address bit 11
81	D15	Card data bit 15
82	OE#	Output enable
83	D14	Card data 14
84	A10	Card address bit 10
85	D13	Card data bit 13
86	CE1#	Chip Enable 1
87	D12	Card data bit 12
88	D7	Card data bit 7
89	GND	Ground
90	–	(WRDATA)
91	GND	Ground
92	D6	Card data bit 6
93	D11	Card data bit 11
94	D5	Card data bit 5
95	CD1#	Card detect 1
96	D4	Card data bit 4
97	–	Bay ID 0 (N.C)
98	–	(RDDATA)
99	GND	Bay ID 1 (GND)
100	D3	Card data bit 3

Figure 3-9 (Part 2 of 2). Pin Assignments for Diskette Drive Connector—Type B

Pin Assignments for Type C

Pin	Signal	Description
1	L_AUX	Left Auxiliary Line Input
2	AGND	Analog ground (CD-ROM)
3	AGND	Analog ground (CD-ROM)
4	R_AUX	Right Auxiliary Line Input
5	–	Reserved
6	–	Reserved
7	–	Reserved
8	–	Reserved
9	RESET#	Drive Reset
10	GND	Ground
11	D7	Data bit 7
12	D8	Data bit 8
13	D6	Data bit 6
14	D9	Data bit 9
15	D5	Data bit 5
16	BAYHDD#	Hard Disk Detection
17	–	Reserved
18	GND	Ground
19	–	Reserved
20	GND	Ground
21	GND	Bay ID 0 (GND)
22	GND	Ground
23	–	Bay ID 1 (N.C)
24	D10	Data bit 10
25	D4	Data bit 4
26	D11	Data bit 11
27	D3	Data bit 3
28	D12	Data bit 12
29	–	Reserved
30	GND	Ground
31	D2	Data bit 2
32	D13	Data bit 13
33	D1	Data bit 1
34	D14	Data bit 14
35	D0	Data bit 0
36	D15	Data bit 15
37	GND	Ground
38	–	Reserved
39	–	Reserved
40	–	Reserved
41	IOW#	I/O write
42	–	Reserved
43	IOR#	I/O read
44	GND	Ground
45	–	Reserved
46	GND	Ground
47	–	Reserved
48	GND	Ground
49	–	Reserved
50	CSEL	Cable Select (=GND)

Figure 3-10 (Part 1 of 2). Pin Assignments for Diskette Drive Connector—Type C

Pin	Signal	Description
51	–	Reserved
52	IOCHRDY	I/O channel ready
53	–	Reserved
54	–	Reserved
55	–	Reserved
56	–	Reserved
57	IRQ	Address bit 19
58	IOCS16	16 bit I/O Detect
59	–	Reserved
60	–	Reserved
61	–	(SMP_SPK)
62	–	Reserved
63	VCC5A	+5 V dc
64	–	(BATLOW)
65	A1	Address bit 1
66	–	Reserved
67	A0	Address bit 0
68	A2	Address bit 2
69	GND	Ground
70	–	Reserved
71	HDCS0#	Chip select 0
72	HDCS1#	Chip select 1
73	DASP#	Drive active or slave present
74	–	Reserved
75	VCC5B	+5 V dc
76	–	Reserved
77	VCC5B	+5 V dc
78	–	Reserved
79	VCC5B	+5 V dc
80	MCS#	Power management signal (CD-ROM)
81	SLEEP-IN#	Drive sleep in (CD-ROM)
82	–	Reserved
83	–	Reserved
84	–	Reserved
85	–	Reserved
86	–	Reserved
87	–	Reserved
88	–	Reserved
89	GND	Ground
90	–	(WRDATA)
91	GND	Ground
92	–	Reserved
93	–	Reserved
94	–	Reserved
95	–	Reserved
96	–	Reserved
97	BAYID0	Bay ID 0 (=GND)
98	–	Reserved (RDDATA)
99	BAYID1	Bay ID 1 (=N.C)
100	–	Reserved

Figure 3-10 (Part 2 of 2). Pin Assignments for Diskette Drive Connector—Type C

Diskette Drive and Controller

Figure 3-11 shows the read, write, and format capabilities of the diskette drive for the ThinkPad computer.

Diskette Type	Format Size			
	720KB	**1.2MB**	**1.44MB**	**2.88MB**
3.5-inch 1.0MB Diskette	RWF	–	–	–
3.5-inch 2.0MB Diskette	–	RWF	RWF	–
3.5-inch 4.0MB Diskette	–	–	–	RWF

Legend:

1KB (kilobyte)	1024 bytes
1MB (megabyte)	1,048,576 bytes
R	Read
W	Write
F	Format

Figure 3-11. Diskette Drive Read, Write, and Format Capabilities

Memory

The ThinkPad computers use the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS RAM)

ROM Subsystem

The ROM subsystem consists of four banks of 128KB memory. ROM is active when power is turned on and is assigned to the top of the first and last 1MB of address space (hex 000F0000–000FFFFF and hex FFFF0000–FFFFFFFF). After POST checks that system memory is operating correctly, the ROM code is copied to RAM at the same address space, and ROM is disabled.

RAM Subsystem

The RAM subsystem on the system board starts at address hex 00000000 of the address space. The RAM subsystem for the ThinkPad 760XD, 760XL, 765D, or 765L is 64 bits wide.

The 8MB base memory is on the system board. The 8MB memory is on the DIMM adaptor card. Two 144-pin 8 byte dual inline memory module (DIMM) connectors are provided on the DIMM adapter card. One connector accepts an 8MB, a 16MB or a 32MB DIMM. The other connector accepts an 8MB, a 16MB, a 32MB, or a 2-bank-type 64MB DIMM by using a slide switch on the DIMM adapter card. If a 2-bank-type 64MB DIMM is installed, the 8MB memory on the DIMM adaptor card becomes disabled. This means that the memory capacity can be increased up to 104MB when DIMMs are used (see “System Board Memory Connector for DIMM Adapter Card” on page 3-22).

For example, if a 32MB memory and a 64MB memory are installed in the memory slots, the total memory size becomes 104MB, as shown by the following formula:

```
8MB (on the system board) + 32MB (on the left-side memory slot)
+ 64MB (on the right-side memory slot) = 104MB
```

The total amount of usable memory is less than the amount of memory installed because of ROM-to-RAM remapping and power management.

System Memory Map

Memory is mapped by the memory controller registers.

Figure 3-12 shows the memory map for a correctly functioning system. Memory can be mapped differently if POST detects an error in system board memory or RT/CMOS RAM. In the figure, the variable *x* represents the number of 1MB blocks of system board memory starting at or above the hex 100000 boundary.

Hex Address Range	Function
00000000 to 0009FFFF	640KB system board RAM
000A0000 to 000BFFFF	Video RAM
000C0000 to 000C7FFF	System board video BIOS ROM mapped to RAM
000C8000 to 000EFFFF	Channel ROM
000F0000 to 000FFFFF	64KB system board ROM mapped to RAM
00100000 to (00100000 + *x*MB)	*x*MB system board RAM
FFFF0000 to FFFFFFFF	64KB system board ROM (same as 000F0000 to 000FFFFF)

Figure 3-12. System Memory Map

System Board Memory Connector for DIMM Adapter Card

The system board has one memory connector that directly accepts a DIMM adapter card with slots for one or two 144-pin DIMMs as described on page 3-21.

Figure 3-13 on page 3-23 shows the pin assignments for the DIMM adapter card memory connector.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	NC	36	-CAS6	71	NC	106	-CAS2
2	GND	37	VDD	72	NC	107	VDD
3	VDD	38	-CAS5	73	GND	108	-CAS1
4	NC	39	-RAS3	74	NC	109	-RAS3
5	NC	40	-CAS4	75	NC	110	-CAS0
6	NC	41	-RAS2	76	NC	111	-RAS2
7	NC	42	-RAS1	77	NC	112	-WE
8	NC	43	GND	78	NC	113	GND
9	NC	44	NC	79	NC	114	NC
10	NC	45	A11	80	NC	115	A10
11	DIMM1 SCL	46	A9	81	DIMM2 SCL	116	A8
12	DIMM1 SDA	47	A7	82	DIMM2 SDA	117	A6
13	GND	48	A5	83	GND	118	A4
14	D63	49	A3	84	D31	119	A2
15	D62	50	A1	85	D30	120	A0
16	D47	51	NC	86	D15	121	NC
17	D61	52	VDD	87	D29	122	VDD
18	D46	53	D55	88	D14	123	D23
19	D60	54	D39	89	D28	124	D7
20	D45	55	D54	90	D13	125	D22
21	D44	56	D38	91	D12	126	D6
22	VDD	57	D37	92	VDD	127	D5
23	D59	58	D53	93	D27	128	D21
24	D58	59	D36	94	D26	129	D4
25	D43	60	D52	95	D11	130	D20
26	D57	61	GND	96	D25	131	GND
27	D42	62	D51	97	D10	132	D19
28	D56	63	D35	98	D24	133	D3
29	D41	64	D50	99	D9	134	D18
30	D40	65	D34	100	D8	135	D2
31	GND	66	D33	101	GND	136	D1
32	DIMMID1	67	D49	102	NC	137	D17
33	DIMMID0	68	D32	103	NC	138	D0
34	-RAS1	69	D48	104	-OE	139	D16
35	-CAS7	70	VDD	105	-CAS3	140	VDD

Figure 3-13. DIMM Adapter Card Memory Connector Pin Assignments

RT/CMOS RAM

The RT/CMOS RAM (real-time clock/complementary metal-oxide semiconductor RAM) module contains the real-time clock and 128 bytes of CMOS RAM. The clock circuitry uses 14 bytes of this memory; the remainder is allocated to configuration and system-status information. A battery is built into the module to keep the RT/CMOS RAM active when the power supply is not turned on. In addition to the 128 bytes of CMOS/RAM, a CMOS/RAM extension of 4KB is provided for configuration and other system information.

Figure 3-14 on page 3-24 lists the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000–00D	Real-time clock
00E	Diagnostic status
00F	Shutdown status
010	Diskette drive type
011	Hard disk 2 and 3 drive type
012	Hard disk 0 and 1 drive type
013	Reserved
014	Equipment
015, 016	Low and high base memory
017, 018	Low and high expansion memory
019	Hard disk 0 extended byte
01A	Hard disk 1 extended byte
01B	Hard disk 2 extended byte
01C	Hard disk 3 extended byte
01D–02D	Reserved
02E, 02F	Checksum
030, 031	Low and high usable memory above 1MB
032	Date-century
033–07F	Reserved

Figure 3-14. RT/CMOS RAM Address Map

RT/CMOS Address and NMI Mask Register (Hex 0070)

The NMI mask register is used with the RT/CMOS data register (hex 0071) to read from and write to the RT/CMOS RAM bytes.

Attention
The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent failures of the RT/CMOS RAM can occur.

Bit	Function
7	NMI mask
6–0	RT/CMOS RAM address

Figure 3-15. RT/CMOS Address and NMI Mask Register (Hex 0070)

Bit 7 When this write-only bit is set to 1, the NMI is masked (disabled). This bit is set to 1 by a power-on reset.

Bits 6–0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

The RT/CMOS data register is used with the RT/CMOS address and NMI mask register (hex 0070) to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7–0	RT/CMOS data

Figure 3-16. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, you should mask interrupts to prevent other interrupt routines from changing the RT/CMOS address register before data is read or written. After I/O operations, you should leave the RT/CMOS address and NMI mask register (hex 0070) pointing to status register D (hex 00D).

Attention
The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent failures of the RT/CMOS RAM can occur.

Writing to the RT/CMOS RAM requires the following:

1. Write the RT/CMOS RAM address to the RT/CMOS address and NMI mask register (hex 0070).
2. Write the data to the RT/CMOS data register (hex 0071).
3. Write the address, hex 0F, to the RT/CMOS and NMI mask register; this leaves hex 0070 pointing to the shutdown status byte (hex 0F).
4. Read address hex 0071 to restore the RT/CMOS.

Reading from the RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI mask register (hex 0070).
2. Read the data from the RT/CMOS data register (hex 0071).
3. Write the address, hex 0F, to the RT/CMOS and NMI mask register; this leaves hex 0070 pointing to the shutdown status byte (hex 0F).
4. Read address hex 0071 to restore the RT/CMOS.

Real-Time Clock Bytes (Hex 000–00D): Bit definitions and addresses for the real-time clock bytes are shown in Figure 3-17.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second alarm	1
002	Minutes	2
003	Minute alarm	3
004	Hours	4
005	Hour alarm	5
006	Day of week	6
007	Date of month	7
008	Month	8
009	Year	9
00A	Status register A	10
00B	Status register B	11
00C	Status register C	12
00D	Status register D	13

Figure 3-17. Real-Time Clock Bytes (Hex 000–00D)

Note: The setup program initializes status registers A and B when the time and date are set. Interrupt 1AH is the BIOS interface to read and set the time and date; it initializes the registers in the same way that the setup program does.

Status Register A (Hex 00A)

Bit	Function
7	Update in progress (UIP)
6	Countdown chain 1 - resets countdown chain 0 - countdown chain enabled
5	Oscillator enable 0 - oscillator off 1 - oscillator on
4	Bank select
3–0	Rate-selection bits

Figure 3-18. Status Register A (Hex 00A)

Bit 7 This bit is a status flag that can be monitored. When this bit is 1, the update transfer will soon occur. When this bit 0, the update transfer will not occur for at least 244 μs.

Bits 6–5 When these bits are a pattern of 01, the oscillator is turned on and the RTC is allowed to keep time. The next update will occur at 500 ms after a pattern of 01 is written to these bits.

Bits 4 To use the original bank of memory, select 0. To use the extended registers, select 1.

Bits 3–0 These bits allow the selection of a divider output frequency or disable the divider output.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Enable periodic interrupt
5	Enable alarm interrupt
4	Enable update-ended interrupt
3	Enable square wave
2	Date mode
1	24-hour mode
0	Enable daylight-saving time

Figure 3-19. Status Register B (Hex 00B)

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the count at a rate of one cycle per second. When set to 1, it immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in status register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in status register A. The system initializes this bit to 0.

Bit 2 This bit indicates whether the binary-coded-decimal (BCD) or binary format is used for time-and-date calendar updates. When set to 1, this bit indicates the binary format. The system initializes this bit to 0.

Bit 1 This bit indicates whether the hours byte is in 12-hour or 24-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight-saving-time mode. When set to 0, this bit disables the daylight-saving-time mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt request flag
6	Periodic interrupt flag
5	Alarm interrupt flag
4	Update-ended interrupt flag
3–0	Reserved

Figure 3-20. Status Register C (Hex 00C)

Note: Interrupts are enabled by bits 6, 5, and 4 in status register B.

Bit 7 When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt has occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt has occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt has occurred.

Bits 3–0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6–0	Reserved

Figure 3-21. Status Register D (Hex 00D)

Bit 7 This read-only bit monitors the internal battery. When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power and the data in CMOS is no longer valid.

Bits 6–0 These bits are reserved.

CMOS RAM Configuration

Figure 3-22 shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-time clock power
6	Configuration record and checksum status
5	Incorrect configuration
4	Memory size mismatch
3	Hard disk controller/drive C initialization status
2	Time status indicator
1, 0	Reserved

Figure 3-22. Diagnostic Status Byte (Hex 00E)

Bit 7 When set to 1, this bit indicates that the real-time clock has lost power.

Bit 6 When set to 1, this bit indicates that the checksum is incorrect.

Bit 5 This bit indicates the results of a power-on check of the equipment byte (hex 014). When set to 1, this bit indicates that the configuration information is incorrect.

Bit 4 When set to 1, this bit indicates that the memory size does not match the configuration information.

Bit 3 When set to 1, this bit indicates that the controller or hard disk drive failed initialization.

Bit 2 When set to 1, this bit indicates that the time is invalid.

Bits 1, 0 These bits are reserved.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of the installed diskette drive.

Bit	Drive Type
7–4	Diskette drive type
3–0	Reserved

Figure 3-23. Diskette Drive Type Byte (Hex 010)

Bits 7–4 These bits indicate the diskette drive type.

Bits 7–4	Description
0 1 1 0	Diskette drive (2.88MB)
0 1 0 0	Diskette drive (1.44MB)
Note: Combinations not shown are reserved.	

Figure 3-24. Diskette Drive Type Bits 7–4

Bits 3–0 These bits are reserved.

Hard Disk Drive Type Byte (Hex 011): This byte defines the type of hard disk drive installed. Hex 00 indicates that no hard disk drive is installed.

Bit	Drive Type
7–4	Hard disk drive type 2
3–0	Hard disk drive type 3

Figure 3-25. Hard Disk Type Byte (Hex 011)

Bit 7–4	Description
0 0 0 0	No drive installed for hard disk drive 2
1 1 1 1	Use CMOS 1BH for hard disk drive 2

Figure 3-26. Hard Disk Drive Type 2 (Bits 7–4)

Bit 3–0	Description
0 0 0 0	No drive installed for hard disk drive 3
1 1 1 1	Use CMOS 1CH for hard disk drive 3

Figure 3-27. Hard Disk Drive Type 3 (Bits 3–0)

Hard Disk Drive Type Byte (Hex 012): This byte defines the type of hard disk drive installed. Hex 00 indicates that no hard disk drive is installed.

Bit	Drive Type
7–4	Hard disk drive 0
3–0	Hard disk drive 1

Figure 3-28. Hard Disk Drive Type Byte

Reserved Bytes (Hex 013): These bytes are reserved.

Equipment Byte (Hex 014): This byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Description
7, 6	Number of diskette drives
5, 4	Display operating mode
3, 2	Reserved
1	Coprocessor presence
0	Diskette drive 0 presence

Figure 3-29. Equipment Byte

Bits 7, 6 These bits indicate the number of installed diskette drives.

Bits 7,6	Number of Diskette Drives
0 0	One drive
0 1	Reserved
1 0	Reserved
1 1	Reserved

Figure 3-30. Installed Diskette Drive Bits

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port.

Bits 5,4	Display Operating Mode
0 0	Reserved
0 1	40-column mode
1 0	80-column mode
1 1	Monochrome mode

Figure 3-31. Display Operating Mode Bits

Bits 3–2 These bits are reserved.

Bit 1 When set to 1, this bit indicates that a coprocessor is installed.

Bit 0 When set to 1, this bit indicates that physical diskette drive 0 is installed.

Low and High Base Memory Bytes (Hex 015 and Hex 016): The low and high base memory bytes define the amount of memory below the 640KB address space.

The value in these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 indicates 640KB. The low byte is hex 015; the high byte is hex 016.

Low and High Expansion Memory Bytes (Hex 017 and Hex 018): The low and high expansion memory bytes define the amount of memory above the 1MB address space.

The value in these bytes represents the number of 1KB blocks of expansion memory. For example, hex 0800 indicates 2048KB. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 01D–02D): These bytes are reserved.

Configuration Checksum Bytes (Hex 02E and Hex 02F): The configuration checksum bytes contain the checksum character for bytes hex 010 through hex 02D of the 64-byte CMOS RAM. The high byte is hex 02E; the low byte is hex 02F.

Low and High Usable Memory Bytes (Hex 030 and Hex 031): The low and high usable memory bytes define the total amount of contiguous memory from 1MB to 20MB.

The hexadecimal values in these bytes represent the number of 1KB blocks of usable memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 30; the high byte is hex 31.

Date-Century Byte (Hex 032): Bits 7 through 0 of the date-century byte contain the binary-coded decimal value for the century. For information about reading and setting this byte, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface*.

Reserved Bytes (Hex 033–07F): These bytes are reserved.

Miscellaneous System Functions and Ports

This section provides information about nonmaskable interrupts (NMIs), the power-on password, and hardware compatibility.

Nonmaskable Interrupt (NMI)

The NMI signals the system microprocessor that a channel check timeout has occurred. This situation can cause lost data or an overrun error on some I/O devices. The NMI masks all other interrupts. The interrupt return (IRET) instruction restores the interrupt flag to the state it was in before the interrupt occurred. A system reset causes a reset of the NMI.

The NMI requests from system board channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address register. See “RT/CMOS Address and NMI Mask Register (Hex 0070)” on page 3-25. The power-on default of the NMI mask is 1 (NMI disabled).

Attention
The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent failures of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the write and read functions of this port are shown in the following figures:

Bit	Function
7–4	Reserved
3	Enable channel check
2	Enable PCI SERR#
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-32. System Control Port B (Hex 0061, Write)

Bit	Function
7	PCI SERR# (PCI error) status
6	Channel check status
5	Timer 2 output
4	Toggles with each refresh request
3	Enable channel check
2	Enable PCI SERR# (PCI error) check
1	Enable speaker data
0	Timer 2 gate to speaker

Figure 3-33. System Control Port B (Hex 0061, Read)

Bit 7 If a system board error occurs and the PCI SERR# line is activated, this bit is set to 1.

Bit 6 When set to 1, this bit indicates that a channel check has occurred.

Bit 5 When read, this bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 When read, this bit toggles for each refresh request.

Bit 3 When set to 0, this bit enables the channel check. This bit is set to 1 during a power-on reset.

Bit 2 When set to 0, this bit enables the PCI SERR#.

Bit 1 When set to 1, this bit enables the speaker data.

Bit 0 When set to 1, this bit enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7–4	Reserved
3	Security lock latch
2	Reserved (must be set to 0)
1	Alternate gate A20
0	Alternate hot reset

Figure 3-34. System Control Port A (Hex 0092)

Bits 7–4 These bits are reserved.

Bit 3 This bit provides a security lock for the secured area of RT/CMOS. When this bit is set to 1, the 8-byte power-on password is locked by the software. After this bit is set by POST, it can be cleared only by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternative method of resetting the system microprocessor. This alternative method supports operating systems requiring faster operation than that provided on the IBM Personal Computer AT. Resetting the system microprocessor switches the microprocessor from protected mode to real address mode.

This bit is set to 0 by either a system reset or a write operation. When a write operation changes this bit from 0 to 1, the 'processor reset' signal is pulsed after the reset has occurred. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is set to 0, POST assumes that the system was just powered on. If the bit is set to 1, POST assumes that the microprocessor has been switched from protected mode to real mode.

When bit 0 is used to reset the system microprocessor to the real mode, use the following procedure:

1. Disable all maskable and nonmaskable interrupts.

2. Reset the system microprocessor by writing a 1 to bit 0.
3. Issue a Halt instruction to the system microprocessor.
4. Reenable all maskable and nonmaskable interrupts.

If you do not follow this procedure, the results are unpredictable.

Note: Whenever possible, use BIOS as an interface to reset the system microprocessor to the real mode. For more information about resetting the system microprocessor, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface*.

Power-On Password

RT/CMOS RAM has 8 bytes reserved for the power-on password and the check character. The 8 bytes are initialized to hex 00. The microprocessor can access these bytes only during POST. After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by any program.

During power-on password installation, the password (1 to 7 characters) is stored in the security space.

Installing the password is a function of the built-in system program *Easy-Setup*. The power-on password does not appear on the screen when it is installed, changed, or removed. After the power-on password has been installed, it can be changed or removed only during POST.

The computer also can have a keyboard password. For more information, see the keyboard and auxiliary device controller section of the *IBM Personal System/2 Hardware Interface Technical Reference*.

Other Passwords

In addition to the power-on password, the computer provides two more passwords:

- The **hard-disk password** (HDP) protects the data on your removable hard disk drive from being accessed by unauthorized persons.
- The **supervisor password** protects the system information in Easy-Setup from being changed.

For more information about these passwords, refer to the *ThinkPad User's Guide*.

Selectable Drive-Startup Sequence

Selectable drive-startup (selectable boot) allows you to control the startup sequence of the drives in your computer. The order in which the computer looks for the drives for your operating system is the *drive-startup sequence*. If you are working with multiple operating systems, you might want to change the drive-startup sequence to load the operating system from the hard disk without first checking the diskette drive, or to do a remote program load (RPL).

Attention
When changing your startup sequence, you must be extremely careful when doing write operations (such as copying, saving, or formatting). Your data or programs can be overwritten if you select the wrong drive.

For more information about the selectable drive-startup sequence, refer to the *ThinkPad User's Guide*.

Hardware Compatibility

The computer supports most of the interfaces used by the IBM Personal Computer AT* and the Personal System/2* (PS/2*) products. In many cases, the command and status organization of these interfaces is maintained.

The functional interfaces for the computer are compatible with the following:

- The Intel 8259 interrupt controllers (edge trigger mode).
- The Intel 8254 timers driven from 1.193 MHz (channels 0, 1, and 2).
- The Intel 8237 DMA controller-address/transfer counters, page registers, and status fields only. The command and request registers, and the rotate and mask functions, are not supported. The mode register is partially supported.
- The NS16550 serial communications controller.
- The Intel Pentium microprocessor.
- The Intel 8086**, 8088**, 80286**, 80386**, and i486DX microprocessors.
- The Intel 8087**, 80287**, 80387** math coprocessors.
- The Intel 82077AA** diskette drive controller.
- The keyboard interface at addresses hex 0060 and hex 0064.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.

Error Codes

POST returns a three or more character code message to indicate the type of test that failed. Figure 3-35 lists the failure indicated with the associated error code.

Error Code	Description
101	Interrupt failure.
102	Timer failure.
103	Timer interrupt failure.
104	Protected mode failure.
105	Last 8042 command not accepted.
107	NMI test failure.
108	Timer bus test failure.
109	Low meg-chip select test.
110	Planar parity.
111	I/O parity.
118	Planar parity error logged.
158	A supervisor password is set, but no hard disk password is set.
159	The hard disk password is not identical to the supervisor password.
161	Dead battery.
163	Date and time are not set; clock not updated.
173	CMOS CRC error.
174	Configuration error.
175	Bad EEPROM CRC 1.
177	Bad supervisor password checksum.
178	EEPROM is not functional.
179	NVRAM error log full.
183	Supervisor password is needed.
184	Bad power-on password checksum.
185	Corrupted startup boot sequence.
186	Inconsistency between EEPROM and security lock latch 2.
188	Bad EEPROM CRC 2.
189	Too many passwords attempted.
190	Critically low battery condition detected.
191*XX*	PM initialization error. (*X* can be any character.)
195	Configuration mismatch error found during hibernation wake-up.
196	Critical error found during hibernation wake-up.
201	Memory data error.
202	Memory line error 00 through 15.
203	Memory line error 16 through 23.
215	Memory test failure on on-board memory.
221	ROM to RAM remap error.
301	Keyboard error.

Figure 3-35 (Part 1 of 2). Error Codes

Error Code	Description
601	Diskette drive or controller error.
602	No valid boot record on diskette.
604	Invalid diskette drive error.
1101	Serial-A test failure.
1201	Serial-B test failure.
1701	Hard disk controller failure.
1780, 1790	Hard disk 0 error.
1781, 1791	Hard disk 1 error.
2401	System board video error.
8081	PCMCIA presence test failure (PCMCIA revision number also checked).
8082	PCMCIA register test failure.
8601	System bus error (8042 mouse interface).
8602	External mouse error.
8603	System bus error or mouse error.
8611	System bus error (I/F between 8042 and IPDC).
8612	TrackPoint III error.
8613	System board or TrackPoint III error.
I9990301	Hard disk error.
I9990302	Invalid hard disk boot record.
I9990303	Bank-2 flash ROM checksum error.
I9990305	No bootable device.

Figure 3-35 (Part 2 of 2). Error Codes

Section 4. Subsystems

This section describes the video, DSP, Audio, IR, Enhanced video, and PCMCIA subsystems of the ThinkPad computers. It also provides the Programmable Option Select (POS) information for the DSP and IR subsystems.

Video Subsystem

The video subsystem consists of the SVGA video controller and video random-access memory (VRAM). The video subsystem supports an IBM thin-film transistor (TFT) or dual-scan super twisted nematic (DSTN) as follows:

LCD type	VRAM size	Color depth		Resolution	
		On the LCD	On the external display	On the LCD	On the external display
SVGA TFT	1MB	65,536	16,777,216	800×600	640×480 800×600 1024×768
XGA TFT	2MB	65,536	16,777,216	1024×768	640×480 800×600 1024×768 1280×1024

The video subsystem also supports PS/2 analog displays without any additional adapters.

Note: Use of any video subsystem features not documented in this book can result in future incompatibility.

Color	Resolution
65,536 colors	640×480
	800×600
	1024×768 *
16,777,216 colors	640×480
	800×600 *
* For 2MB video RAM models only.	

Video Modes

The video subsystem supports the modes listed in Figure 4-1 and Figure 4-2 on page 4-4. VESA112 and VESA115 modes are supported only for the external PS/2 display.

Table 4-1. BIOS video VGA modes

Mode (Hex)	Type	Colors	Alpha-numeric Format	Buffer Start Address	Box Size	Max Pages	Pels	Expanded Size	
								SVGA	XGA
0, 1	A/N	16	40×25	B8000	8×8	8	320×200	800×600	960×600
0*, 1*	A/N	16	40×25	B8000	8×14	8	320×350	800×525	960×700
0#, 1#	A/N	16	40×25	B8000	8×16	8	320×400	800×600	960×600
2, 3	A/N	16	80×25	B8000	8×8	8	640×200	800×600	960×600
2*, 3*	A/N	16	80×25	B8000	8×14	8	640×350	800×525	960×700
2#, 3#	A/N	16	80×25	B8000	8×16	8	640×400	800×600	960×600
4, 5	APA	4	40×25	B8000	8×8	1	320×200	800×600	960×600
6	APA	2	80×25	B8000	8×8	1	640×200	800×600	960×600
7*	A/N	–	80×25	B0000	8×14	8	640×350	800×525	960×700
7#	A/N	–	80×25	B0000	8×16	8	640×400	800×600	960×600
D	APA	16	40×25	A0000	8×8	8	320×200	800×600	960×600
E	APA	16	80×25	A0000	8×8	4	640×200	800×600	960×600
F	APA	–	80×25	A0000	8×14	2	640×350	800×525	960×700
10	APA	16	80×25	A0000	8×14	2	640×350	800×525	960×700
11	APA	2	80×30	A0000	8×16	1	640×480	800×600	960×720
12	APA	16	80×30	A0000	8×16	1	640×480	800×600	960×720
13	APA	256	40×25	A0000	8×8	1	320×200	800×600	960×600

Figure 4-1. BIOS Video VGA Modes

The following shows the video BIOS extended modes for the 760XD, 765D, or 765L (containing a video chip Trident 9385 and 2MB VRAM) or the 760XL (containing the Trident 9385 and 1MB VRAM):

Video mode	VESA mode number	External monitor								TFT LCD		DSTN LCD	TV out**	
		87i	96i	56	60	70	72	75	85	SVGA	XGA	SVGA	NTSC	PAL
VGA modes	—				o					o	o	o	o	o
640x480x256	101h				o		o	o	o	o	o	o[1]	o	o
640x480x64k	111h				o		o	o	o[1]	o[1]	o	o[1]	o	o[2]
640x480xTrue	112h				o		o	o	o[1]					
* 800x600x16	102h				o			o	o	o	o	o		o
800x600x256	103h				o			o	o	o	o	o[1]		o
800x600x64k	114h				o[1]			o	o[1]	o[1]	o	o[1]		o[2]
800x600xTrue	115h				o[1]			o[1]						
* 1024x768x16	104h	o			o	o		o			o			
1024x768x256	105h	o[1]			o[1]	o		o			o			
1024x768x64k	117h				o[1]			o[1]			o			
1024x768xTrue	118h													
* 1280x1024x16	106h	o[1]			o[1]									
1280x1024x256	107h													
1280x1024x64k	11Ah													

Note:

*: 16 color modes are not supported.
**: For the Enhanced video model only.
o: Supported by both 2MB and 1MB VRAM model.
o[1]: Supported by the 2MB VRAM model only.
o[2]: Supported by the SVGA TFT model only.

Figure 4-2. BIOS Video Extended Modes—Trident 9385

DSP Subsystem

Digital signal processing (DSP) is a method of processing data. In particular, it is a way to rapidly process a continuous stream of data (for example, voice data over a telephone line). Unlike central processing unit (CPU) chips, which usually execute a series of instructions on the same data, DSP chips execute the same instruction over and over on this system of data. As a result, DSP technology is well suited for processing real-time events—data transmission, audio playback, and voice recognition.

The Mwave DSP subsystem provides ThinkPad with a full complement of audio and telephony features:

- High-quality audio (44.1 kHz MPC-2 16-bit audio)
- General MIDI compatible, 32-voice wave table synthesizer
- Sound Blaster** support
- 28.8 kilobaud data/fax modem
- Full-featured telephone
- Answering machine
- Headphone-free, full-duplex speaker phone

System Settings

Mwave DSP

The Mwave DSP subsystem provides three system settings: I/O address, IRQ level, and DMA channel.

I/O Address	IRQ Level	DMA Channel
4E30–4E3F (default)	IRQ 5	DMA 0
8E30–8E3F	IRQ 7	DMA 1
CE30–CE3F	IRQ 10 (default)	DMA 6
	IRQ 11	DMA 7 (default)
	IRQ 15	

MIDI Port Function (760XD and 765D)

The MIDI port function provides one system setting:

I/O Address
0300–0302
0330–0332 (default)

Sound Blaster Support Function

The Sound Blaster support function provides three system settings: I/O address, IRQ level, and DMA channel.

I/O Address	IRQ Level	DMA Channel
0220–0233 (default)	IRQ 5 (default)	DMA 0
0240–0253	IRQ 7	DMA 1 (default)
0338–033F (FM synthesizer)	IRQ 10	DMA 6
	IRQ 11	DMA 7

Telephony (Modem) Function

The telephony (modem) function provides the following settings:

Serial Port
COM1 (I/O: 03F8h - IRQ 4)
COM2 (I/O: 02F8h - IRQ 3) (default)
COM3 (I/O: 03E8h - IRQ 4)
COM4 (I/O: 02E8h - IRQ 3)

Audio Port Specifications

- Audio Output:
  - ⅛-inch mini-jack for headphone
  - Headphone speaker output: 15.6 mW (32 ohm) maximum
  - Maximum output level: 1.9 V pp
  - Output impedance: 75 ohm
- Audio Input:
  - ⅛-inch mini-jack for microphone or line input
  - Microphone gain: 32 dB minimum, 54.5 dB maximum
  - Maximum input level:
    Microphone: 64.5 mV pp
    Line In: 5.3 V pp

– Input impedance:
  Microphone: 9 k ohm
  Line In: 8 k ohm

Audio Subsystem

ESS AudioDrive subsystem (for the 760EL and 760ELD only) gives 16-bit stereo audio with high-quality FM music synthesis using four operators per voice. It can record, compress, and play back voice, sound, and music with built-in mixer controls.

The AudioDrive provides the computer with the following audio features:

- High-quality audio (44.1 kHz MPC-2 16-bit audio)
- General MIDI compatible, 32-voice wave table synthesizer
- Sound Blaster support

System Settings

MIDI Port Function

The MIDI port I/O address is as follows (only when docked to the docking station):

I/O Address
0300–0301
0330–0331 (default)

Sound Blaster Support Function

The Sound Blaster support function provides three system settings: I/O address, IRQ level, and DMA channel.

I/O Address	IRQ Level	DMA Channel
0220–022F (default)	IRQ 5 (default)	DMA 0
0240–024F	IRQ 7	DMA 1 (default)
0338–038B (FM synthesizer)	IRQ 10	
	IRQ 11	

Audio Port Specifications

- Audio Output:
  - ⅛-inch mini-jack for headphone
  - Headphone speaker output: 22 mW (32 ohm) maximum
  - Maximum output level: 2.4 V pp
  - Output impedance: 75 ohm
- Audio Input:
  - ⅛-inch mini-jack for microphone or line input
  - Microphone gain: 26 dB minimum, 48.5 dB maximum
  - Maximum input level:
    Microphone: 1255 mV pp
    Line In: 4.0 V pp
  - Input impedance:
    Microphone: 47 k ohm
    Line In: 30 k ohm

Infrared (IR) Subsystem

The IR subsystem supports the following functions:

- ThinkPad mode
  - 1,152,000 bits per second with DMA
  - FM/NRZI with flash (1/4) modulation
- Generic mode[1]
  - 115,200 bits per second
  - Flash (3/16) modulation/1.6 microsecond pulse
- Sharp** mode
  - 9,600 bits per second
  - Digital amplitude shift keying modulation

System Settings

The I/O address can be selected from the following with the system utility program. The IR subsystem uses one serial port address and one IR controller register address.

I/O Address	
03F8–03FF	Serial port 1 (default)
02F8–02FF	Serial port 2
03E8–03EF	Serial port 3
02E8–02EF	Serial port 4
01A0–01AF	IR controller register 1 (default)
01B0–01BF	IR controller register 2
01C0–01CF	IR controller register 3
01D0–01DF	IR controller register 4

[1] Designed to be compatible with the IrDA** Data Link Specification Version 1.0.

IRQ Level and DMA Channel

The IR subsystem uses one IRQ level and two DMA channels for ThinkPad mode. (Generic mode and Sharp mode do not require DMA channels.)

IRQ Level	DMA Channel
IRQ 3	DMA 0
IRQ 4 (default)	DMA 3
IRQ 5	
IRQ 10	
IRQ 11	
IRQ 15	

Enhanced Video Subsystem (760XD and 765D)

The enhanced video subsystem consists of the following functions:

- Video acceleration (hardware scaling, interpolation, color space conversion)
- Video overlay
- Video capture
- One video-in jack (NTSC or PAL[1] input)
- One video-out jack
- MPEG playback

Video Port Specification

- S-Video Jack (In/Out)
  - 4-pin mini DIN jack (provided with attached special cable)
  - Color standard: NTSC or PAL
  - Y signal: 1 V pp 75 ohm with negative composite sync
  - C signal: 0.286 V pp 75 ohm
- Composite Video Jack (In/Out)
  - Pin jack (provided with attached special cable)
  - Color standard: NTSC or PAL
  - 1 V pp 75 ohm with negative composite sync

[1] NTSC: National Television Standards Committee
PAL: Phase-alternation-by-line

PCMCIA Subsystem

The system board has two PCMCIA (Personal Computer Memory Card International Association) slots that support the following types of PC Card:

- 16bit PC Card Type–I, II, III 5V, 3.3V
- 32bit PC Card Type–I, II, III 5V, 3.3V

However, x.xV, y.yV, DMA and ZV are not supported.

The maximum current allowable for both slots at the same time is:

- 1.0 A at 5 V dc
- 0.8 A at 3.3 V dc
- 0.1 A at 12 V dc

The PCI1130 PCI-TO-CARDBUS CONTROLLER UNIT[2] is used as the PC card controller in the system unit. The available interrupt levels are IRQ 3, 4, 5, 7, 9, 10, 11, 14, and 15. The IRQ 15 signal is connected to pin 161 of the PC card controller module at the controller side. Interrupt levels INTA# and INTB# for PCI bus cannot be used.

The system unit resumes operation from suspend mode when it receives the 'RI_OUT' signal. The Type I and Type II PC cards can be installed into either the upper or the lower slot, or into both slots at the same time. The Type III PC card, however, must be installed only in the lower slot. The Type II PC card cannot be used in the upper slot when a Type III PC card is used.

[2] Manufactured by Texas Instruments corporation.

The PCMCIA slots are designed according to the following PCMCIA standards and specifications:

Standards and Specifications	Characteristics
PCMCIA Card standard	Release 2.0 or 2.1
PCMCIA Socket Services interface specifications	Release 2.0 or 2.1
PCMCIA Card Services interface specifications	Release 2.0 or 2.1
PC Card physical configuration	Type II and Type III
Supported voltage	5.0 V dc or 3.3 V dc

Figure 4-3. PCMCIA Standards and Specifications

Pin Assignments

Figure 4-4 shows the pin assignments for the PCMCIA slots.

Pin	16-bit PC Card	32-bit PC Card
1	Ground	Ground
2	D3	CAD0
3	D4	CAD1
4	D5	CAD3
5	D6	CAD5
6	D7	CAD7
7	CE1#	CC/BE0#
8	A10	CAD9
9	OE	CAD11
10	A11	CAD12
11	A9	CAD14
12	A8	CC/BE1#
13	A13	CPAR
14	A14	CPERR#
15	WE#	CGNT#
16	IRQ#	CINT#
17	Vcc	Vcc
18	Vpp	Vpp
19	A16	CCLK
20	A15	CIRDY#
21	A12	CC/BE2#
22	A7	CAD18
23	A6	CAD20
24	A5	CAD21
25	A4	CAD22
26	A3	CAD23
27	A2	CAD24
28	A1	CAD25
29	A0	CAD26
30	D0	CAD27

Figure 4-4 (Part 1 of 2). PCMCIA PC Card Slot Pin Assignments

Pin	16-bit PC Card	32-bit PC Card
31	D1	CAD29
32	D2	Reserved
33	IOIS16#	CCLKRUN#
34	Ground	Ground
35	Ground	Ground
36	CD1#	CCD1#
37	D11	CAD2
38	D12	CAD4
39	D13	CAD6
40	D14	Reserved
41	D15	CAD8
42	CE2	CAD10
43	VS1#	CVS1
44	IORD#	CAD13
45	IOWR#	CAD15
46	A17	CAD16
47	A18	Reserved
48	A19	CBLOCK#
49	A20	CSTOP#
50	A21	CDEVSEL#
51	Vcc	Vcc
52	Vpp	Vpp
53	A22	CTRDY#
54	A23	CFRAME#
55	A24	CAD17
56	A25	CAD19
57	AS2#	CVS2
58	RESET	CRST#
59	WAIT#	CSERR#
60	INPACK#	CREQ#
61	REG#	CC/BE3#
62	SPKR#	CAUDIO
63	STSCHG#	CSTSCHG
64	D8	CAD28
65	D9	CAD30
66	D10	CAD31
67	CD2#	CCD2#
68	GND	GND

Figure 4-4 (Part 2 of 2). PCMCIA PC Card Slot Pin Assignments

The maximum current for +5 V dc is 1.0 A (including both slots and V pp).

The maximum current for +12 V dc is 0.1 A (including both slots and V pp). When the computer is in suspend mode, it requires a current of 0.05 A.

Programmable Option Select (POS)

This section provides the POS information for the DSP and IR subsystems.

DSP Subsystem Setup

Take the following precautions before you set individual bits in the POS registers:

- Set bit 3 in the system board Enable/Setup register (hex 0094) to 0 to put the DSP subsystem into setup mode.
- Set other bits in the system board Enable/Disable register to 1 to prevent other subsystems from entering setup mode.

  Note: During the setup operation, the DSP subsystem is disabled.

After the setup operation is complete, take the following precaution:

- Set the system board Enable/Setup register to hex FF.

System Board DSP Subsystem POS Register 2 (Hex 0102)

This section describes the setting for the system board DSP subsystem POS register 2 (hex 0102). When the DSP subsystem is in setup mode, this read/write register enables or disables the system board DSP subsystem functions.

Bit	Function
7–1	Reserved
0	Enable DSP subsystem functions

Figure 4-5. System Board DSP Subsystem POS Register 2 (Hex 0102)

IR Subsystem Setup

Take the following precautions before you set individual bits in the POS registers:

- Set bit 0 in the system board Enable/Setup register (hex 0094) to 0 to put the IR subsystem into setup mode.
- Set other bits in the system board Enable/Disable register to 1 to prevent other subsystems from entering setup mode.

  Note: During the setup operation, the IR subsystem is disabled.

After the setup operation is complete, take the following precaution:

- Set the system board Enable/Setup register to hex FF.

System Board IR Subsystem POS Register 2 (Hex 0102)

This section describes the setting for the system board IR subsystem POS register 2 (hex 0102). When the IR subsystem is in setup mode, this read/write register enables or disables the system board IR subsystem functions.

Bit	Function
7–1	Reserved
0	Enable IR subsystem functions

Figure 4-6. System Board IR Subsystem POS Register 2 (Hex 0102)

IDE Channel on the UltraBay

A primary IDE channel is provided on the UltraBay connector, providing two system settings: I/O address and IRQ level.

I/O Address	IRQ Level
01F0–01F7 03F6–03F7	IRQ 14

When a hard disk is attached to the hard disk connector, an IDE device on the UltraBay will be a primary slave. (The hard disk attached to the hard disk connector is primary master.) When no hard disk is attached to the hard disk connector, an IDE device on the UltraBay will be a primary master.

MIDI/Joystick Port

The MIDI/Joystick port consists of the following functions:

- MIDI port (in/out)
- Joystick port

A standard game port connector is provided with a MIDI/Joystick cable.

MIDI Interface

A MIDI communication function is provided with the DSP subsystem. The MIDI interface is compatible with MPU-401 (UART mode).

Joystick Interface

A joystick interface is provided at I/O address 0201. You can select whether to enable or disable it with the ThinkPad Features program.

Appendix A. System Resources

The following summarizes the available system resources for the computer and docking stations. Values in parentheses are alternative values that are selectable in the ThinkPad Features program or application programs. The default values are highlighted.

System Resources	IRQ	I/O Address (Hex)	Memory Address (Hex)	DMA Channel
Timer	0	0040–0043	None	None
Keyboard	1	0060 and 0064	None	None
Serial Port	**Disabled**	**Disabled**	None	None
	4	03F8–03FF		
	3	02F8–02FF		
	4	03E8–03EF		
	3	02E8–02EF		
Parallel Port	**7**	**03BC–03BE** (and **07BC–07BE**[1])	None	0, 1, 3, or disabled[1]
	7	0378–037F (and 0778–077A[1])		
	5	0278–027F (and 0678–067A[1])		
	Disabled	Disabled		
Infrared Port	**4**, 3, 5, 10, 11, 15, or disabled	**01A0–01AF**, 01B0–01BF, 01C0–01CF, or 01D0–01DF and **03F8–03FF**, 02F8–02FF, 02E8–02EF, or 03E8–03EF	None	**0 and 3** or disabled
Diskette Controller	6	03F0–03F7	None	2

System Resources	IRQ	I/O Address (Hex)	Memory Address (Hex)	DMA Channel
Video Controller	None	03BA, 03B4–03B5, 03C0–03CF, 03D4–03D5, 03D8–03D9, 03DA, 2100–21FF, 43C6–43C9, 46E8, and 83C6–83C9	A0000–BFFFF and C0000–C7FFF	None
Enhanced Video/MPEG (for the Enhanced Video model)	**11**, 3, 4, 5, 7, 9, 10, 15, or disabled[1]	None	(Automatically set by the system)[1]	None
Mwave DSP Device	**10**, 5, 7, 11, 15, or disabled	**4E30–4E3F**, 8E30–8E3F, or CE30–CE3F	None	**7**, 0, 1, or 6
Audio (ESS) Device	**5**, 7, 10, 11, or disabled	**0220—022F,** 0240—024F, or 0338—038B	None	0 or **1**
Sound Blaster	**5**, 7, 10, 11, or disabled[2]	**0220–022F** or 0240–024F	None	**1**, 0, 6, or 7
MIDI Port	**5**, 7, 10, 11, or disabled[2]	**0330–0332** or 0300–0302	None	None
Joystick Port	None	0201	None	None
Mwave Modem	**3**	**02F8–02FF**	None	None
	4	03F8–03FF		
	4	03E8–03EF		
	3	02E8–02EF		
	Disabled	Disabled		
Hard Disk Drive, CD-ROM Drive (for the CD-ROM drive model), or Hard Disk Drive in the UltraBay	14	01F0–01F7 and 03F6–03F7	None	None

System Resources	IRQ	I/O Address (Hex)	Memory Address (Hex)	DMA Channel
PCMCIA Controller	None	03E0–03E1 (The PCMCIA Cartridge option in the UltraBay: 13E0–13E1 Docking station's PC Card slots: 03E2–03E3)	None	None
PC Card	(Depends on the type of PC Card)	(Depends on the type of PC Card)	(Depends on the type of PC Card)	None
Real Time Clock	8	0070–0071	None	None
TrackPoint III or Mouse	12	0060 and 0064	None	None
Math Coprocessor Exception	13	None	None	None
SCSI Controller in Dock I[1]	**11**, 3, 5, 10, 12, 14, or 15	None[2]	**CA000–CBFFF**, C8000–C9FFF, CE000–CFFFF, or DE000–DFFFF	None
SCSI Controller in Dock II[1]	**11**, 9, 10, or 12	**340–35F** or 140–14F	**DC000–DFFFF**, CC000–CFFFF, C8000–CBFFF, D0000–D3FFF, D4000–D7FFF, D8000–DBFFF, or disabled	None
SCSI Controller in SelectaDock Docking System	**11**, 3, 4, 5, 7, 9, 10, 15, or disabled	(Automatically set by the system)	None	None
IDE Hard Disk Drive or IDE CD-ROM Drive in the docking station	15	0170–0177 and 0376–0377	None	None
ISA adapter card (option card) in the docking station	(Refer to manual that came with the adapter card.)			

System Resources	IRQ	I/O Address (Hex)	Memory Address (Hex)	DMA Channel
PCI adapter card (option card) in the SelectaDock Docking System	**11**, 3, 4, 5, 7, 9, 10, 15, or disabled[1]	(Refer to manuals that came with the adapter card.)		
Note: [1] Select an IRQ and the memory addresses with the jumper and DIP switches on the system board of the Dock I or Dock II. See *Dock I User's Guide* or *Dock II User's Guide*. Do not select **Disabled** when OS/2 is used.	**Note:** [1] Enhanced Video features and PCI adapter card in the SelectaDock Docking System share the same IRQ11. [2] Sound Blaster and MIDI share the same IRQ.	**Note:** [1] Addresses in the parentheses are also used when ECP is enabled by the ThinkPad Features program as the printer operating mode. [2] Memory-mapped I/O	**Note:** [1] Memory upper than the system memory will be automatically set by the system.	**Note:** [1] When you enable ECP as the printer operating mode by ThinkPad Features program, one of the choices (including "disabled") must be selected.

Appendix B. System Management API (SMAPI) BIOS Overview

Overview

The ThinkPad Basic Input/Output System (BIOS) provides a special software interface, called the System Management Application Program Interface (SMAPI) BIOS, to control the following unique features of the ThinkPad system:

System Information
This BIOS provides unique ThinkPad information, such as the system identifier (system ID).

System Configuration
The ThinkPad SMAPI BIOS provides system configuration control for such features as display device selection or resource configuration for built-in devices.

Power Management
Through the SMAPI BIOS, the operating system or application software can control the ThinkPad power management features (the power mode or suspend/hibernation/resume options).

“Header Image” on page B-4 describes how to use the SMAPI BIOS.

Header Image

Systems that support SMAPI BIOS must provide the following header image in the F000 segment system ROM area at the 16-byte boundary. The client needs to search and find this SMAPI BIOS header image to get the entry point for the service.

Field	Offset (in Hex)	Length	Value
Signature	00	4 bytes	'$SMB' (ASCII)
Version (Major)	04	Byte	01h
Version (Minor)	05	Byte	00h
Length	06	Byte	20h
Checksum	07	Byte	–
Information Word	08	Word	–
Reserved 1	0A	Word	–
Real mode 16-bit offset to entry point	0C	Word	–
Real mode 16-bit code segment address	0E	Word	–
Reserved 2	10	Word	–
16-bit protected mode offset to entry point	12	Word	–
16-bit protected mode code segment base address	14	Double words	–
32-bit protected mode offset to entry point	18	Double words	–
32-bit protected mode code segment base address	1C	Double words	–

Signature ASCII Code '$SMB' is stored at the top of the header image.

Version (Major or Minor)
Indicates the SMAPI BIOS version.

Length The length of the header image.

Checksum Checksum byte area. The client verifies that this header image is valid by using this checksum; the client should check all header image bytes, and the result will be zero bytes.

Information Word

This area identifies the following BIOS service level:

```
Information Word
        Bit 0    : Real/V86 mode interface support
        Bit 1    : 16-bit protected mode support
        Bit 2    : 32-bit protected mode support
        Bit 3-15 : Reserved
```

Real Mode Entry Point

The entry point is specified in segment, offset format. Clients using Real/V86 mode can use this area for the far-call value.

16-bit or 32-bit Protected Mode Entry Point

The code base code address specifies the physical address for this BIOS, and the client must prepare the selector for this BIOS. The length should be 64KB.

Calling Convention

The client can invoke the SMAPI BIOS with a far-call to the entry point that is specified in the header file. All parameters for the BIOS and other results are stored in the client data area; the client needs to prepare an input parameter and output parameter area in its data area, and informs this area by pushing those pointers onto its stack before the far-calls.

The SMAPI BIOS uses the stack/data area directly with the selector when the BIOS is invoked. Therefore, the caller needs to define the same privilege level as the BIOS.

Parameter Structure

The memory allocation for the input/output field should be prepared by the caller. The input field specifies the function request to the SMAPI BIOS, and the BIOS fills in the return value to the output field.

Input Field

Field	Offset (in Hex)	Length
Major Function Number	00	Byte
Minor Function Number	01	Byte
Parameter 1	02	Word
Parameter 2	04	Word
Parameter 3	06	Word
Parameter 4	08	Double words
Parameter 5	0C	Double words

Output Field

Field	Offset (in Hex)	Length
Return Code	00	Byte
Auxiliary Return Code	01	Byte
Parameter 1	02	Word
Parameter 2	04	Word
Parameter 3	06	Word
Parameter 4	08	Double words
Parameter 5	0C	Double words

Sample in Assembler Language

```
;
; Input Parameter Structure
;
SMB_INPARM              STRUC
 @SMBIN_FUNC            DB      ?
 @SMBIN_SUB_FUNC        DB      ?
 @SMBIN_PARM_1          DW      ?
 @SMBIN_PARM_2          DW      ?
 @SMBIN_PARM_3          DW      ?
 @SMBIN_PARM_4          DD      ?
 @SMBIN_PARM_5          DD      ?
SMB_INPARM              ENDS


;
; Output Parameter Structure
;

SMB_OUTPARM             STRUC
 @SMBOUT_RC             DB      ?
 @SMBOUT_SUB_RC         DB      ?
 @SMBOUT_PARM_1         DW      ?
 @SMBOUT_PARM_2         DW      ?
 @SMBOUT_PARM_3         DW      ?
 @SMBOUT_PARM_4         DD      ?
 @SMBOUT_PARM_5         DD      ?
SMB_OUTPARM             ENDS
```

Sample in C Language

```
//
// Input Parameter Structure
//
typedef struct {
   BYTE     SMBIN_FUNC     ;
   BYTE     SMBIN_SUB_FUNC ;
   WORD     SMBIN_PARM_1   ;
   WORD     SMBIN_PARM_2   ;
   WORD     SMBIN_PARM_3   ;
   DWORD    SMBIN_PARM_4   ;
   DWORD    SMBIN_PARM_5   ;
} INPARM, *PINPARM ;


//
// Output Parameter Structure
//
typedef struct {
   BYTE     SMBOUT_RC      ;
   BYTE     SMBOUT_SUB_RC  ;
   WORD     SMBOUT_PARM_1  ;
   WORD     SMBOUT_PARM_2  ;
   WORD     SMBOUT_PARM_3  ;
   DWORD    SMBOUT_PARM_4  ;
   DWORD    SMBOUT_PARM_5  ;
} OUTPARM, *POUTPARM ;


typedef INPARM    far * FPINPARM ;
typedef OUTPARM   far * FPOUTPARM ;
```

Calling Convention Pseudo Code

The following describes the calling convention using pseudo code.

Assembler Language

```
InputParm       SMB_INPARM      < >
OutputParm      SMB_OUTPARM     < >

16-bit

        push    ds
        mov     ax, offset OutputParm
        push    ax
        push    ds
        mov     ax, offset InputParm
        push    ax
        call    dword ptr SmapiBios
        add     sp, 8


32-bit
        push    ds
        mov     eax, offset OutputParm
        push    eax
        push    ds
        mov     eax, offset InputParm
        push    eax
        call    fword ptr SmapiBios
        add     sp, 16
```

C Language

```
typedef WORD (far * SMB)(FPINPARM, FPOUTPARM) ;

SMB         SmapiBios ;
INPARM      InputParm ;
OUTPARM     OutputParm ;
WORD        RC ;

RC = SmapiBios(&InputParm, &OutputParm) ;
```

Return Codes

The following hexadecimal return codes are stored in both the AL (AX) register and the return code field of the output parameter:

00	No error
53	SMAPI function is not available
81	Invalid parameter
86	Function is not supported
90	System error
91	System is invalid
92	System is busy
A0	Device error (disk read error)
A1	Device is busy
A2	Device is not attached
A3	Device is disabled
A4	Request parameter is out of range
A5	Request parameter is not accepted

All other values are reserved.

Function Description

System Information Service

Get System Identification

Input Field

```
Major Function Number - 00
Minor Function Number - 00
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Return value format
                        = 00 - ASCII format
                        = 01 - Binary format
Parameter 1           - System ID
Parameter 2           - Country Code
Parameter 3           - System BIOS revision
Parameter 4           - (Bit 16-31) Reserved
                      - (Bit 0-15) System Management BIOS revision
Parameter 5           - (Bit 16-31) Reserved
                      - (Bit 0-15) SMAPI BIOS Interface revision
```

Get CPU Information

Input Field

```
Major Function Number - 00
Minor Function Number - 01
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - CPU ID
                        (Bit 15-8) Microprocessor type
                        (Bit 7-0) Microprocessor stepping level
                        = FFFFh : Unknown
Parameter 3           - Clock Information
                        (Bit 15-8) CPU clock (units: MHz)
                        = FFh : Unknown
                        (Bit 7-0) Internal clock (units: MHz)
                        = FFh : Unknown
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get Display Device Information

Input Field

```
Major Function Number - 00
Minor Function Number - 02
Parameter 1           - (Bit 8) LCD information
                        (Bit 9) External CRT information
                        (Bit 15-10) Reserved
                        (Bit 7-0) Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - (Bit 15-8)
                        Built-in display device (panel)
                        information 1
                        = 00 : Monochrome STN LCD
                        = 01 : Monochrome TFT LCD
                        = 02 : Color STN LCD
                        = 03 : Color TFT LCD
                        = FF : Unknown
                        (Bit 7-0)
                        Built-in display device (panel)
                        information 2
                        = 00 : 640x480
                        = 01 : 800x600
                        = 02 : 1024x768
                        = FF : Unknown
Parameter 2           - (Bit 15-8) External CRT monitor
                        information
                        = 00 : External CRT is not attached
                        = 10 : Color monitor
                        = 20 : Monochrome monitor
                        = FF : Unknown
                        (Bit 7-0) Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get Docking Station Information

Input Field

```
Major Function Number - 00
Minor Function Number - 03
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Docking station status
                         Bit 0 - Docking status
                         = 0 : Undock
                         = 1 : Dock
                         Bit 5-1 - Reserved
                         Bit 6 - Security key status
                         = 0 : Lock position
                         = 1 : Unlock position
                         Bit 7 - Bus status
                         = 0 : BUS isolated
                         = 1 : BUS connected
Parameter 1           - Docking station ID
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get UltraBay Information

Input Field

```
Major Function Number - 00
Minor Function Number - 04
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - (Bit 15-8) UltraBay device information
                        = 00 : FDD
                        = 01 : Serial device
                        = 02 : TV tuner
                        = 10 : IDE device
                        = 20 : PCMCIA adapter
                        = 30 : Battery
                        = 40 : AC adapter
                        = FE : No UltraBay
                        = FF : Unknown
                        (Bit 7-0) UltraBay device ID
                        = 00 : FDD
                        = 01 : Cellular
                        = 02 : TV tuner
                        = 10 : CD-ROM
                        = 11 : IDE-HDD
                        = FF : ID is not available
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get Slave Micro Control Unit Information

Input Field

```
Major Function Number - 00
Minor Function Number - 06
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Return value format
                        = 00 - ASCII format
                        = 01 - Binary format
Parameter 1           - Reserved
Parameter 2           - Slave controller Revision
                       (= 0FFFF) - Not valid
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get System Sensor Status

Input Field

```
Major Function Number - 00
Minor Function Number - 07
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Current Status
                        Bit 8 - LID Status
                             = 0 : Open
                             = 1 : Close
                        Bit 9 - Keyboard status
                             = 0 : Close
                             = 1 : Open
                        Bit 10- AC Adapter
                             = 0 : Not attached
                             = 1 : Attached
                        Bit 15-11 : Reserved
                        (Bit 7-0) Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get Video Information

Input Field

```
Major Function Number - 00
Minor Function Number - 08
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Video BIOS revision
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get Refresh Rate Capability

Input Field

```
Major Function Number - 00
Minor Function Number - 09
Parameter 1           - mode
                        = 00xxh - VGA modes
                        (Bit 0-7 is ignored)
                        = 0100 - 640x400x256
                        = 0101 - 640x480x256
                        = 0110 - 640x480x32K
                        = 0111 - 640x480x64K
                        = 0112 - 640x480x16M
                        = 0102 - 800x600x16
                        = 0103 - 800x600x256
                        = 0113 - 800x600x32K
                        = 0114 - 800x600x64K
                        = 0104 - 1024x768x16
                        = 0105 - 1024x768x256
                        = 0106 - 1280x1024x16
                        = 0109 - 1056x350x16
                        = 010A - 1056x473x16
                        = 010C - 1056x480x16
                        = Others : Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Refresh rate capability for
                        specified mode:
                        Bit 0 - 60Hz available
                        Bit 1 - 72Hz available
                        Bit 2 - 75Hz available
                        Bit 3 - 43Hz(I) available
                        Bit 4 - 56Hz available
                        Bit 5 - 70Hz available
                        Bit 6-15 : Reserved (must be B'0')
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

System Configuration Service

Get Display Device State

Input Field

```
Major Function Number - 10
Minor Function Number - 00
Parameter 1           - Request type
                        = 0000h : Current hardware
                        = 0001h : CMOS
                                  (effective after reboot)
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - (Bit 15-8) Reserved
                        Bit 7-0 : Capability of display device function
                        Bit 0 - Display function type
                              = 0 : Not support
                              = 1 : Support
                        Bit 7-1 : Reserved
Parameter 2           - (Bit 15-8) Display current status
                        Bit 0 - Built-in display (panel) status
                              = 0 : Disable
                              = 1 : Enable
                        Bit 1 - External CRT status
                              = 0 : Disable
                              = 1 : Enable
                        Bit 2 - TV status
                              = 0 : Disable
                              = 1 : Enable
                        Bit 6-3 : Reserved
                        Bit 7 - Dual enable flag
                              = 0 : Disable
                              = 1 : Enable
                        (Bit 7-0) : Display function type
                              = 00h : No TV-out model
                              = 01h : Not support model for simultaneous
                                      display of TV and CRT
Parameter 3           - Reserved
Parameter 4           - When parameter 2 (bit 7-0) is 01h:
                        (Bit 31-16) : Reserved
                        (Bit 15-0) : Display selection mode
                        Bit 0 - Display selection mode
                              = 0 : LCD - CRT selection mode
                              = 1 : LCD - TV selection mode
                        (Bit 7-1) : Reserved
Parameter 5           - Reserved
```

Set Display Device State

Input Field

```
Major Function Number - 10
Minor Function Number - 01
Parameter 1           - Request display status
                        Bit 0 - Built-in display (panel) status
                              = 0 : Disable
                              = 1 : Enable
                        Bit 1 - External CRT status
                              = 0 : Disable
                              = 1 : Enable
                        Bit 2 - TV status
                              = 0 : Disable
                              = 1 : Enable
                        Bit 5-3 : Reserved
                        Bit 6 - Monitor detection ignore
                              = 0 : Do not ignore
                              = 1 : Ignore
                        Bit 7 - Dual enable flag
                              = 0 : Disable
                              = 1 : Enable
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - When parameter 2 (bit 7-0) is 01h in return
                        of "Get Display Device State":
                        (Bit 31-16) : Reserved
                        (Bit 15-0) : Display selection mode
                        Bit 0 - Display selection mode
                              = 0 : LCD - CRT selection mode
                              = 1 : LCD - TV selection mode
                        Bit 7-1 : Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get Pointing Device State

Input Field

```
Major Function Number - 11
Minor Function Number - 02
Parameter 1           - (Bit 15-8) Request type
                           = 00h - Current hardware
                           = 01h - CMOS (effective after reboot)
                        (Bit 7-0) Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - (Bit 15-8) Pointing device current status
                        Bit 8 - Built-in pointing device status
                           = 0 : Disable
                           = 1 : Enable
                        Bit 9 - External pointing device status
                           = 0 : Disable
                           = 1 : Enable
                        Bit 15-10: Reserved
                        (Bit 7-0) Pointing device capability
                        Bit 0 - Built-in pointing device status
                           = 0 : Status is not controllable
                           = 1 : Status is controllable
                        Bit 1 - External pointing device status
                           = 0 : Status is not controllable
                           = 1 : Status is controllable
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Set Pointing Device State

Input Field

```
Major Function Number - 11
Minor Function Number - 03
Parameter 1           - Reserved
Parameter 2           - (Bit 15-8)
                        Pointing device current status
                        Bit 8 - Built-in pointing device status
                           = 0 : Disable
                           = 1 : Enable
                        Bit 9 - External pointing device status
                           = 0 : Disable
                           = 1 : Enable
                        Bit 15-10: Reserved
                        (Bit 7-0) Request type
                           = 00h - Current hardware
                           = 01h - CMOS (effective after reboot)
                        Bit 7-2: Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
                        Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get Hotkey Sticky/Lock

Input Field

```
Major Function Number - 13
Minor Function Number - 02
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - (Bit 15-8) Capability
                         Bit 9-8 - Fn Key Lock
                        (Bit 9, bit 8) =
                          (0, 0) - Not supported
                          (0, 1) - Sticky Fn key support
                          (1, 1) - Sticky and
                                   Lock Fn key support
                          (1, 0) - Reserved
                         Bit 15-10 - Reserved
                        (Bit 7-0) Current status
                         Bit 1-0 - Fn key lock
                        (Bit 1, bit 0) =
                          (0, 0) - Disable
                          (0, 1) - Enable sticky
                                   Fn key support
                          (1, 1) - Enable sticky and
                                   Lock Fn key support
                          (1, 0) - Reserved
                         Bit 7-2 - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Set Hotkey Sticky/Lock

Input Field

```
Major Function Number - 13
Minor Function Number - 03
Parameter            - (Bit 15-8) Reserved
                       (Bit 7-0) Request Status
                        Bit 1-0 - Sticky/lock Fn
                                  key support
                       (Bit 1, bit 0) =
                         (0, 0) - Disable
                         (0, 1) - Enable sticky
                                  Fn key support
                         (1, 1) - Enable sticky and
                                  Lock Fn key support
                         (1, 0) - Reserved
                        Bit 7-2 - Reserved
Parameter 2          - Reserved
Parameter 3          - Reserved
Parameter 4          - Reserved
Parameter 5          - Reserved
```

Output Field

```
Return Code          - Error status
Auxiliary Return Code - Reserved
Parameter 1          - Reserved
Parameter 2          - Reserved
Parameter 3          - Reserved
Parameter 4          - Reserved
Parameter 5          - Reserved
```

Power Management Service

Get Power Management Mode

Input Field

```
Major Function Number - 22
Minor Function Number - 00
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - (Bit 15-8) Power management mode
                             Battery operation
                             = 00h - High performance mode
                             = 01h - Auto power management mode
                             = 02h - Manual power management mode
                        (Bit  7- 0) Power management mode
                             AC operation
                             = 00h - High performance mode
                             = 01h - Auto power management mode
                             = 02h - Manual power management mode
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Set Power Management Mode

Input Field

```
Major Function Number - 22
Minor Function Number - 01
Parameter 1           - (Bit 15-8) Power management mode
                             Battery operation
                             = 00h - High performance mode
                             = 01h - Auto power management mode
                             = 02h - Manual power management mode
                        (Bit 7-0) Power management mode
                             AC operation
                             = 00h - High performance mode
                             = 01h - Auto power management mode
                             = 02h - Manual power management mode
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
                        Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get Timer Control

Input Field

```
Major Function Number - 22
Minor Function Number - 02
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - (Bit 15-8) Capability of timer control
                        Bit 8 - System
                        (Hibernation/suspend) timer
                                = 0 : Disable
                                = 1 : Enable
                        Bit 9 - Standby timer
                                = 0 : Disable
                                = 1 : Enable
                        Bit 10 - LCD off timer
                                = 0 : Disable
                                = 1 : Enable
                        Bit 11 - HDD off timer
                                = 0 : Disable
                                = 1 : Enable
                        Bit 15-12 - Reserved
                        (Bit 7-0) Timer control
                            Bit 0 - System (Hibernation/suspend)
                                    timer
                                      = 0 : Disable
                                      = 1 : Enable
                            Bit 1 - Standby timer
                                      = 0 : Disable
                                      = 1 : Enable
                            Bit 2 - LCD off timer
                                      = 0 : Disable
                                      = 1 : Enable
                            Bit 3 - HDD off timer
                                      = 0 : Disable
                                      = 1 : Enable
                            Bit 7-4 - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Set Timer Control

Input Field

```
Major Function Number - 22
Minor Function Number - 03
Parameter 1           - (Bit 15-8) Reserved
                        (Bit 7-0) Timer control
                         Bit 0 - System
                             (Hibernation/suspend) timer
                                     = 0 : Disable
                                     = 1 : Enable
                         Bit 1 - Standby timer
                                     = 0 : Disable
                                     = 1 : Enable
                         Bit 2 - LCD off timer
                                     = 0 : Disable
                                     = 1 : Enable
                         Bit 3 - HDD off timer
                                     = 0 : Disable
                                     = 1 : Enable
                         Bit 7-4 - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
                        Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Event Bit Definition

```
Bit 2-0 - Reserved
Bit 3   - Standby
Bit 4   - Suspend
Bit 5   - RediSafe
Bit 6   - Hibernation
Bit 7   - Power off
```

Note: If bits are duplicated, the highest bit is available.

Get System Event Global Condition

Input Field

```
Major Function Number - 30
Minor Function Number - 00
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - (Bit 15-8) Capability for event
                              Bit 8 - RediSafe is
                              controlled by global conditions.
                              (RediSafe bit is ignored
                              in each event condition.)
                               = 0 - Disable
                               = 1 - Enable
                        (Bit 7-0) Global event condition
                              Bit 0 - Enable RediSafe
                              if suspend is selected.
                               = 0 - Disable
                               = 1 - Enable
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Set System Event Global Condition

Input Field

```
Major Function Number - 30
Minor Function Number - 01
Parameter 1           - (Bit 15-8) Reserved
                        (Bit 7-0) Global condition for event
                         Bit 0 - Enable safe suspend if suspend
                         is selected.
                          = 0 - Disable
                          = 1 - Enable
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
                        Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get System Event 1 Condition

Input Field

```
Major Function Number - 31
Minor Function Number - 00
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Hardware and software
                        event definition
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0 - Condition
                        (see page B-33)
Parameter 3           - Reserved
Parameter 4           - (Bit 31-16) Reserved
                        (Bit 15-0) Power switch detection
                                   event definition
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0 - Condition
                        (See page B-33)
Parameter 5           - (Bit 31-16) Reserved
                        (Bit 15-0) LID close detection
                                   event definition
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0 - Condition
                        (see page B-33)
```

Set System Event 1 Condition

Input Field

```
Major Function Number - 31
Minor Function Number - 01
Parameter 1           - Condition for hardware and software event
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0 - Condition
                        (see page B-33)
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - (Bit 31-16) Reserved
                        (Bit 15-0) Condition for power
                                   switch detection
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0 - Condition
                        (see page B-33)
Parameter 5           - (Bit 31-16) Reserved
                        (Bit 15-0) Condition for
                                   LID close detection
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0 - Condition
                        (see page B-33)
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get System Event 2 Condition

Input Field

```
Major Function Number - 32
Minor Function Number - 00
Parameter 1           - System timer expiry
                        event definition
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0 - Condition
                        (see page B-33)
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - (Bit 31-16) Reserved
                        (Bit 15-0) Standby timer expiry
                                    event definition
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0 - Condition
                        (see page B-33)
Parameter 5           - (Bit 31-16) Reserved
                        (Bit 15-0)
                         Hibernation timer during suspend
                         mode expiry event definition.
                         Bit 15-8 - Capability
                         (see page B-33)
                         Bit 7-0 - Condition
                         (see page B-33)
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Set System Event 2 Condition

Input Field

```
Major Function Number - 32
Minor Function Number - 01
Parameter 1           - Condition for system timer expiry
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0  - Condition
                        (see page B-33)
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - (Bit 31-16) Reserved
                        (Bit 15-0) Condition for standby
                                   timer expired
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0 - Condition
                        (see page B-33)
Parameter 5           - (Bit 31-16) Reserved
                        (Bit 15-0) Condition for hibernation
                        timer during suspend mode expired
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0 - Condition
                        (see page B-33)
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get System Timer

Input Field

```
Major Function Number - 32
Minor Function Number - 02
Parameter 1           - (Bit 15-8) Power mode select
                          = 00h - Reserved
                          = 01h - Manual PM mode (AC)
                          = 02h - Manual PM mode (battery)
                          = F3h - High performance mode
                          = F4h - Auto pwr mgmt mode
                        (Bit 7-0) Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - (Bit 15-8) System timer capability
                        Bit 8 = 0 - Timer cannot be specified
                                in each power mode
                                = 1 - Timer can be specified
                                in each Power mode
                         Bit 15-9 - Reserved
                        (Bit  7- 0) Reserved
Parameter 2           - (Bit 15- 8) Reserved
                        (Bit  7- 0) System timer initial value
                        (units: minutes)
                               = 00h - Disable system timer
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Set System Timer

Input Field

```
Major Function Number - 32
Minor Function Number - 03
Parameter 1           - (Bit 15-8) Power mode select
                               = 00h - All mode
                               = 01h - Manual PM mode (AC)
                               = 02h - Manual PM mode (battery)
                               = F3h - High performance mode
                               = F4h - Auto pwr mgmt mode
                        (Bit 7-0) System timer initial
                               value (units: minutes)
                               = 00h - Disable system timer
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
                        Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get Standby Timer

Input Field

```
Major Function Number - 32
Minor Function Number - 04
Parameter 1           - (Bit 15-8) Power mode select
                         = 00h - Reserved
                         = 01h - Manual PM mode (AC)
                         = 02h - Manual PM mode (battery)
                         = F3h - High performance mode
                         = F4h - Auto pwr mgmt mode
                        (Bit 7-0) Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - (Bit 15- 8) Standby timer capability
                         Bit 8 = 0 - Timer cannot be specified
                                in each power mode
                                = 1 - Timer can be specified
                                in each power mode
                                 Bit 15-9 - Reserved
                                (Bit 7-0) Reserved
Parameter 2           - (Bit 15-8) Reserved
                        (Bit 7-0) Standby timer initial
                        value (units: minutes)
                             = 00h - Disable standby timer
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Set Standby Timer

Input Field

```
Major Function Number - 32
Minor Function Number - 05
Parameter 1           - (Bit 15-8) Power mode select
                          = 00h - All mode
                          = 01h - Manual PM mode (AC)
                          = 02h - Manual PM mode (battery)
                          = F3h - High performance mode
                          = F4h - Auto pwr mgmt mode
                          (Bit  7- 0) Standby timer initial value
                          (units: minutes)
                          = 00h - Disable standby timer
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
                        Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get Hibernation Timer

Input Field

```
Major Function Number - 32
Minor Function Number - 06
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - (Bit 15-8) Reserved
                        (Bit 7-0) Hibernation timer during
                                  suspend mode initial value
                                  (units: minutes)
                          = 00h - Disable hibernation timer
                                  during suspend mode
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Set Hibernation Timer

Input Field

```
Major Function Number - 32
Minor Function Number - 07
Parameter 1           - (Bit 15-8) Reserved
                        (Bit 7-0) Hibernation timer during
                                  suspend mode initial value
                                  (units: minutes)
                         = 00h - Disable hibernation timer
                                 during suspend mode
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
                        Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get System Event 3 Condition

Input Field

```
Major Function Number - 33
Minor Function Number - 00
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Critical low battery condition
                               detection event definition
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0  - Condition
                        (see page B-33)
Parameter 3           - Reserved
Parameter 4           - (Bit 16-31) Reserved
                        (Bit 0-15) Out-of-environment condition
                        detection event definition
                        Bit 15-8 - Capability
                        (see page B-33)
                        Bit 7-0  - Condition
                        (see page B-33)
Parameter 5           - Reserved
```

Set System Event 3 Condition

Input Field

```
Major Function Number - 33
Minor Function Number - 01
Parameter 1           - (Bit 15-8) Reserved
                        (Bit 7-0) Condition for critical
                        low battery condition detection
                        Bit 7-0 - Condition
                        (see page B-33)
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - (Bit 31-8) Reserved
                        (Bit 7-0) Condition for out-of-environment
                        condition detection
                        Bit 7-0 - Condition
                        (see page B-33)
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
                        Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get System Resume Condition

Input Field

```
Major Function Number - 34
Minor Function Number - 00
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Condition for resuming trigger
                        from system suspend mode
                        Bit 0 - Resume switch by hardware
                        Bit 1 - LID open detection
                        Bit 2 - RTC alarm (resume timer)
                                detection
                        Bit 3 - RI from the serial device
                                detection
                        Bit 15-4 - Reserved
Parameter 3           - Capability for resuming trigger from
                        the system suspend mode
                        Bit 0 - Resume switch by hardware
                        Bit 1 - LID open detection
                        Bit 2 - RTC alarm (resume timer)
                                detection
                        Bit 3 - RI from the Serial Device
                                detection
                        Bit 15-4 - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Set System Resume Condition

Input Field

```
Major Function Number - 34
Minor Function Number - 01
Parameter 1           - Condition for resuming trigger
                        from the system suspend mode
                        Bit 0 - Resume switch by hardware
                        Bit 1 - LID open detection
                        Bit 2 - RTC alarm (resume timer)
                                detection
                        Bit 3 - RI from the serial device
                                detection
                        Bit 15-4 - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Get System Resume Timer

Input Field

```
Major Function Number - 34
Minor Function Number - 02
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - TOD of resume timer (BCD format)
                        Bit 7-0  - Seconds    (0-59)
                        Bit 15-8  - Minutes   (0-59)
                        Bit 23-16 - Hours     (0-23)
                        Bit 31-24 - Reserved
Parameter 5           - Date of resume timer (BCD format)
                        Bit 7-0  - Day        (1-31)
                        Bit 15-8  - Month     (1-12)
                        Bit 23-16 - Year      (0-99)
                        Bit 30-24 - Reserved
                        Bit 31    - Resume date validation
                                  = 0 - Valid (specified day)
                                  = 1 - Invalid (every day)
```

Set System Resume Timer

Input Field

```
Major Function Number - 34
Minor Function Number - 03
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - TOD of resume timer (BCD format)
                        Bit 7-0  - Seconds    (0-59)
                        Bit 15-8  - Minutes   (0-59)
                        Bit 23-16 - Hours     (0-23)
                        Bit 31-24 - Reserved
Parameter 5           - Date of resume timer (BCD format)
                        Bit 7-0  - Day        (1-31)
                        Bit 15-8  - Month     (1-12)
                        Bit 23-16 - Year      (0-99)
                        Bit 30-24 - Reserved
                        Bit 31    - Resume date validation
                                  = 0 - Valid (specified day)
                                  = 1 - Invalid (every day)
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Request System Standby

Input Field

```
Major Function Number - 70
Minor Function Number - 00
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Request System Suspend

Input Field

```
Major Function Number - 70
Minor Function Number - 01
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Request System Hibernation

Input Field

```
Major Function Number - 70
Minor Function Number - 02
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Request System Off

Input Field

```
Major Function Number - 70
Minor Function Number - 03
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Output Field

```
Return Code           - Error status
Auxiliary Return Code - Reserved
Parameter 1           - Reserved
Parameter 2           - Reserved
Parameter 3           - Reserved
Parameter 4           - Reserved
Parameter 5           - Reserved
```

Samples

Data Structure

Assembler Language

```
;
;  Smapi BIOS Header
;
SMB_HEADER              STRUC
 @SMBHDR_SIG           DB   4 dup (?) ; +00 - Signature
 @SMBHDR_VER           DB   ?         ; +04 - Major version
 @SMBHDR_VER_VER       DB   ?         ; +05 - Minor version
 @SMBHDR_LEN           DB   ?         ; +06 - Length
 @SMBHDR_CHKSUM        DB   ?         ; +07 - Checksum
 @SMBHDR_INFO          DW   ?         ; +08 - Information word
 @SMBHDR_RSV1          DW   ?         ; +0A - Reserve 1
 @SMBHDR_R_OFFSET      DW   ?         ; +0C - Real mode offset
 @SMBHDR_R_SEGMENT     DW   ?         ; +0E - Real mode segment
 @SMBHDR_RSV2          DW   ?         ; +10 - Reserve 2
 @SMBHDR_P16_OFFSET    DW   ?         ; +12 - 16-bit protected mode offset
 @SMBHDR_P16_BASE      DD   ?         ; +14 - 16-bit protected mode base address
 @SMBHDR_P32_OFFSET    DD   ?         ; +18 - 32-bit protected mode offset
 @SMBHDR_P32_BASET     DD   ?         ; +1C - 32-bit protected mode base address
SMB_HEADER             ENDS
```

Parameters

```
;
;Input Parameter
;
SMB_INPARM                STRUC
 @SMBIN_FUNC              DB      ?
 @SMBIN_SUB_FUNC          DB      ?
 @SMBIN_PARM_1            DW      ?
 @SMBIN_PARM_2            DW      ?
 @SMBIN_PARM_3            DW      ?
 @SMBIN_PARM_4            DD      ?
 @SMBIN_PARM_5            DD      ?
SMB_INPARM                ENDS


;
;Output Parameter
;
SMB_OUTPARM               STRUC
 @SMBOUT_RC               DB      ?
 @SMBOUT_SUB_RC           DB      ?
 @SMBOUT_PARM_1           DW      ?
 @SMBOUT_PARM_2           DW      ?
 @SMBOUT_PARM_3           DW      ?
 @SMBOUT_PARM_4           DD      ?
 @SMBOUT_PARM_5           DD      ?
SMB_OUTPARM               ENDS
```

C Language

```
//
//  SMAPI BIOS Header
//
typedef struct {
   BYTE     SMBHDR_SIG]4[       ; // Signature
   BYTE     SMBHDR_VER          ; // Major version
   BYTE     SMBHDR_VER_VER      ; // Minor version
   BYTE     SMBHDR_LEN          ; // Length
   BYTE     SMBHDR_CHKSUM       ; // Checksum
   WORD     SMBHDR_INFO         ; // Information word
   WORD     SMBHDR_RSV1         ; // Reserve 1
   WORD     SMBHDR_R_OFFSET     ; // Real mode offset
   WORD     SMBHDR_R_SEGMENT    ; // Real mode segment
   WORD     SMBHDR_RSV2         ; // Reserve 2
   WORD     SMBHDR_P16_OFFSET   ; // 16-bit Protect mode offset
   DWORD    SMBHDR_P16_BASE     ; // 16-bit Protect mode base address
   DWORD    SMBHDR_P32_OFFSET   ; // 32-bit Protect mode offset
   DWORD    SMBHDR_P32_BASE     ; // 32-bit Protect mode base address
} SMB_HEADER, *PSMB_HEADER ;
```

Parameters

```
//
// Input Parameter
//
typedef struct {
   BYTE     SMBIN_FUNC       ;
   BYTE     SMBIN_SUB_FUNC   ;
   WORD     SMBIN_PARM_1     ;
   WORD     SMBIN_PARM_2     ;
   WORD     SMBIN_PARM_3     ;
   DWORD    SMBIN_PARM_4     ;
   DWORD    SMBIN_PARM_5     ;
} INPARM, *PINPARM ;

//
// Output Parameter
//
typedef struct {
   BYTE     SMBOUT_RC        ;
   BYTE     SMBOUT_SUB_RC    ;
   WORD     SMBOUT_PARM_1    ;
   WORD     SMBOUT_PARM_2    ;
   WORD     SMBOUT_PARM_3    ;
   DWORD    SMBOUT_PARM_4    ;
   DWORD    SMBOUT_PARM_5    ;
} OUTPARM, *POUTPARM ;

typedef INPARM  far * FPINPARM;
typedef OUTPARM far * FPOUTPARM;
```

Function Declaration

C Language

```
//
// Smapi BIOS function
//
typedef WORD (far * SMB)(FPINPARM, FPOUTPARM) ;
```

Installation Check

Assembler Language: Real Mode

```
;
;  FindSmapi
; -----------
;
;   On Entry : None
;   On Exit    : CF = 0 .. Find out
;                   DX - Segment
;                   BX - Pointer to header
;
;                CF = 1 .. No Smapi BIOS
;

FindSmapi         Proc    Near

        push      eax
        push      cx
        push      si
        push      ds

        mov       ax, BIOS_SEG      ; F000 Segment
        mov       ds, ax
        mov       bx, 0             ; Start point
        mov       cx, SMB_CAND_CNT  ; Total check count
        mov       eax, 'BMS$'  ; Target strings

  @@:
        cmp       eax, dword ptr ds:[bx].@SMBHDR_SIG
        je        short @f
        add       bx, 10h      ; Next paragraph
        loop      @b
        stc
        jmp       short FindSmapiFin
```

```
   @@:  ;         Find Smapi Head
        mov       dx, BIOS_SEG

        ;         Calculate Checksum.. next.
        pushf                ; Save direction flag
        cld                  ; Clear it
        mov       si, bx
        xor       ax, ax
        movzx     cx,byte ptr ds:[bx].@SMBHDR_LEN
   @@:
        lodsb
        add       ah, al
        loop      @b

        popf                 ; Restore Direction flags
        cmp       ah, 1      ; Checksum is OK?
        cmc

FindSmapiFin:
        pop       ds
        pop       si
        pop       cx
        pop       eax
        ret

FindSmapi         Endp
```

C Language

```
        typedef struct {
           BYTE     SMBHDR_SIG[4]         ; // Signature
           BYTE     SMBHDR_VER              ; // Major version
           BYTE     SMBHDR_VER_VER          ; // Minor version
           BYTE     SMBHDR_LEN              ; // Length
           BYTE     SMBHDR_CHKSUM           ; // Checksum
           WORD     SMBHDR_INFO             ; // Information word
           WORD     SMBHDR_RSV1             ; // Reserve 1
           WORD     SMBHDR_R_OFFSET         ; // Real mode offset
           WORD     SMBHDR_R_SEGMENT        ; // Real mode segment
        } SMB_HEADER_REAL, far * PFSMB_HEADER_REAL ;

BOOLEAN GetSmapiEntry(PSMB pFunc)
{
   PFSMB_HEADER_REAL        MyPtr = 0xF0000000 ;
   WORD                     cnt = 0 ;
   BYTE                     cksum = 0 ;

   //
   // 1) Search for signature first
   //
   while((cnt++ < 0x1000) &&
         !(((MyPtr->SMBHDR_SIG)[0] == '$') &&
            ((MyPtr->SMBHDR_SIG)[1] == 'S') &&
            ((MyPtr->SMBHDR_SIG)[2] == 'M') &&
            ((MyPtr->SMBHDR_SIG)[3] == 'B') )) {
      MyPtr++ ;
   }


   //
   //  2) Find the Signature?
   //
   if (cnt >= 0x1000) {
      // We cannot find it.
      return FALSE ;
      } else {
      //
      //  3) Calculate Checksum
      //
      for (cnt = 0 ; cnt < MyPtr->SMBHDR_LEN ; cnt++)
         cksum += (BYTE)((MyPtr->SMBHDR_SIG)[cnt]) ;

      if (cksum) {
         // Bad Checksum
         return FALSE ;
      } else {
         // Build Return Address
         (*pFunc) = ( (DWORD)(MyPtr->SMBHDR_R_OFFSET) +
                (((DWORD)(MyPtr->SMBHDR_R_SEGMENT)) << 16) ) ;
         return TRUE ;
      }
   }
}
```

BIOS Call

Assembler Language: 16-Bit Protected Mode

```
;
; Build Input Parameter Field
;

mov       al, SMB_GET_SYSID
mov       [bx].@Func, al

push      ds
mov       ax, offset OutputParm
push      ax
push      ds

mov       ax, offset InputParm
push      ax
call      _SmapiBios
add       sp, 8

;
; Get information from Output Parm
;
or        ax, ax
jnz       Error

mov       bx, offset OutputParm
mov       al, [bx].@Parm1
```

32-Bit Protected Mode

```
;
; Build Input Parameter Field
;
mov       ebx, offset InputParm
mov       al, SMB_GET_SYSID
mov       [ebx].@Func, al

push      ds
mov       eax, offset OutputParm
push      eax
push      ds
mov       eax, offset InputParm
push      eax
call      _SmapiBios
add       sp, 16

;
; Get information from Output Parm
;
or        ax, ax
jnz       Error

mov       ebx, offset OutputParm
mov       ax, [ebx].@Parm1
```

C Language

```
WORD  GetSystemID()
{
   SMB         SmapiEntry ;
   INPARM      MyInput ;
   OUTPARM     MyOutput ;
   WORD        Rc = -1 ;

   if (GetSmapiEntry(&SmapiEntry)) {

      MyInput.SMBIN_FUNC        = 0 ;
      MyInput.SMBIN_SUB_FUNC    = 0 ;

      if (SmapiEntry(&MyInput, &MyOutput)) {
        // No System ID is available
      } else {
        Rc = MyOutput.SMBOUT_PARM_1 ;
      }

   } else {
      // No Smapi BIOS interface.
      // Try to use CBIOS INT 15.
   }
   return Rc ;
}
```

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Index

S

T

V

W

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