Headland
Technology Inc

GCK181
Universal PS/2 Chip Set

FEATURES

- Universal Micro Channel Compatible chip set supporting the Intel 80286, 386SX and 80386 to 25 MHz
- Designed in 0.9 Micron channel length HCMOS and BiCMOS in Surface Mount Packages
- Manages up to 8 MB of Paged/Interleaved Memory on a Private Memory Bus for faster access
- Delivers zero wait state Page Mode Memory performance at 20MHz with 80ns DRAMs
- Supports 4Megabit, 1Megabit, & 256k DRAMs
- Supports Shadow RAM BIOS
- Allows Asynchronous DMA
- Conforms to the full Micro Channel specification including Matched Memory Cycles at 20MHz
- Includes 8 DMA Channels with Auto-initialization and Extended Addressing Mode
- Integrates parallel port and NPU interface logic
- High Performance VGA Compatible Graphics with the GC205

DESCRIPTION

The GCK181 product family provides a universal engineering platform for PS/2 compatible systems using the Intel 80286, 80386, and 80386SX microprocessors. This chip set introduces the most highly integrated solution for manufacturing high performance PS/2 compatible computer systems.

The GC181 CPU/Bus Controller initiates and controls all bus cycles. It controls the interface to the Micro Channel, address and data buffers, CPU, DMA and Memory Controllers. Full Micro Channel support is provided including Matched Memory Cycles and all timing requirements. This device also integrates reset control and clock generation logic. It is packaged in a 68 pin PLCC.

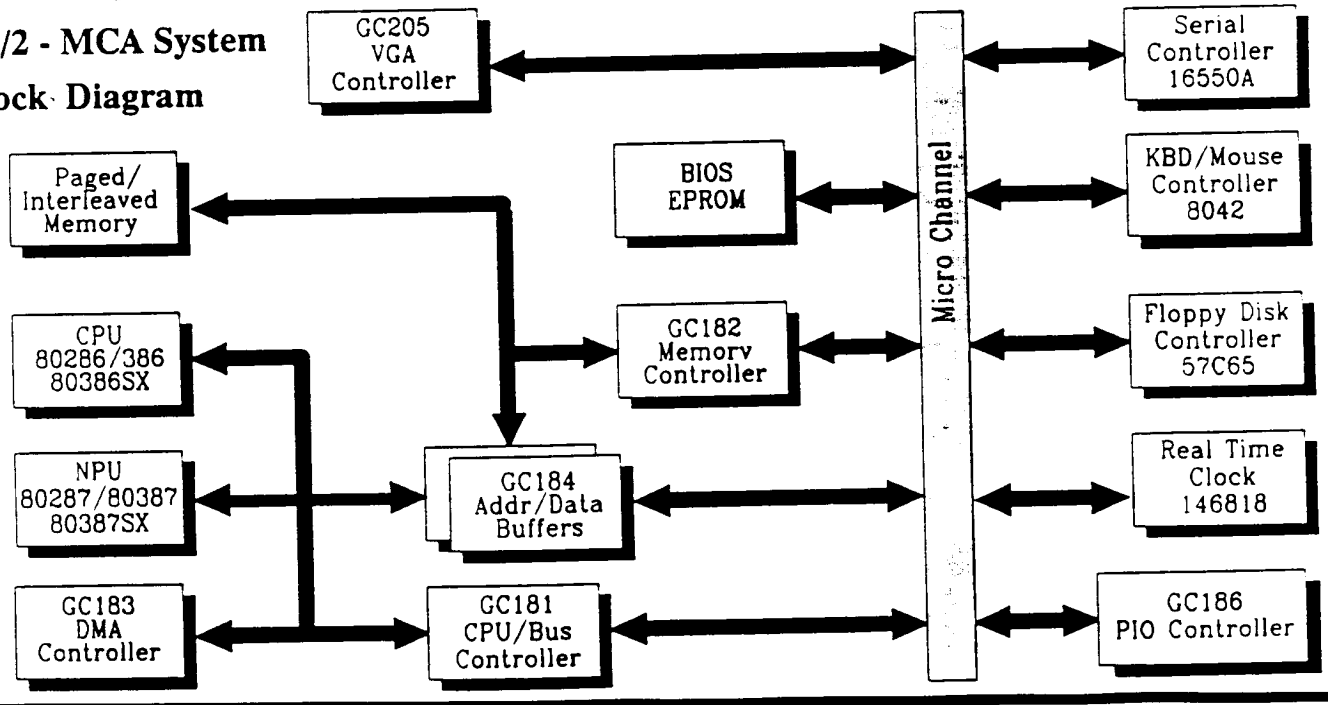
The GC182 Memory Controller interfaces the CPU and Micro Channel to System DRAM. Four DRAM chip sizes are supported: 1Mx1, 1Mx4, 256Kx1, 256Kx4. These can be configured to 8 MBytes of interleaved/paged memory. Four memory modes are selectable to meet IBM Model 50/60/70/80 memory requirements. Zero wait state page mode is achievable at 20 MHz with 80ns DRAMs. Package type is 120 pin PQFP (plastic quad flat pack).

The GC183 DMA Controller provides 8 DMA channels, supporting 24 address bits and 8 or 16 bit data transfers. This device provides the Micro Channel with 15 levels of bus arbitration and support for multiple bus masters. It also contains DRAM refresh logic and NPU support logic. Package type is 160 pin PQFP.

The GC184 Address/Data Buffer integrates approximately 44 TTL packages otherwise required in a PS/2 system. It is packaged in a 160 pin PQFP.

The GC186 Peripheral Controller interfaces peripherals with the Micro Channel. It supports 15 interrupt channels, the refresh rate counter, and three programmable timers. It also contains PS/2 POS Registers, a PS/2 and AT compatible parallel port, address decodes for serial ports, floppy disk, keyboard, real time clock and CMOS RAM. Package type is 160 pin PQFP.

PS/2 - MCA System Block Diagram



Preliminary

FEATURES

- 68 Pin Package
- Generates all bus cycles for the system
- Operation at 16, 20 and 25 MHz
- Supports 80286, 80386SX and 80386 processors

OVERVIEW

The Bus / CPU Controller integrates many system functions into one VLSI component. Even though the Controller is only 68 pins, it controls the interface between the following system sections: CPU, DMA, address and data buffers, Memory Controller, and the Micro Channel. In addition, it generates the system clocks and internal reset signals. The resulting advantage for the microcomputer system is very efficient use of logic partitioning which reduces the number of total system components devices that would otherwise be necessary. Furthermore, the system operates faster because of tighter logic integration.

The system implementation provides for a special "private" data bus, generates special control signals that allow faster read access to main, "private", on-board memory than is possible with the IBM PS/2 computer. The Bus Controller also permits system use of both 8 and 16 bit Micro Channel devices and generates all wait state and READY control signals to interface different size and speed devices to the CPU. Built in buffers allow direct support of Micro Channel electrical specifications. Finally, built in test circuitry enhances the fabrication of the Controller and simultaneously allows easier integration into systems built around this part.

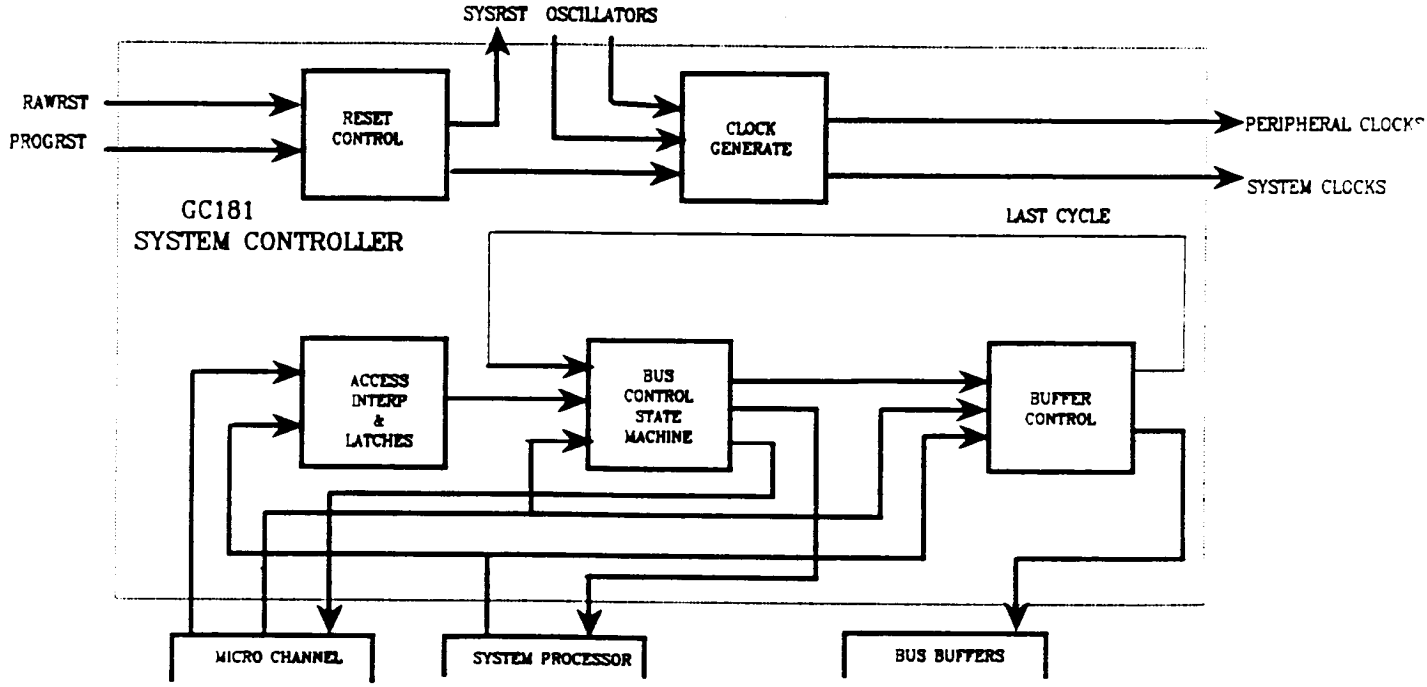


Figure 1.1 GC181 Block Diagram

FUNCTIONAL DESCRIPTION

The Bus / CPU Controller performs the bus control function for a multiprocessor desktop microcomputer. The functional blocks of the chip are illustrated in Figure 1.1.

RESET CONTROL

The RESET CONTROL block takes resets from two different sources and generates the appropriately conditioned resets for use throughout the system. The RAWRST input is from the power on reset or a physical reset switch on the computer system. The resultant system reset signal begins following the trailing edge of the RAWRESET input and will be a minimum of 16 cycles of the system clock in duration. The other sources of resets within the system are the KILL signal, a programmed reset and a keyboard reset. These resets generate a reset to the system processor only. The remainder of the system is not reset. The KILL signal is generated by multiple exception conditions occuring. It is a special decoded bus sequence identified as SHUTDOWN in the processor specification. The programmed reset is the result of writing to a bit in one of the I/O ports defined for a PS/2 system and physically contained within the GC186 PIO chip. The keyboard reset is typically generated through a CTL, ALT, DELETE key sequence and is issued by the 8042 keyboard controller. The KILL signal is generated from the GC181 and routed through the DMA part along with the other two processor-only resets to assure that they are synchronized with a cycle boundary to prevent loss of data through prematurely terminated cycles. A block diagram of the reset functions in a typical system design is shown in Figure 1.2.

CLOCK GENERATION

This section of the chip does a fairly straightforward job of generating the system and peripheral clocks. The peripheral clock input is a constant 48 MHz which is used for generating the clocks for the floppy disk. One of these clocks, DSK16M is a constant 16 MHz. A control input, DKCK16 determines the clock frequency generated at the DSK96M output. If DKCK16 is low, then the DSK96M output is the 9.6 MHz required for high density 5 1/4" floppies. Otherwise the output is the 16 MHz used for other floppy disk requirements.

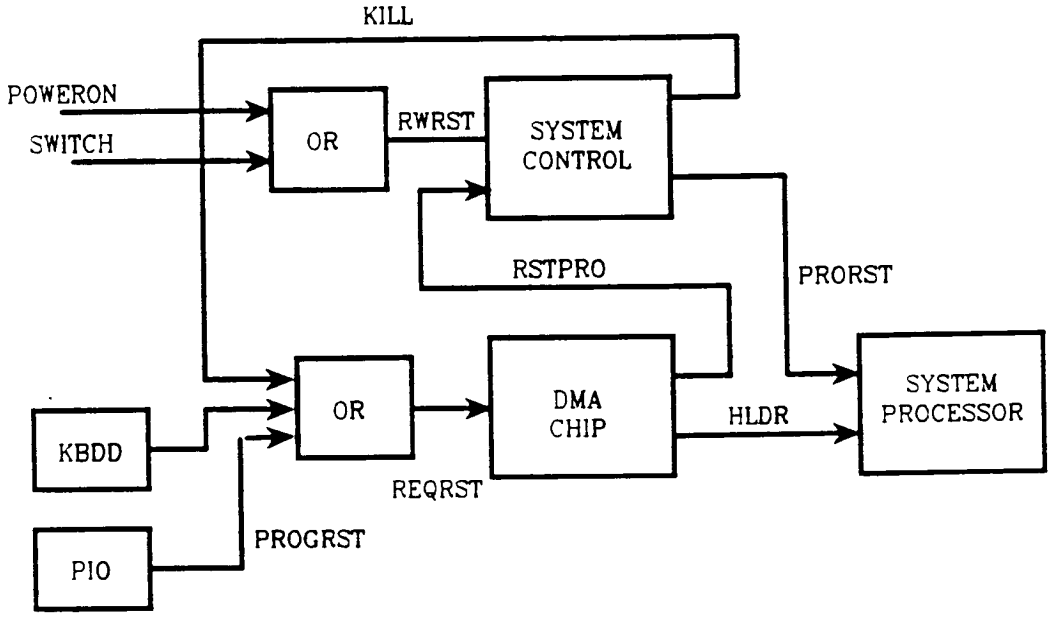


Figure 1.2 Reset - System Block Diagram

ACCESS INTERPRETTER & LATCHES

This block takes inputs from the microchannel and system processor as well as latched microchannel information to provide an encoded output which represents the current state of the system bus activity.

The chip determines the size of the processor currently in control of the system buses by monitoring the TR32 pin. When this pin is low, it means that a 32 bit master is in control. The GC183 DMA Controller is a 16 bit master in a PS/2 compatible design. The system implementation in a system with a 16 bit system processor would normally tie this pin only to the TR32 signal of the Micro Channel. In a system with a 32 bit system processor, the Micro Channel would normally be ORed with an indication (such as HOLDA being inactive) that the 32 bit system processor was in control.

The GC181 has signal connections which are appropriate for both 16 and 32 bit processors. The /PS0, /PS1, and PMEM signals provide the processor status information when an 80286 serves as the system processor. The PWRI, PDAT and PMEM signals which correspond to the similarly named signals on the 80386 processor family provide this status in 80386 or 386SX systems. The chip knows which signals to use for bus cycle interpretation by examining the TR32 signal as described above. The /LOCK signal on the 80386 is not required in a system design because the HOLDR/HOLDA mechanism of the processor is used as a means of acquiring and acknowledging acquisition of system resources by other masters (or DMA) in the system. Since the processor will not go into a HOLD while a LOCK condition is in progress, this HOLD mechanism provides adequate synchronization of system operations.

BUS CONTROL STATE MACHINE

This block is the real heart of the chip. It takes the encoded information from the ACCESS INTERPRETTER block which identifies the current bus state as well as the additional information directly from the microchannel and the feedback regarding the LAST CYCLE from the buffer control block in order to determind the next machine state. The state machine block directly provides the critical control signals for the Micro Channel operation as well as the READY signal to the system processor, DMA controller and memory controller.

TR32	/PBE3	/PBE2	/PBE1	/PBE0	/CWLE	/CBHE	/CBLE	/CBE3	/CBE2	/CBE1	/CBE0
0	1	1	1	0	0	1	0	1	1	1	0
0	1	1	0	1	0	0	1	1	1	0	1
0	1	0	1	1	1	1	0	1	0	1	1
0	0	1	1	1	1	0	1	0	1	1	1
0	1	1	0	0	0	0	0	1	1	0	0
0	1	0	0	1	0	0	1	1	0	0	1
0	0	0	1	1	1	0	0	0	0	1	1
0	1	0	0	0	0	0	0	1	0	0	0
0	0	0	0	1	1	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0
1	X	0	1	0	0	1	0	1	1	1	0
1	X	0	0	1	0	0	1	1	1	0	1
1	X	0	0	0	0	0	0	1	1	0	0
1	X	1	1	0	1	1	0	1	0	1	1
1	X	1	0	1	1	0	1	0	1	1	1
1	X	1	0	0	1	0	0	0	0	1	1

Figure 1.3 Bus States

	/PS0	/PS1	PWRI	PDAT	PMEM
80286	CPU&DMA	CPU&DMA	DMA	N/C	CPU&DMA
803863SX	DMA	DMA	CPU&DMA	CPU&DMA	CPU&DMA
80386	DMA	DMA	CPU&DMA	CPU&DMA	CPU&DMA

CPU CONNECTIONS

	PWRI	PDAT	PMEM	/S0	/S1
INTERRUPT ACKNOWLEDGE	0	0	0	0	0
INSTRUCTION FETCH	0	0	1	1	0
I/O READ	0	1	0	1	0
MEMORY READ	0	1	1	1	0
N/A	1	0	0	1	1
HALT (add = 2)	1	0	1	0	0
SHUTDOWN (addr = 0)	1	0	1	0	0
I/O WRITE	1	1	0	0	1
MEMORY WRITE	1	1	1	0	1

Figure 1.4 Processor to Channel - Control Translation

BUFFER CONTROL

The BUFFER CONTROL block takes inputs from the STATE MACHINE block, the Micro Channel and the system processor in order to privide control to the Micro Channel and to the bus buffers in the system. Figure 1.3 shows the relationship between the byte enable inputs to the chip, /PBE0-3, the TR32 signal and the control signals provided to the Micro Channel for a given cycle. In a system with an 80386 processor, the connections of the byte enable input signals corresponds directly to those similarly named signals on the processor. For 16 bit wide processors (80386SX or 80286) then the /PBE2 signal is connected to A1, /PBE1 is connected to /BHE and /PBE0 connects to either /BLE on the 386SX or A0 on the 80286. The first table shown in Figure 1.4 gives the control signal connections for the supported processor types as well as the DMA chip in order to implement a PS/2 system. The other table shows the translation between the 80386 type of control signal connection and the Micro Channel control signals.

The bus buffer controls bits are used to implement the bus steering and translations required to do bus size matching when the Micro Channel resident devices and the current bus master are of different data sizes. This size matching not only includes the mapping of data from one part of the bus to another, but also includes the latching of data in order to accumulate a complete word of data for presentation to a 32 bit processor.

The buffer controls consist of four signal groups which can be used to control the operation of a discretely implemented set of system bus buffers if the system design does not include a GC184 configured as a data buffer. The signals LB0-2 are used to latch the bytes appearing on Bytes 0-2 of the Micro Channel. The signals /ENR0-2 read these latched bytes onto the processor data bus during subsequent cycles. The /ENX1-3 signals are used to control crossover buffers. /ENX1 copies data between bytes 0 of the processor bus and byte 1 of the Micro Channel. /ENX2 copies data between the word consisting of bytes 0 and 1 of the processor bus and the word consisting of bytes 2 and 3 on the Micro Channel. Finally, /ENX3 copies a byte between byte0 of the cpu bus and byte 3 of the Micro Channel.

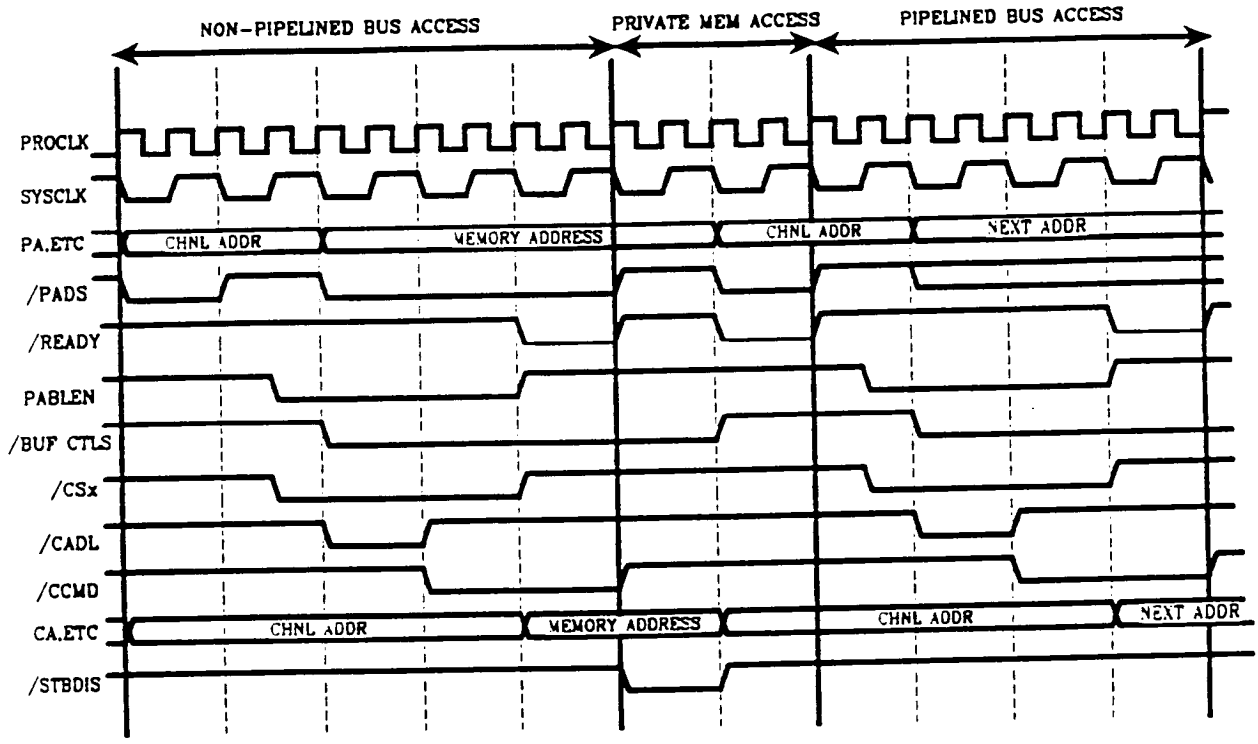


Figure 1.5 Basic System Timing

TIMING

The timing diagram in Figure 1.5 illustrates a mix of Micro Channel and private memory cycles. The first cycle is a non-pipelined cycle which might result from a an idle cycle occuring or a system design which did not force a pipelined cycle for a particular I/O operations. Due to the startup time associated with this particular cycle, the total duration exceeds the normal Micro Channel time by one cpu microcycle. The subsequent private memory access and Micro Channel cycle are both pipelined. Note that the signal PABLEN is required to latch the processor address due to the pipelining.

The timing diagram of Figure 1.6 shows the phasing of the Processor Reset signal with respect to the system clocks. Figure 1.7 illustrates the timing for a Micro Channel access which is extended by an adapter on the channel using the asynchronous channel extension capability of the IOCHRDY line.

All of the signals generated by the GC181 are referenced to the leading edge of PROCLK as given in Figure 1.8. External inputs with hold time requirements are also referenced to this same clock edge. The typical loading requirments are also given in the accompanying table.

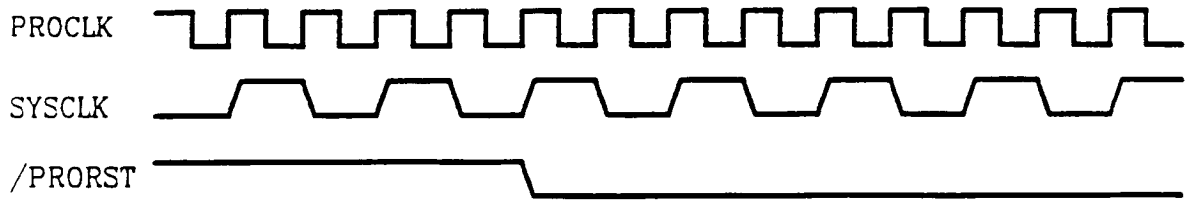


Figure 1.6 - Phasing of Processor Reset

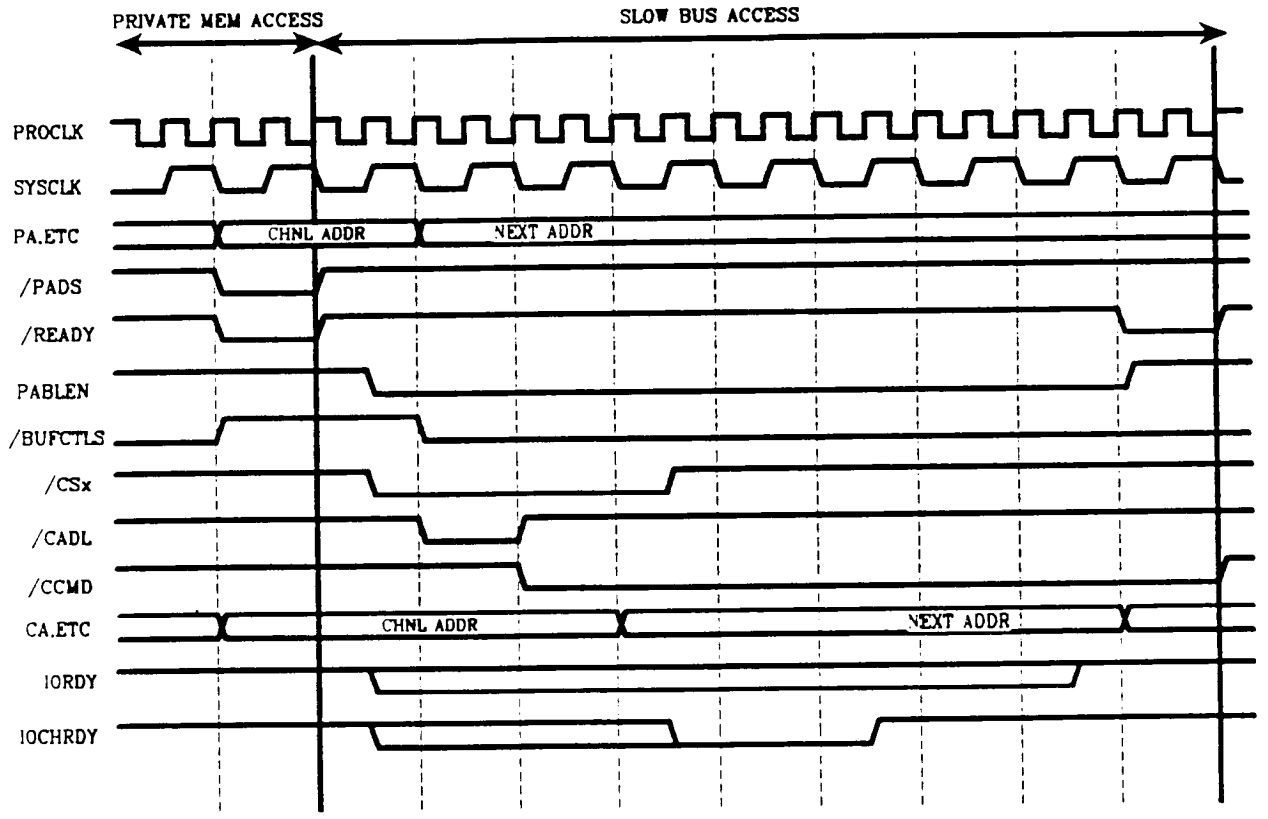


Figure 1.7 - Asynchronous Extended Micro Channel Cycle

GC181 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vcc	Supply Voltage	-	7.0	V
Vi	Input Voltage	-0.5	5.5	V
Vo	Output Voltage	-0.5	5.5	V
Top	Operating Temperature	-25	85	C
Tstg	Storage Temperature	-40	125	C

GC181 Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vcc	Supply Voltage	4.75	5.25	V
Ta	Ambient Temperature	0	70	V

GC181 DC Characteristics

Symbol	Parameter	Min	Max	Unit	Conditions	Notes
VIL	Input Low Voltage	VSS	0.8	V	4.75<VDD<5.25	
VIH	Input High Voltage	2.0	VDD	V	4.75<VDD<5.25	
IIL	Input Low Current	-10.0	-	uA	VIN=VSS	
IIH	Input High Current	-	10.0	uA	VIN=VDD	
VILS	Schmidt Input Low Voltage	VSS	1.0	V	4.75<VDD<5.25	/RAWRST
VIHS	Schmidt Input High Voltage	4.0	VDD	V	4.75<VDD<5.25	
VOL	Output Low Voltage	VSS	0.4	V	0.0mA<IOL<4.0mA	
VOH	Ouput High Voltage	2.4	VDD	V	-4.0<IOH<-0.0mA	
IOH	Output High Current	-10.0	-80.0	mA	VO=VDD	
IOL	Output Low Current	20.0	110.0	mA	VO=VSS	
IOZL	Output Leakage Current/Low	-10.0	-	uA	VO=VDD	Tri-State (high impedance output)
IOZH	Output Leakage Current/High	-	10.0	uA	VO=VSS	
VOML	Low Level Output (medium drive current	VSS	0.4	V	0.0mA<IOL<8.0mA	PABLEN,DT
VOMH	High Level Output (medium drive curren	2.4	VDD	V	-8.0<IOH<-0.0mA	

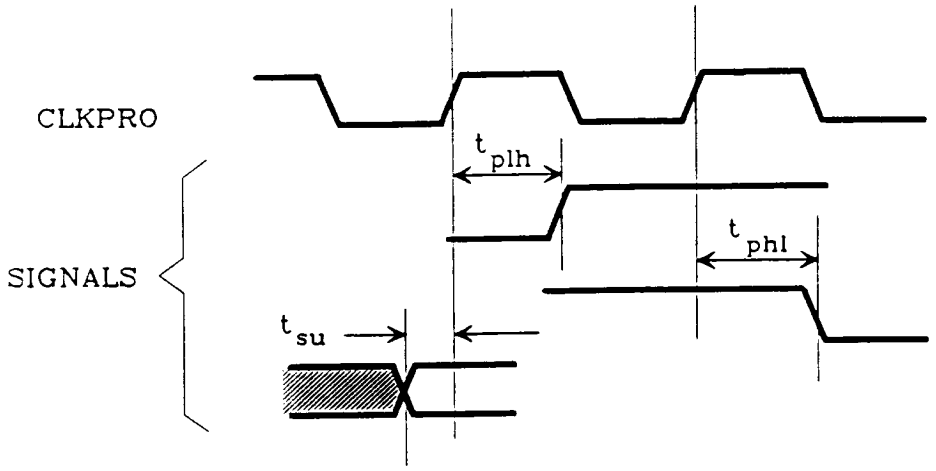


Figure 1.8 - Timing Reference

SETUP TIMES
TO CLKPRO

	MAX (ns)
/STBDIS	5
IORDY	4
IOCHRDY	5

SIGNALS		MIN (ns)	MAX (ns)	LOAD (pf)
/SO, / S1	L- H	7	16	10
	H - L	8	17	
/ADL, /CMD, /MMCCMD,	L- H	5	10	10
	H - L	6	12	
/SYSCLK,	L- H	5	10	20
	H - L	6	12	
/READYD, /PRORST	L- H	5	10	15
	H - L	6	12	
/READY, /BUSY	L- H	5	12	15
	H - L	7	14	
/PABLE	L- H	6	17	45
	H - L	8	22	

DELAY TIMES FROM CLKPRO

Pin Symbol	Pin Numbers	Pin Type	Description
CLOCK GENERATION			
CLK48M	32	I	48 MHz Oscillator Clock. An input signal used to generate DSKCLK and PERCLK.
CLKPRO	3	I	A clock input which runs at double the speed of the processor microcycle rate. This is the same signal as PROCLK for an 80286 processor or CLK2 for an 80386. It as used for running the internal Bus Controller state machine.
DKCK16	28	I	Disk Clock 16. The state of this input signal determines if DSK96M is 16 MHz (high) or 9.6 MHz (low).
DSK96M	26	O	Disk Clock. An output signal used as the floppy disk clock. It is either 9.6 MHz or 16 MHz depending on the state of the DKCK16 input signal.
DSK16M	49	O	This is a constant frequency 16 MHz clock which is equal to CLK48M divided by 3. It can be used for floppy disk control or for any other system element which needs 16 MHz.
PERCLK	24	O	This output is equal to CLK48M divided by 26 for a resultant frequency of 1.846MHz. It typically is used for the serial I/O functions in the system..
SYSCLK	57	O	System Clock. An output signal that is used to synchronize the Bus / CPU Controller to the processor and the Memory Controller. Its frequency is equal to 1/2 the frequency of PROCLK.
CPU INTERFACE			
/PADS	39	I	Processor Address Status. This input signal from the processor indicates that a valid bus cycle is in operation and that a valid address is present on the processor output pins
PDAT	37	I	Processor Data / -Control. This input signal from the processor indicates whether the current cycle is a Data (high) or Control (low) operation.

Pin Symbol	Pin Numbers	Pin Type	Description
/PS0, /PS1	40,41	I	Processor Bus Cycle Status. These input signals indicate initiation of a bus cycle and define the bus cycle type in a 80286 system. In any system, these signal are also connected to the S0OUT and S1OUT signals of the GC183 DMA controller.
/PENA	45	I	Processor enabled. This input is the hold acknowledge from the processor or a similiar function from the DMA. When high, it releases the bus to prevent contention.
IORDY	43	I	I/O Ready. This input delays the generation of /READY to the processor.
/PBE0 - 3	59-62	I	Processor Byte Enables. These inputs from the processor indicate which bytes of the data bus are involved with the current transfer. Internal circuitry determines from these signals the proper bus signals to enable. They are connected directly to the corresponding pins of an 80386 processor. For 16 bit processors the /PBE3 signal is not active and should be pulled up. The remaining signals /PBE0-2 should be connected to A0, /BHE and A1 for an 80286 or /BLE, /BHE and A1 for an 80386SX.
PMEM	38	I	Processor Memory / -IO. This input signal from the processor indicates whether the current cycle is a Memory (high) or I/O (low) operation.
PRORST	55	O	Processor Reset. This active high output is used to reset the processor. It is caused by either the RAWRST or the RSTPRO inputs being active.
/RAWRST	25	I	Raw Reset. This active low input will cause a reset to the system which lasts for the duration of the input level and for 1 minimum of 16 clock cycles after the signal goes to the inactive high level.
/READY	50	O	Ready. This active low output is the READY signal for a 80386 processor.
/READYD	51	O	Ready Delayed. This active low output is the READY signal for a 80286 processor. It is similiar to the /READY output signal but the trailing edge is delayed by one CLKPRO cycle to match the requirements of the 80286..
/RSTPRO	10	I	Reset Processor. An active low signal on this input will produce the PRORST output signal.

Pin Symbol	Pin Numbers	Pin Type	Description
/SYSRST	56	O	System Reset. This active low output is used for general system reset. It is caused only by the RAWRST input signal.
PWRI	36	I	Processor Write / -Read. This input signal from the processor indicates whether the current cycle is a Write (high) or a Read (low).
KILL	42	O	Shutdown instruction. This is a decode of the processor shutdown instruction which causes a partial reset to the system. It goes to the GC183 DMA part to assure that there is proper timing of the reset to prevent partial DMA cycles from occuring.
MICRO CHANNEL INTERFACE			
/ADL	14	O	Address Decode Latch (Micro Channel signal). This active low output signal is used by channel devices to latch valid address and status bits.
/CBE0 - 3	19-22	O	Channel Bus Enables (Micro Channel signals). These active low output signals are used during 32-bit data transfers to indicate which bytes will be placed onto the bus.
/CBHE	46	IO	Channel Byte High Enable. A bi-directional signal used to enable transfer of data on the high byte of the data bus.
/CBLE	23	IO	Channel Byte Low Enable. A bi-directional signal (same as address bit A0) used to enable transfer of data on the low byte of the data bus.
/CMD	15	O	Command (Micro Channel signal). This active low bi-directional output signal is used to execute read and write commands on the Micro Channel bus.
/CWLE	47	IO	Channel Word Low Enable. A bi-directional signal (same as address bit A1) used to steer bytes of data on the Micro Channel bus.
/DV16	35	O	Data Size 16 Return (Micro Channel signal). This active low output signal allows channel bus masters to monitor the data size information.
/DV32	34	O	Data Size 32 Return (Micro Channel signal). This active low output signal allows channel bus masters to monitor the data size information.
IOCHRDY	44	I	I/O Channel Ready (Micro Channel signal - CD CHRDY). This input is used by a channel device to extend the time needed to complete an operation.
/MMCCMD	16	O	Matched Memory Cycle Command (Micro Channel signal). This active low output signal is used to indicate valid data on the bus during a Matched Memory cycle.

Pin Symbol	Pin Numbers	Pin Type	Description
/S0, /S1	12,13	IO	Status Bits 0 and 1(Micro Channel signals). These bi-directional signals indicate the start and type of a channel cycle.
TR32	33	I	Translate 32 (Micro Channel signal). When this input signal is low, 32-bit bus masters drive /CBE0 - 3.
BUFFER CONTROL SIGNALS			
/BUSDIS	29	I	Bus Disable. This input signal disables data buffer control signals so that bus collisions are avoided when the CPU programs the DMA registers.
DT	54	O	Data Transmit. When this output signal is high, it enables the direction of data from the processor to the bus. When it is low, the data direction is from the bus to the processor.
/ENB0 - 3	65-68	O	Enable Data Buffers. Depending upon the bus cycle type, these active low output signals will control the bus data buffers.
/LB0-2	7-9	O	Latch bytes. These signals may be used with discrete buffers to cause bytes on the bus to be latched for subsequent readback to the system processor as an assembled word. Used in conjunction with the /ENRX signals.
/ENR0-3	4-6	I	Enable latched byte read. These three lines control reading of the byte latches in a discrete bus buffering implementation. This is part of the bus translation mechanism used for the reading of 32 bit quantities from devices with data paths as small as 8 bits.
/ENX1	58	O	Enable Byte Crossover. This active low output enables the data buffer to crossover from data byte 0 to data byte 1.
/ENX2	63	O	Enable Word Crossover. This active low output enables the data buffer to crossover the lower 16 bits to the upper 16 bits.
/ENX3	64	O	Enable byte opposite byte crossover. This active low output enables the data buffer to crossover from data byte 0 to data byte 3.
/MMCYCL	31	I	Matched Memory Cycle. This input is used to indicate a Matched Memory cycle is in progress.
/PABLE	11	O	Processor Address Bus Latch Enable. This active low output signal is used to latch the address bus buffers.
/STBDIS	30	I	Strobe Disable. This input signal when low will disable channel controls to allow the CPU faster main memory accesses.

Pin Symbol	Pin Numbers	Pin Type	Description
TEST SIGNALS			
BUSY	48	O	This active high output signal indicates that a bus cycle is in progress.
/TEST	27	I	Test control which disables all of the outputs.
MISCELLANEOUS			
VDD	17,53,1		Power
VSS	18,52,2		Ground

FEATURES

- Private memory bus for high performance
- Page/Interleave mode operation
- Up to 8 Megs of Memory on Board
- Shadow RAM BIOS
- Split memory
- Programmable memory speed
- Memory bank reassignment

OVERVIEW

The Memory Controller is designed to interface system board DRAM to the Micro Channel and the CPU. The CPU access to the system board memory is through a private bus with much faster access than is available for memory resident on the Micro Channel. Page and interleave operation provides a means of operating with a minimal number of wait states by effectively eliminating or overlapping portions of the memory access cycles.

BLOCK DIAGRAM

The block diagram for the GC182 is shown in figure 2.1. Two kinds of accesses are possible; those that use the private memory bus and those that come through the Micro Channel. In order to be qualified as an access via the private memory bus the access must be from the CPU, must be a read operation and must be within the address range of the system board memory as currently configured. If the memory operation is a write, it is forced to go through the Micro Channel so that any bus watch devices on the bus can monitor any changes to the state of the memory.

The CPU access detection block monitors the control lines from the CPU to determine the start of a new memory access cycle and whether this cycle is a read. Simultaneously the Address Comparison Block checks to determine whether or not the currently initiated memory access is within the address range of the memory installed on the system board. If these conditions are met, it provides appropriate signals to the internal Sequencer block as well as to the GC181 Bus Controller that a private bus memory access is in progress. The Address Com-

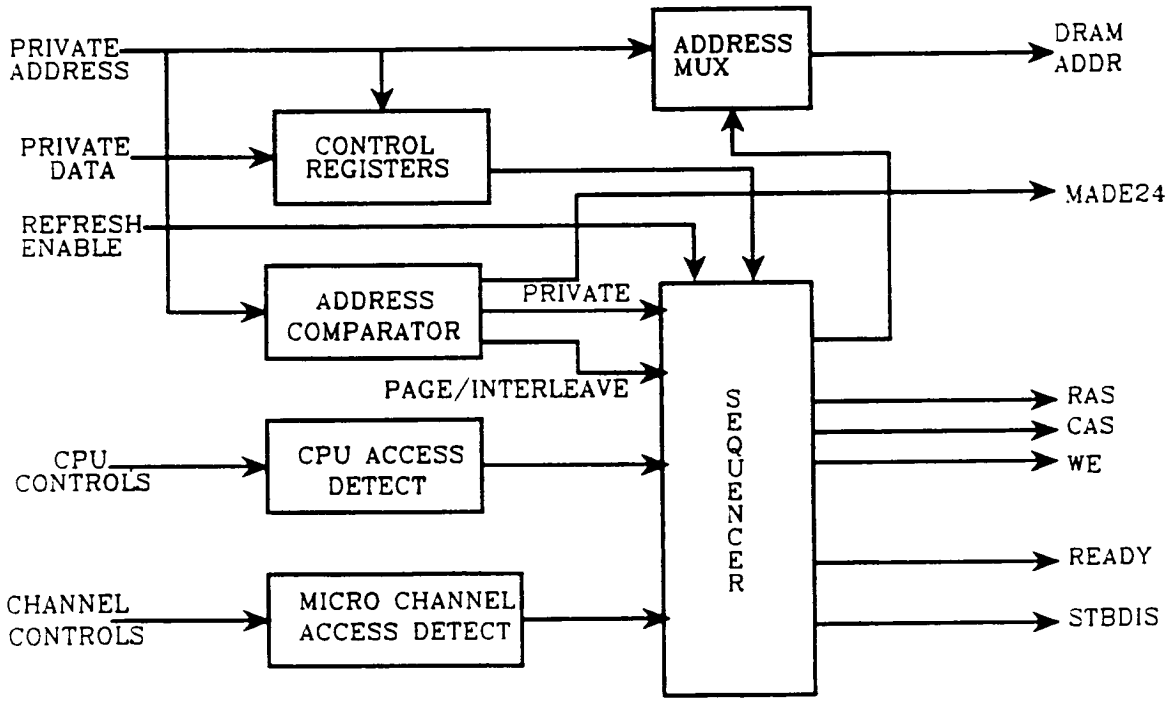


Figure 2.1 - Memory Control Block Diagram

parison block also checks for whether the current access can take advantage of the page and interleave modes based upon the selected configuration and memory capacity. Internal signals based upon these comparisons are passed along to the Sequencer block.

The Micro Channel Access Detection block performs the same functions as the equivalent block for the CPU. In this case it monitors the Micro Channel controls to determine the start of an access.

The Sequencer block generates the necessary detailed timing signals for support of the memory. This includes the necessary RAS and CAS signals to access the DRAMs as well as the PRDY (Private Bus Ready) signal to indicate that the memory access is complete. If page mode is enabled and the current access is on the same RAM page as a previous access, the RAS from the previous access does not change and only the CAS needs to be generated. If interleave is enabled, an access to the other bank of memory from the previous access is begun. Modifications to these cycles occur if a "miss" is indicated from the Address Comparison block. Use of both page and interleave modes of access can eliminate almost all wait states in a typical processing environment without resorting to extremely high speed memories. If the memory operation is due to a Micro Channel cycle either because it is a write operation or is initiated by a source other than the system CPU, the Sequencer monitors the Micro Channel to sequence the memory cycle.

The Address Multiplexor block provides the address multiplexing appropriate for DRAM operation in response to the internal mux signal from the Sequencer block.

MEMORY CONFIGURATIONS SUPPORTED

The GC182 supports either 16 or 32 bit memory configurations appropriate to the data size of the system processor. In addition, 256K, 1Meg and 4 Meg chip densities are supported. The 1Meg density may be in a 256K x 4 configuration and the 4 Meg density must be in as 1Meg x 4. This results in the following memory increments being available in the computer systems:

System Processor	Data Size	RAM Chips	Single Bank	Dual Banks
80286, 80386SX	16 Bit	256K x 1	512K	1Meg
		256K x 4	512K	1Meg
		1Meg x 1	2Megs	4Megs
		1Meg x 4	2Megs	4Megs
80386	32 Bit	256K x 1	1Meg	2Megs
		256K x 4	1Meg	2Megs
		1Meg x 1	4Megs	8Megs
		1Meg x 4	4Megs	8Megs

SYSTEM PROCESSOR SUPPORT

The GC182 directly supports 80386 and 80386SX processors with clock speeds to 20 MHz and 80286 processors with clock speeds to 16 MHz. For 80386 clock speeds above 20 MHz, cache memory systems are required to achieve performance commensurate with the processor capabilities. For these systems the GC182A part must be used.

SYSTEM CONFIGURATION

The GC182 resides between the private address bus and the system board DRAM. When the system processor makes accesses to the private memory, this bus is driven by that processor. This circumstance remains true during private memory write operations which necessitate a use of the Micro Channel in order to allow bus watch devices to monitor memory modifications. When Micro Channel operations are in progress which don't involve the system processor the processor is put into a HOLD state and this address bus is driven by the source of the Micro Channel cycle. For DMA operations, the GC183 chip drives this bus directly and for other bus masters the address is driven from the Micro Channel via the GC184 Address Buffer.

The output of the address multiplexor within the chip must be buffered by external TTL bus drivers in order to drive the heavy capacitive load represented by the DRAM memory array.

MEMORY CONFIGURATION OPTIONS

Interleave Mode / Page Mode is a configuration option which gives near zero wait state performance with readily available DRAMs. If the controller is set up for Special mode, the memory is organized to work in the Interleave mode when two banks are installed. Consecutive 32-bit word accesses will be from two different banks. If accesses are from the same bank, then the Page mode will be applied whenever possible. The memory uses 8K byte pages (4K byte for 256K chips). The memory configurations are described in more detail below.

Memory Below 1 Mbyte may be set to 512 Kbytes or 640 Kbytes.

The remaining memory of the first megabyte may be split, i.e. it may be used for other purposes. If the ENSPLIT bit is set to a 0 then the memory above 512K or 640K will be relocated to the 1 Meg boundary defined by the low order four gbits of the Split Address Register at E0 Hex. If these four bits are all zeros, the split function is disabled by hardware within the chip to avoid a conflict with the low order memory in the system.

The BIOS ROM address range (0E0000H - 0FFFFFH) can be duplicated in DRAM at the same address to speed up the BIOS accesses. The ROM contents are first copied to a RAM area prior to invoking this option and then subsequently copied to this address range in RAM. In order to use this option, the ENSPLIT option must be inactive.

MEMORY REASSIGNMENT

A 1 megabyte block of memory may be deactivated if errors are found during POST (Power On Self Test). This allows the computer system to continue to be useable in what would otherwise be a catastrophic failure condition. This reconfiguration is only valid if the memory consists of 1 meg capacity chips (or 1Meg x 4). The reconfiguration is accomplished by using the high order 4 bits of register EO to disable the block in error. The bit corresponding to the page which has an error is set to zero to disable the error page. The higher order pages are automatically remapped as contiguous memory. Note that in a memory system with dual banks and populated with 1 MBit memory devices, an entire bank of memory will be disabled if an error is found within the bank. This is the only way that the interleave feature can operate correctly.

REGISTERS

Three registers are used in the Memory Controller to provide configuration information. Two of these are read and write I/O addresses at 00E0 and 00E1. The third, the Startup register is a write-only register which is latched from the byte wide chip data bus on the trailing edge of RESET. The contents of this register may not be accessed or modified by the system processor.

In the first 1M address space (00000H - 0FFFFFH), the RAM located above the first 512K or 640K addresses overlaps with the BIOS ROM, and the video RAM. To avoid wasting this memory, the Memory Controller can re-assign it to another address block, beginning at a 1M page boundary. (This is called split-memory). The remap address bits in this register are only used if the ENSPLIT bit is enabled (set to 0) and the ROMEN bit is disabled (set to 1). This register identifies the starting address most significant four bits for the excess 512K (for 512K assigned at 000000) or 384K (for 640K at 000000) of RAM. Note: SPA20-23 are set to zero at reset and must be set to a non-zero value if this feature is used to avoid conflict with the lowest 1 Meg of memory.

Split Address Register
Port E0 Hex

Bit	Label	Function
7	S34M	1 Meg Page
6	S23M	Enables
5	S12M	
4	S01M	
3	SPA23	MSB
2	SPA22	
1	SPA21	
0	SPA22	LSB

At RESET, SPA20 - SPA23 are set to 0.

This register is used to select size, mapping and parity check options for the system board memory. In addition

to determining the amount of memory installed, it also enables the splitting of memory and whether or not the ROM address space is remapped to RAM.

Memory Encoding Register
Port E1 Hex

Bit	Label	Function	Value at Reset
7	EN4	Constant = 1	1
6	EN3	0 = Bank 1 present	0
		1 = Bank 1 absent	
5	EN2	Constant = 1	1
4	EN1	0 = Bank 0 present	0
		1 = Bank 0 absent	
3	ENSPLIT	0 = Split memory	1
		1 = No split memory	
2	S640	0 = 640K RAM at 0H	0
		1 = 512K RAM at 0H	
1	ROMEN	0 = BIOS into RAM	1
		1 = BIOS in ROM only	
0	ENPCHK	0 = Enable parity chk	0
		1 = No parity check	

Setup Register: The Setup register is a write-only register which determines the hardware configuration expected on the system board. It tells the hardware the memory speed, memory density, processor type and emulation mode for which the system board is designed. Its value is latched on the trailing edge of RESET. The memory controller will only provide interleaved operation when the extended mode operation is selected by the two configuration bits described below. Of course there also must be two banks of memory present for interleave to be operational.

Note: The Bank status bits in both the Setup register and in the register at 00E1 must indicate that the bank is present for the Memory Controller to acknowledge the presence of the Bank.

Setup Register Bit Assignments

Bit	Label	Function
7	BNK1	0 = Bank 1 present
		1 = Bank 1 absent
6	FRAM	0 = Not fast (100 nsec.) RAM
		1 = Fast RAM (80 nsec.)
5	UNM	0 = 256K RAM
		1 = 1M RAM
4	386EN	0 = 80286 CPU
		1 = 80386 or 80386SX CPU
3,2	Reserved = 0	
1,0	Emulation Mode Select	

Bit1	Bit0	Mode
1	1	Model 50/60
1	0	Extended mode
0	1	Model 80,Type 1
0	0	Model 80,Type 2

TIMING DIAGRAMS

The timing shown in Figure 2.2 shows private memory accesses when there is a page miss and when there is a non-interleaved page hit. When the page miss occurs and no interleave is possible, the memory controller must examine the address to determine that there was no page hit. The RAS signals from the previous access are then negated and the precharge time must be met before RAS is reissued to the memory array. Subsequent to this, the CAS and then the READY signals are issued to complete the access. On the same diagram, the next access is determined to be on the same page. In this case, there is no need to issue another RAS. The RAS from the first access is left at the active level and only a new CAS needs to be issued to complete the system processor access to memory.

In Figure 2.3, two sequential channel accesses to memory are shown. The first access is neither paged nor interleaved. The second access is on the same page as the first

and as a result is able to take advantage of the page mode of the memory.

The timing illustrated in Figure 2.4 shows the interleave operation available when two banks are installed in the system configuration. When an interleave "hit" is detected, the access may proceed to the alternate bank of memory earlier since there is no need to wait for the precharge time which would be required for an access to the same memory bank. The result is a fast access to the alternate memory bank.

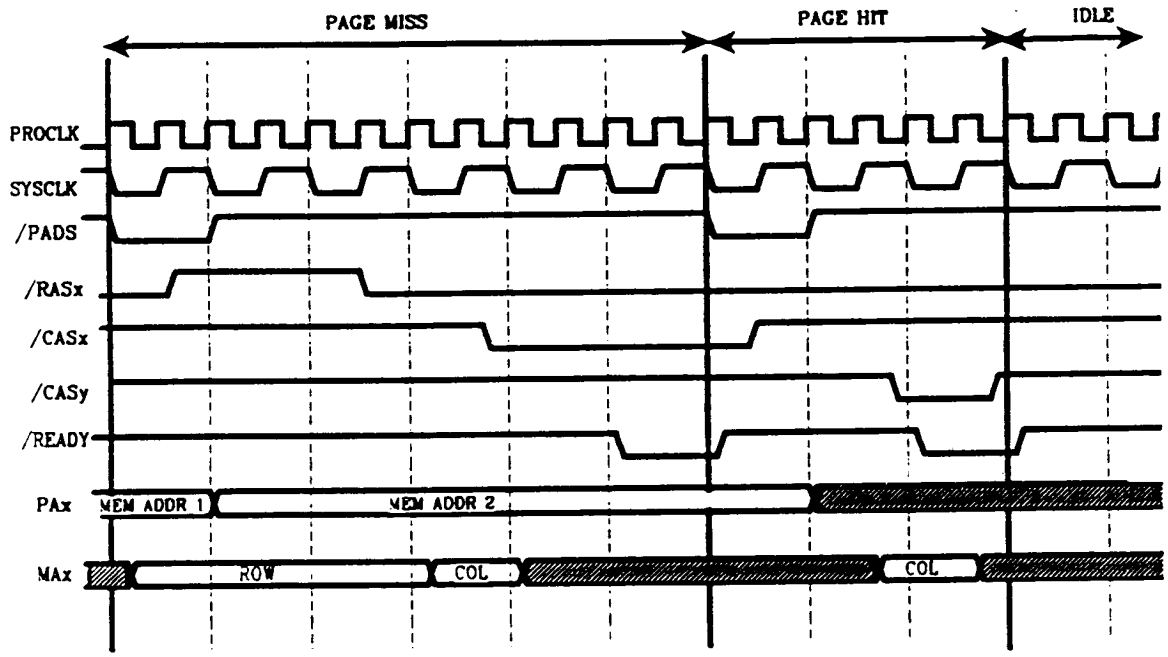


Figure 2.2 - Private Memory Access

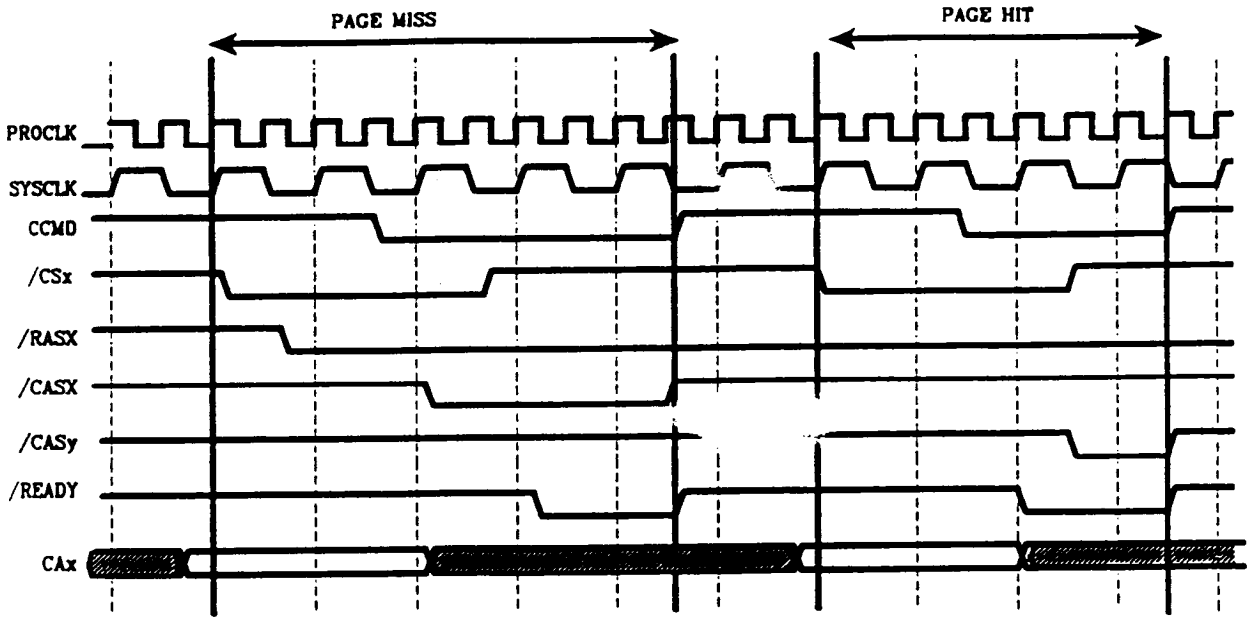


Figure 2.3 - Channel Memory Access

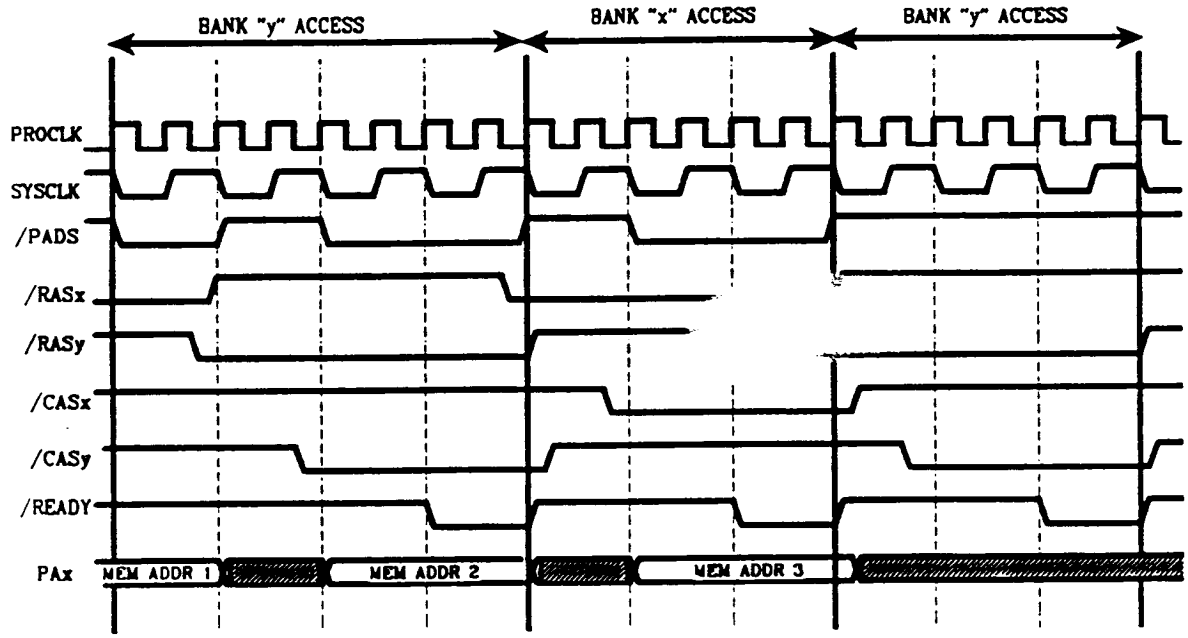


Figure 2.4 Interleaved Memory Access

GC182 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vcc	Supply Voltage	-	7.0	V
Vi	Input Voltage	-0.5	5.5	V
Vo	Output Voltage	-0.5	5.5	V
Top	Operating Temperature	-25	85	C
Tstg	Storage Temperature	-40	125	C

GC182 Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vcc	Supply Voltage	4.75	5.25	V
Ta	Ambient Temperature	0	70	V

GC182 DC Characteristics

Symbol	Parameter	Min	Max	Unit	Conditions	Notes
VIL	Input Low Voltage	VSS	0.8	V	4.75<VDD<5.25	
VIH	Input High Voltage	2.0	VDD	V	4.75<VDD<5.25	
IIL	Input Low Current	-10.0	-	uA	VIN=VSS	
IIH	Input High Current	-	10.0	uA	VIN=VDD	
VOL	Output Low Voltage	VSS	0.4	V	0.0mA<IOL<4.0mA	
VOH	Ouput High Voltage	2.4	VDD	V	-4.0<IOH<-0.0mA	
IOH	Output High Current	-10.0	-80.0	mA	VO=VDD	
IOL	Output Low Current	20.0	110.0	mA	VO=VSS	
IOZL	Output Leakage Current/Low	-10.0	-	uA	VO=VDD	Tri-State (high impedance output)
IOZH	Output Leakage Current/High	-	10.0	uA	VO=VSS	
VOSL	Low Level Output (high drive)	VSS	0.4	V	0.0mA<IOL<12.0mA	/CASxx, /RASxx
VOSH	High Level Output (high drive)	2.4	VDD	V	-12.0<IOH<-0.0mA	
VOML	Low Level Output (medium drive)	VSS	0.4	V	0.0mA<IOL<8.0mA	BRDCLK,/WE,PCLOCK,/CMEN
VOMH	High Level Output (medium drive)	2.4	VDD	V	-8.0<IOH<-0.0mA	/PARSTB,/PMEN

AC Characteristics and reference diagram this page

Pin Symbol	Pin Numbers	Pin Type	Description
CPU, DMA, AND BUS CONTROLLER			
/B0 - /B1	41-40	I	Private Bus Byte Enables. This set of inputs is used with the address bus to steer data for the Memory Controller.
/B2 - /B3	38-37	I	
CA20	80	I	CPU Address Line 20. This input is combined with the GATE20 signal to generate memory address line 20. This signal is used to maintain compatibility with the AT computers.
/CMEN	52	O	Channel to Memory Enable. This output, active low, enables the data line buffers between the memory and the Micro Channel.
/DBUFEN	113	O	Data Bus Enable. This active low output enables the buffers between the data bus and the Memory Controller I/O registers.
A20GATE	51	I	Gate Address Line 20. This input is used to qualify the CPUA20 signal described above.
HOLDA	98	I	Hold Acknowledge. This input indicates that the CPU has relinquished control of the bus in response to a HOLDR request. This signal is used here to differentiate between CPU and DMA accesses for memory reads.
M240-M241	70,71	I	Memory Address Decode 24. Two lines are provided for an external decode which indicates that the high order 8 bits of the current address are all equal to zero. When both of these lines are active, then the address is within the low order 16 MBytes of the address space.
/MADE31	110	I	Memory Address Enable 31. This input signal indicates that the address bits A24 - A31 are all set to 1, which is the ROM address space.
PA2-23	68,34-32,29-27,23, 22,20,119,115,114, 64-62,59,58,56,53	I	Private Address Bus, Bits 2 - 23. This set of inputs is the address bus for the Memory Controller
/PADS	87	I	Address Status. This input signals that a command is starting.
/PMIO	85	I	Private Bus Memory/IO Operation. This input signals that the private bus is performing a memory (set to 1) or I/O (set to 0) operation. This signal is qualified by /PADS.

Pin Symbol	Pin Numbers	Pin Type	Description
/PMEM	83	O	Private Bus to Memory Bus Enable. This active low output enables the buffers between the private data bus and the memory.
PRDY	97	O	Private Bus Ready. This output signals the Bus Controller that a private bus access has been completed.
PWR	84	I	Private Bus Write. This input indicates that the current private bus operation is a write (set to 1) or a read (set to 0).
/ROMCS	94	O	BIOS ROM Selected. This active low output indicates that the BIOS ROM address space has been accessed.
/STBDIS	86	O	Strobe Disable. This active low output signal is sent to the Bus Controller to disable the drivers to the MicroChannel for private bus accesses.
MEMORY			
/CAS0 - /CAS3	13,42,72,102	O	Column Address Select, Even Bank. These active low outputs select the DRAM columns. CAS0N - CAS3N are used for bytes 0 - 3 respectively of the even address bank.
/CAS10 - /CAS13	17,47,77,107	O	Column Address Select, Odd Bank. These outputs select bytes 0 - 3 respectively of the odd address bank.
MA0 - MA2	24-26	O	Memory Address 0 - 9. These output signals are used with CAS and RAS to address the DRAM. These signals must be buffered external in order to drive the system board RAM.
MA3 - MA5	35,36,54	O	
MA6 - MA9	55,65-67	O	
/WE	21	O	Memory Write Enable. This active low output indicates that the current DRAM access is a write to memory. If not asserted, the access is a memory read. This signal must be buffered externally to drive the system board RAM.
/PARSTB	39	O	Parity Strobe. This active low output qualifies the parity checking operation.
/RAS0 - /RAS3	14,44,74,109	O	Row Address Select,Even Bank. These active low outputs select the DRAM banks for bank 0.

Pin Symbol	Pin Numbers	Pin Type	Description
/RAS10 - /RAS13	19,49,78,104	O	Row Address Select, Odd Bank. These active low outputs select the DRAM banks for bank 1.
REN	105	O	Ram Enabled. This active high input permits the system to enable or disable the memory in this part of the system.
MICRO CHANNEL			
/CCMD	82	I	Channel Command. This active low input indicates that the signals on the Micro Channel are stable and the Memory Controller may use them.
D0 - D3	116-119	IO	Data Bus. These are the bidirectional, three state data lines for the Memory Controller.
D4 - D7	2-5	IO	
MADE24	96	I	Memory Address Decode 24. This input is asserted when all of the Micro Channel address bits A24 - A31 are zero, indicating that the address on the bus is lower than 8 MBytes.
CMIO	95	I	Channel Memory/IO. This active low input indicates that the current operation is a memory access (if 1) or an I/O operation (if 0).
/RFRSH	112	I	Refresh. This active low input commands the Memory Controller to perform a memory refresh.
/CS0	88	I	Command Status Bit 0. This input signal is used to decode the channel commands.
/CS1	89	I	Command Status Bit 1. This input signal is used to decode the channel commands.
CRDY	57	O	Channel Memory Ready. This output signals the MicroChannel of the end of a memory cycle. This signal is also generated during accesses to the Memory Controller registers.
/MMCR	93	O	Matched Memory Cycle Return. This active low output indicates that the Memory Controller will accept a matched memory cycle.

Pin Symbol	Pin Numbers	Pin Type	Description
/LOCK	92	I	Lock memory configuration registers. Whenever this signal is at a low state, the software is unable to access the memory configuration registers at addresses E0 and E1.
OTHER			
BOSC	7	I	14 MHz. Clock. This input signal is the same as OSC on the Micro-Channel.
/BRST	6	I	System Reset. This input resets the Memory Controller.
BSYSCLK	111	I	System Clock. This input is the system clock from the Bus Controller.
BRDCLK	69	O	Processor Clock. This output signal is the CPU clock for a 80386 processor implemented in the system.
/TESTIN	46	I	Test Input. This active low input places the Memory Controller in a test mode. This signal is used for functional testing of the part before it is installed in the system, not for in-circuit testing.
BMCLK	99	I	Master processor clock. Comes from an oscillator running at double the processsor clock frequency.
PCHKEN	8	O	Parity check enable. This output is from one of the bits in memory configuration register E1 which enables or disables parity checking in the on-board system memory.
PCLOCK	81	O	Processor clock for an 80286 processor implementation on the system board.
BUSY	100	I	Busy signal from the GC181 bus controller chip. Synchronizes the memory controller operation to cycle boundaries.
MISCELLANEOUS			
VDD	115,45,76,106		Power
VSS	12,16,18,31,43, 48,50,73,75,79, 101,103,108		Ground

FEATURES

- 8 DMA channels
- Compatible and extended mode operation
- DRAM refresh logic
- Numeric coprocessor interface
- Central Arbitration Point
- Floppy Disk Arbitration

OVERVIEW

The GC183 provides eight channels of Direct Memory Access (DMA). The system microprocessor programs the DMA registers for the various modes of operation, transfer addresses and transfer counts. The DMA Controller may be programmed in one of two modes. The first programming mode emulates the operation of two Intel 8237 DMA Controllers. The other programming mode uses extended addressing. In the DMA transfer mode, I/O devices may transfer data directly to and from memory in single transfer, burst or read verification mode. The data transfer is initiated when an I/O device requests and is granted control of the bus by the bus arbitration logic, and the DMA has been programmed to service the DMA request.

BLOCK DIAGRAM

The block diagram of the chip is shown in figure 3.1. The address decode provides the mechanism for selecting one of the many registers contained within the chip. In addition to a number of discrete registers which are available for various functions, there are a number of registers which are contained in register files. These register files contain the Address, Word Count and Control registers for each of the DMA channels supported in a PS/2 architecture. There are a number of data multiplexer and latches to provide not only the standard function of temporary data storage during DMA transfer operations, but also for enhanced off-boundary DMA transfer functionality. The state machine is the major control portion of the chip. Because the chip is so complex, there are extensive test and diagnostic functions included to assure testability during design and manufacturing. Finally, circuitry is included for support of the numeric coprocessor in the system.

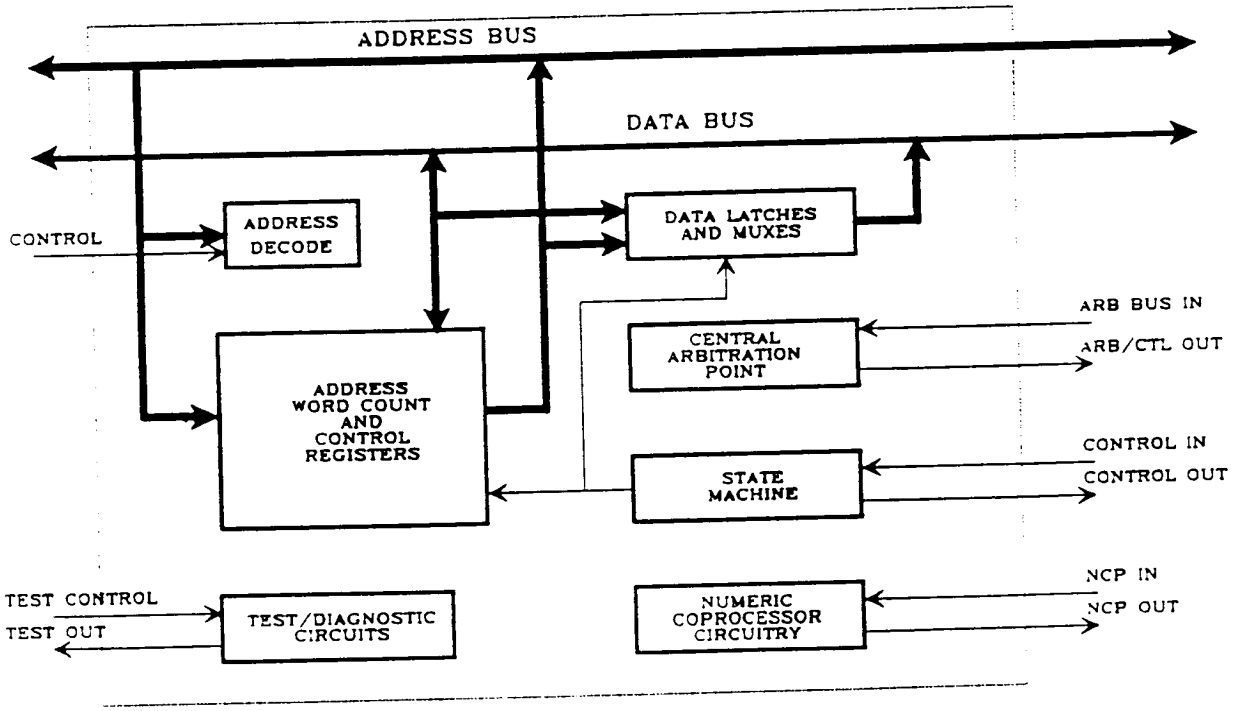


Figure 3.1 - DMA Controller Block Diagram

DATA PATHS

The data paths for the GC183 are shown in the block diagram of Figure 3.2. A major portion of the chip is consumed by the register files which contain the address registers, word counts, etc. Two sets of address registers are stored. One set is the base value which is loaded by the system processor. The other register set are the current addresses which are updated as DMA transfers take place. When a DMA transfer occurs, the current updated address for the transfer is accessed from the register file and output to the Micro Channel. At the same time this address is also either incremented or decremented as specified by the mode register for the selected channel. Bit 6 of the corresponding extended mode register determines whether the address is to be modified by one or two to match the byte or word transfer size.

The transfer count register file structure is very similar to that for the memory address. The 16 bit current count is always decremented by one and therefore is either a word or byte count depending upon the setting of the mode register for the particular DMA channel. The decremented count is examined for a terminal count condition whenever a transfer takes place.

The I/O address is a simple register file. The output is either sent to the address bus on the appropriate Micro Channel cycle or to the data bus if it is being read by the system processor. The mode register is similar in it's simplicity except that its data is for internal use only although it may be read by the system processor by using the extended commands.

There are a number of internal registers which are used for control or status but have fewer than a single register

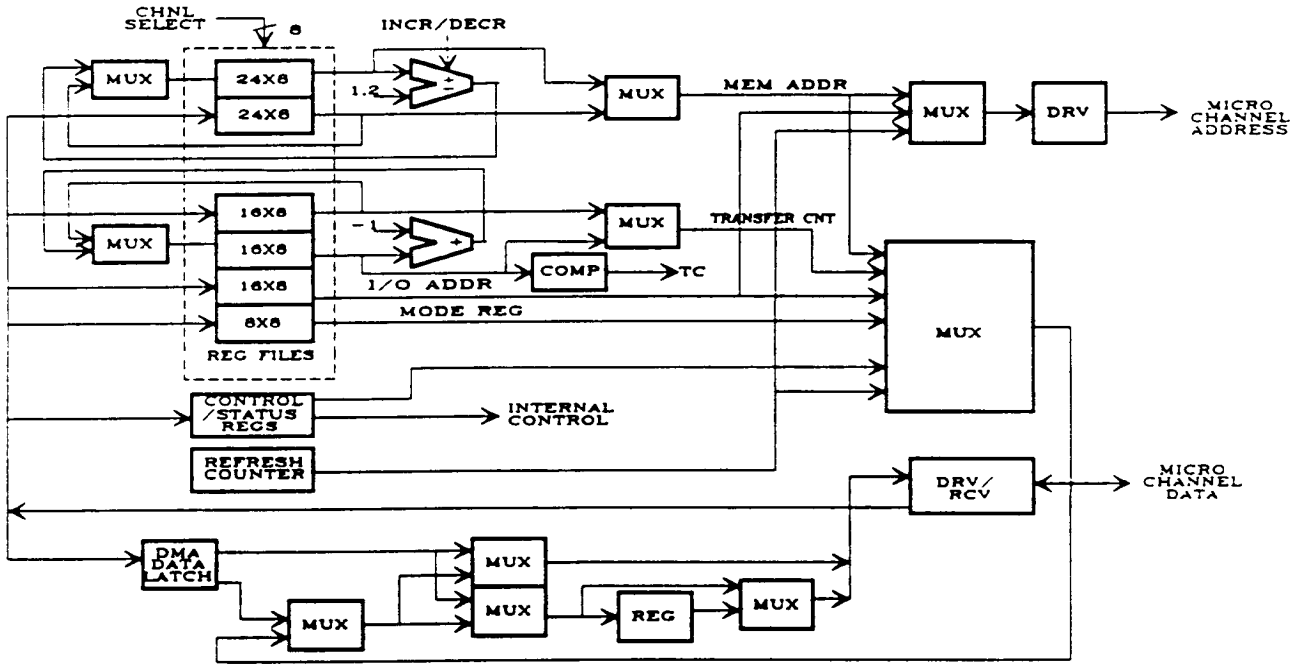


Figure 3.2 - DMA Data Paths

per DMA channel. These registers are therefore not organized into register files but rather as individual registers with outputs into the chip for control as well as into the data mux allowing the system processor to read their contents.

The DMA data latch is used for the temporary storage of DMA data from the first cycle of a DMA cycle pair. This register is not accessible by the system processor. Associated with this same data path are multiplexors and an additional latch which allows the efficient handling of word wide DMA operations which are specified to begin on an odd byte memory boundary. The way in which such transfers are handled by the IBM implementation is that all memory accesses are single byte accesses with an accompanying word access to the I/O location. This implementation requires three Micro Channel cycles for each word of data transferred. To overcome this performance penalty, the G2 DMA chip provides an additional register for storing one of the bytes of data from a previous DMA transfer. This byte can then be merged with the data for a current transfer to eliminate the extra Micro Channel cycle incurred for odd byte transfers. A comparison of the cycles required for IBM and G2 is shown below in Figure 3.3. The G2 implementation requires almost 1/3 fewer cycles to transfer a block of data to or from an odd memory block boundary.

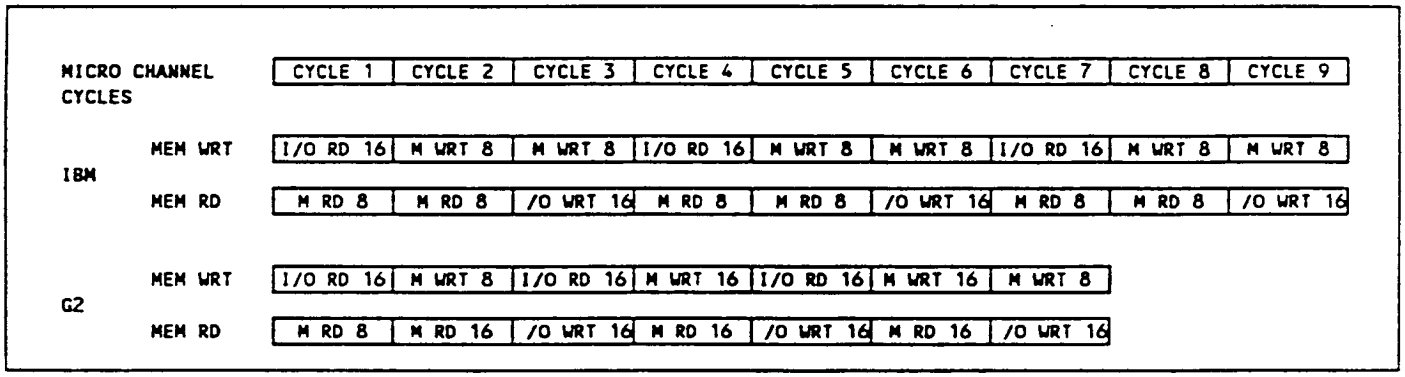


Figure 3.3 - Odd Boundary DMA

SYSTEM CONFIGURATION

The DMA Controller is connected to the private bus to receive instructions from the CPU and to provide the bus control signals during DMA transfers. It is also connected to the Micro Channel to control the bus arbitration process. When the CPU programs the DMA Controller, the CPU treats it like an 8 bit I/O device on the Micro Channel. The DMA Controller uses addresses in the range 0000H - 00DFH. In the 8237 mode, individual registers are represented by separate locations in the I/O address map. In the extended mode, one address is used to store a code which indicates the register being addressed and the function to be performed. A second address is used for the data to be read or written.

OPERATING MODES

The DMA controller operates in the two basic states of Idle and Command. In the Idle mode, the DMA controller is not actively controlling the bus and may be programmed by the system board processor. Conversely, in the command mode the DMA Controller drives Micro Channel bus control signals in order to generate DMA transfers.

REGISTERS

The following registers are contained within the DMA:

Register	Length	Registers
Memory Address (Base)	24	8
Memory Address (Current)	24	8
I/O Address	16	8
Transfer Count (Base)	16	8
Transfer Count (Current)	16	8
Mode	8	8
Status	8	2
Arbus	4	2
Mask	4	2
Temp Holding	16	1
Function	8	1
Arbitration	8	1
Refresh	10	1

CHANNEL REGISTERS

Each of the eight channels uses a set of four registers: Memory Address, I/O Address, Transfer Count, and Mode.

Memory Address Register: Each channel uses a set of Memory Address registers. The base address register is programmed by the CPU with the starting address for the DMA transfer. The base address is copied into the current address register. The contents of the base register do not change during DMA transfers. The current address register points to the memory address to be used in the next transfer and is updated (incremented or decremented) after each DMA transfer cycle. The changes made to this register (increment or decrement and byte or word) are controlled by the contents of the mode register for the channel. The CPU can read the base and current registers. When the autoinitialization option is selected, the base address is copied into the current address register upon completion of the transfer.

I/O Address Register: This register identifies the address for the I/O device being used for the DMA transfer. The contents of this register do not change during DMA transfers and may be read by the system processor.

Transfer Count Register: Each channel uses a set of transfer count registers. The Base Count register is programmed by the CPU with the count of transfers to be performed for the DMA transfer. The count is copied to the current count register. The contents of the Base register do not change during DMA transfers. The current count register is decremented with each transfer that is completed. When this register is decremented from 0000 to FFFF, the terminal count signal is activated. Because of this method of indicating the terminal count, this register should be loaded at setup with the value one less than the number of transfers required. When the autoinitialization option is selected, the base count is copied into the current count register upon completion of the transfer.

Mode Register: The Mode register configures its associated channel for the type of operation to perform during DMA transfers. The functions programmed are the same but the methods for programming this register are different for the 8237 mode and the extended mode. This register may be read only in the extended mode. The bit assignments for the two operating modes are as follows:

Mode Register (8237 Compatible)

Bit	Function
7,6	Reserved = 0
5	0 = Increment Memory Address
	1 = Decrement Memory Address
4	0 = Autoinitialization Disabled
	1 = Autoinitialization Enabled
3,2	00 = Verify Transfer
	01 = Write Transfer
	10 = Read Transfer
	11 = Reserved
1,0	00 = Select Channel 0 or 4
	01 = Select Channel 1 or 5
	10 = Select Channel 2 or 6
	11 = Select Channel 3 or 7

Mode Register (Extended Mode)

Bit	Function
7	Reserved = 0
6	0 = 8 Bit Transfer 1 = 16 Bit Transfer
5	Reserved = 0
4	0 = Memory Address Increment 1 = Memory Address Decrement
3	0 = Memory Read Transfer 1 = Memory Write Transfer
2	0 = Verify Transfer 1 = Data Transfer
1	0 = Autoinitialization Disabled 1 = Autoinitialization Enabled
0	0 = I/O Address Forced to 0000H 1 = I/O Address Taken from I/O Address Register

COMMON REGISTERS

Several registers are shared among the channels or are used for other functions. These are the Status Register, Arbus Register, Mask Registers, Byte Pointer, Temporary Holding Register, and Refresh Register.

Status Register: Two 8-bit Status registers are provided. One for channels 0 thru 3 and the other for channels 4 thru 7. The information in these registers tells which channels have reached a terminal count and which channels have requested the bus since the last time the status register was read (bits are cleared after each time the register is read). This register can be read using either 8237 mode or extended mode.

In the extended mode, the entire byte containing the information for the selected channel is returned. The information is retreived in conjunction with the Byte Pointer. The channel number in the Extended Function Register (address 0018H) is ignored. The value returned corresponds to the group selected by the Byte Pointer. When the Byte Pointer is cleared, it selects the status register for channels 0 - 3. Reading the status register in the extended mode toggles the Byte Pointer.

Status Register Bit Assignments

Bit	Function
7	Channel 3 or 7 Request
6	Channel 2 or 6 Request
5	Channel 1 or 5 Request
4	Channel 0 or 4 Request
3	Terminal count for Channel 3 or 7
2	Terminal count for Channel 2 or 6
1	Terminal count for Channel 1 or 5
0	Terminal count for Channel 0 or 4

Arbus Register: The DMA Controller can work with any of the arbitration levels from 0 to 14, with eight possible channels. Channels 1 - 3 and 5 - 7 are assigned a fixed arbitration level priority to the corresponding arbitration levels as shown. Channels 0 and 4 may be assigned to any of the levels 0-14. Two 4-bit registers are provided, one register is for channel 0 and the other for channel 4. These registers provide virtual DMA operation by allowing the system microprocessor to assign the arbitration level and allow channels 0 and 4 to service devices at any arbitration level. When channel 0 or channel 4 is assigned to one of the pre-assigned levels (1-3 or 5-7), the mask bits are used to select which of the channels (or none) is to be used.

Arbus Register Bit Assignments

Bit	Function
7-4	Reserved
3-0	Arbitration level

Arbitration Levels

ARB Level	Primary Assignment	
-2	Memory Refresh	
-1	NMI	
0	DMA Channel 0	VDMA Channel
1	DMA Channel 1	
2	DMA Channel 2	
3	DMA Channel 3	
4	DMA Channel 4	VDMA Channel
5	DMA Channel 5	
6	DMA Channel 6	
7	DMA Channel 7	
8	Reserved	
9	Reserved	
A	Reserved	
B	Reserved	
C	Reserved	
D	Reserved	
E	Reserved	
F	System CPU	

Mask Registers: If a device requests DMA service by winning the arbitration for a channel which has the mask bit set, the DMA will not execute any DMA transfer cycles. This method may be used for a bus master to gain access to the Micro Channel, or to select among several DMA channels assigned to the same arbitration level. If the arbitrating device does not execute the transfer itself, a timeout will occur which will generate a nonmaskable interrupt.

In the 8237 mode, two 4-bit Mask Registers are provided, one register for channels 7-4, and one for channels 3-0. In the extended mode, the individual bits are set and cleared by selecting the desired channel and using the appropriate command.

Individual mask bits may be set or cleared in either 8237 mode or extended mode. All mask bits are set by a system reset or by a DMA Controller master clear. All mask bits in the four-register group are cleared by a "Clear Mask Register" command in the 8237 mode.

Mask Register Bit Assignments

Single Mask Register
(0000A, 00D4)

Bit	Function
7-3	Reserved = 0
2	0 = Clear Mask Reg 1 = Set Mask Reg
1,0	00 = Select Channel 0 or 4 01 = Select Channel 1 or 5 10 = Select Channel 2 or 6 11 = Select Channel 3 or 7

All Mask Register
(000F, 00DE)

Bit	Function
7-4	Reserve = 0
3	Channel 3 or 7 0 = Clear Mask Reg 1 = Set Mask Reg
2	Channel 2 or 6 0 = Clear Mask Reg 1 = Set Mask Reg
1	Clear Channel 1 or 5 0 = Clear Mask Reg 1 = Set Mask Reg
0	Channel 0 or 4 0 = Clear Mask Reg 1 = Set Mask Reg

Byte Pointer: The memory addressing range requires 24 bits of address data. The Transfer Counter and I/O addresses use 16 bits. To move data on an 8-bit bus, the DMA Controller uses a Byte Pointer. Each access of a part of the system using the Byte Pointer causes it to toggle to the next state. A write to 000CH or 00D8H in 8237 mode or a master reset command will reset the Byte Pointer. In addition, any write to the extended mode Function register (0018H) will reset the Byte Pointer. When reset, the Byte Pointer will select the least significant byte of the word accessed. The next access will be to the next more significant byte. Once the most significant byte is accessed, the Byte Pointer will again toggle to the least significant byte. The Byte Pointer is also used with the Status register to select between the status bits for channels 0-3 and for channels 4-7.

Temporary Holding Register: One 16-bit Temporary Holding register is provided. During a DMA transfer, data that have been read are held in this register while waiting to be written to their destination. The system microprocessor does not have access to this register.

Function Register: One 8-bit Function Register is provided. This receives the extended mode I/O commands and is the register which identifies the operation to be performed The system microprocessor executes functions by first writing to the function register (address 0018) the function is to be performed and the channel to use. The selected function is then executed by writing or reading port address 001A.

I/O Address	Command
0018	Function Register
001A	Execute Function Register

The Function Register bits are assigned as follows:

Bit	Function
7-4	Command
3	Reserved = 0
2-0	Channel

Extended Commands Registers

Command	Register	Bits	Byte Pointer
0 W/R	I/O Address Register	15-00	Yes
1 W/R	Reserved		
2 W	Base and Current Memory Address Write	23-00	Yes
2 R	Base Memory Address Read	23-00	Yes
3 W	Reserved		
3 R	Current Memory Address Read	23-00	Yes
4 W	Base and Current Transfer Count Write	15-00	Yes
4 R	Base Transfer Count Read	15-00	Yes
5 W	Reserved		
5 R	Current Transfer Count Read	15-00	Yes
6 W	Reserved		
6 R	Status Register Read	07-00	Yes
7 W/R	Extended Mode Register Write/Read		
8 W/R	Arbus Register Write/Read	04-00	
9	Mask Register Set Single Bit (Direct from Function Register)		
A	Mask Register Clear Single Bit (Direct from Function Register)		
B W/R	Reserved		
C W/R	Reserved		
D	Master Clear (Direct from Function Register)		
E W/R	Reserved		
F W/R	Reserved		

Arbitration Register: This register is used to program several options for the arbitration function and to monitor the status of key parameters of the arbitration cycle. This register is located at 0090H on the I/O address map. The bit representations are different for writing and reading the register:

Arbitration Register Bit Assignments

Bit	Rd/WR	Function	Initial Value
7	R/W	1 = Enable CPU cycles during arbitration cycles	0
		0 = Disable CPU cycles during arbitration cycles	
6	R	1 = An NMI has occurred and has masked arbitration	
		0 = Normal operation	
	W	1 = Force arbitration when CPU controls the channel	
		0 = Normal arbitration	
5	R	1 = A bus timeout has occurred	0
		0 = Normal operation	
	W	1 = Arbitration time is 600 ns.	0
		0 = Arbitration time is 300 ns.	
4	R/W	1 = Enable Preempt for interrupt request	0
		0 = Disable Preempt for interrupt request	
3 - 0	R	Value of Arbitration Bus during the previous Grant state	
	W	Reserved = 0	

Refresh Register: One 10-bit Refresh register is provided. This register provides memory addresses for the refresh operation. The system microprocessor does not have access to the refresh register.

PROGRAMMING

In 8237 compatibility mode, The DMA Controller contains logic to model two Intel 8237 DMA Controllers. This compatibility model includes a byte pointer which is used internally to sequence through the bytes of a 16 or 24 bit register being addressed through an 8 bit port. When this mode is used for programming, the registers are accessed by selecting individual addresses and reading from or writing to them. Multiple accesses will read or write higher order bytes of multi-byte registers. When in Extended Mode, the processor uses a register pair at addresses 18 and 1A (hex). To address one of the DMA registers in this mode, the system processor first writes to the Function Register at 18 (hex) with a data byte which consists of the function in the high nibble and channel number in the low nibble. The internal byte pointer is always set to 0 when this address is accessed. The system processor then executes the desired function by doing an I/O operation to port address 1A. The second access to address 1A is not required for the commands which execute directly as shown in the Extended Command Table. The DMA Controller provides full 16-bit address decoding for the I/O bus. The functions and their addresses are as follows:

DMA Controller Registers

Address		Function	Byte Pointer
0000	W	Base and Current Memory Address Write Channel 0	Yes
	R	Current Memory Address Read Channel 0	Yes
0001	W	Base and Current Transfer Count Write Channel 0	Yes
	R	Current Transfer Count Read Channel 0	Yes
0002	W	Base and Current Memory Address Write Channel 1	Yes
	R	Current Memory Address Read Channel 1	Yes
0003	W	Base and Current Transfer Count Write Channel 1	Yes
	R	Current Transfer Count Read Channel 1	Yes
0004	W	Base and Current Memory Address Write Channel 2	Yes
	R	Current Memory Address Read Channel 2	Yes
0005	W	Base and Current Transfer Count Write Channel 2	Yes
	R	Current Transfer Count Read Channel 2	Yes
0006	W	Base and Current Memory Address Write Channel 3	Yes
	R	Current Memory Address Read Channel 3	Yes
0007	W	Base and Current Transfer Count Write Channel 3	Yes
	R	Current Transfer Count Read Channel 3	Yes
0008	W	Reserved	
	R	Channel 0 - 3 Status Register Read	
0009	R/W	Reserved	
000A	W	Channel 0 - 3 Single Mask Register Write	
	R	Reserved	
000B	W	Channel 0 - 3 Mode Register Write	
	R	Reserved	
000C	W	Clear Byte Pointer	
	R	Reserved	
000D	W	Master Clear	
	R	Reserved	
000E	W	Channel 0 - 3 Mask Register Clear	
	R	Reserved	
000F	W	Channel 0 - 3 All Mask Register Bits Write	
	R	Reserved	
0018		See Extended Mode Operation	
01A		See Extended Mode Operation	
0080	W/R	Not Implemented	
0081	W/R	Channel 2, Page Table Address Register	
0082	W/R	Channel 3, Page Table Address Register	
0083	W/R	Channel 1, Page Table Address Register	
0084 - 0086		Not Implemented	

DMA Controller Registers (Continued)

Address		Function	Byte Pointer
0087	W/R	Channel 0, Page Table Address Register	
0088	W/R	Not Implemented	
0089	W/R	Channel 6, Page Table Address Register	
008A	W/R	Channel 7, Page Table Address Register	
008B	W/R	Channel 5, Page Table Address Register	
008C - 008E		Not Implemented	
008F	W/R	Channel 4, Page Table Address Register	
0090	W/R	Arbitration Register Write/Read	
00C0	W	Base and Current Memory Address Write Channel 4	Yes
	R	Current Transfer Count Read Channel 4	Yes
00C1	W/R	Reserved	
00C2	W	Base and Current Transfer Count Write Channel 4	Yes
	R	Current Transfer Count Read Channel 4	Yes
00C3	W/R	Reserved	
00C4	W	Base and Current Memory Address Write Channel 5	Yes
	R	Current Transfer Count Read Channel 5	Yes
00C5	W/R	Reserved	
00C6	W	Base and Current Transfer Count Write Channel 5	Yes
	R	Current Transfer Count Read Channel 5	Yes
00C7	W/R	Reserved	
00C8	W	Base and Current Memory Address Write Channel 6	Yes
	R	Current Transfer Count Read Channel 6	Yes
00C9	W/R	Reserved	
00CA	W	Base and Current Transfer Count Write Channel 6	Yes
	R	Current Transfer Count Read Channel 6	Yes
00CB	W/R	Reserved	
00CC	W	Base and Current Memory Address Write Channel 7	Yes
	R	Current Transfer Count Read Channel 7	Yes
00CD	W/R	Reserved	
00CE	W	Base and Current Transfer Count Write Channel 7	Yes
	R	Current Transfer Count Read Channel 7	Yes
00CF	W/R	Reserved	
00D0	W	Reserved	
	R	Channel 4 - 7 Status Register Read	
00D1	W/R	Reserved	
00D2	W/R	Reserved	
00D3	W/R	Reserved	
00D4	W	Channel 4 - 7 Single Mask Register Write	
	R	Reserved	

DMA Controller Registers (Continued)

Address		Function
00D5	W/R	Reserved
00D6	W	Channel 4 - 7 Mode Register Write
	R	Reserved
00D7	W/R	Reserved
00D8	W	Clear Byte Pointer
	R	Reserved
00D9	W/R	Reserved
00DA	W	Master Clear
	R	Reserved
00DB	W/R	Reserved
00DC	W	Channel 4 - 7 Mask Register Clear
	R	Reserved
00DD	W/R	Reserved
00DE	W	Channel 4 - 7 All Mask Register Bits Write
	R	Reserved
00DF	W/R	Reserved

EXTENDED MODE

In the extended mode, two addresses are used to access all registers and bits. The first address (0018), known as the Extended Function Register, serves as a pointer to the desired channel register or bit and identifies the function to be performed. The second address (001A) is used to pass data, if required. Refer to the Function Register description above for details on the function codes.

AUTOINITIALIZATION

The DMA Controller autoinitialization feature allows the programmer to reduce the overhead associated with setup for DMA transfers by automatically initializing the current Memory Address register and the Transfer Count register with the values in their corresponding base registers after completion of a DMA transfer. To do this, the autoinitialization bit is set in the Mode register.

ARBITRATION

Arbitration of the contention for access to the Micro Channel bus consists of allowing all master or slave devices requesting access to issue their requests in parallel and then selecting the device with the highest priority to perform its transfer. The sequence is:

1. A device requests access by pulling the PREEMPTIN line low.
2. The DMA Controller begins the arbitration cycle by pulling /GRANT high.
3. The DMA Controller requests access to the Private Bus from the CPU by pulling the HOLDR line high.
4a. The CPU completes its current cycle and releases the bus, signalling the DMA controller by pulling the HOLDA line high.
4b. At the same time, all devices requesting service drive the Arbitration bus with their priority code. They adjust until the code on the bus matches the code of the device with the highest priority (lowest number).
5. After allowing time for the Arbitration bus to stabilize, the DMA Controller pulls the /GRANT signal low to lock in the code of the device to be serviced. This signals the winning device that DMA transfer may begin.

FLOPPY DISK ARBITRATION

The system board floppy disk controller notifies the DMA controller chip that it is ready to perform a DMA transfer by asserting FDREQ. The DMA controller then sets /FDPRMT to request access to the Micro Channel bus. During the ensuing arbitration cycle the DMA controller competes for the bus by driving FDARB0 and FDARB23 if the mask bit for channel 2 is not set (i.e. DMA is enabled for that channel). Arbitration attempts continue until channel 2 wins an arbitration cycle. Then the DMA controller asserts /FDACK and proceeds to do a non-bursting transfer for the floppy controller.

DRAM REFRESH LOGIC

DRAM refresh is controlled by the DMA Controller. This is performed as if it were a request from a peripheral device for DMA service. The sequence is:

1. The refresh timer generates a request for refresh every 15 microseconds.

2. The DMA Controller generates a PREEMPT and waits for the end of transfer.

3. The DMA Controller generates an arbitration cycle. The refresh request automatically wins access. The Grant mode is not entered.

4. The refresh address is transferred to the address bus and /REFRESH, MEM and STATUS signals are issued.

5. The DMA controller completes the refresh cycle and returns control of the system either to the CPU or to a device on the channel if a preempt was active.

NUMERIC COPROCESSOR INTERFACE

The 80387 and 80287 Numeric Coprocessors require some support logic to operate in the system. The DMA Controller has this circuitry included.

Address Decoding and Bus Timing: The Numeric Coprocessor is located at I/O addresses 00FXH. The Chip Select (/NCPCS) and Busy (/CPUBUSY) signals are generated to handshake with the Bus Controller.

Error Processing: The DMA Controller uses the Numeric Coprocessor error signal (/NPERROR) signal to generate the coprocessor error interrupt (/IRQ13).

Reset: The DMA Controller uses the system reset signal (/RESET) or the I/O write to 00F0 (software reset) to provide the Numeric Coprocessor reset signal (NPRESET).

TIMING

Two timing diagrams are shown. The first of these, Figure 3.4 is an illustration of a typical DMA cycle. Notice that the CHRDYRTN is not shown. It is assumed to not go inactive, i.e. Micro Channel cycles of minimum duration are shown.

The second timing diagram shows the acquisition of the bus by the CPU after it has been dedicated to some other device. The same diagram shows the subsequent acquisition of the bus by some other device other than the system CPU. In the first sequence, note that there is no activity on the PREEMPTIN line since the CPU gains the bus only by default since it is lowest priority. There must be no other claim on the bus. There is a logical ANDing between the /CCMD and /BURST Micro Channel signals going to an inactive level. When this logical condition is met and the required setup time to the rising edge of PROCLK is also met, the Central Arbitration Point causes GRANT to go inactive (causing an arbitration cycle to occur).

When the bus is subsequently acquired by some other bus master, the potential bus master activates the PREEMPTIN line to begin the arbitration cycle. Once the arbitration is complete, the HOLDR line is asserted. The CPU responds by asserting the HOLDA at the next instruction boundary and floating all of the output lines with the exception of the HOLDA.

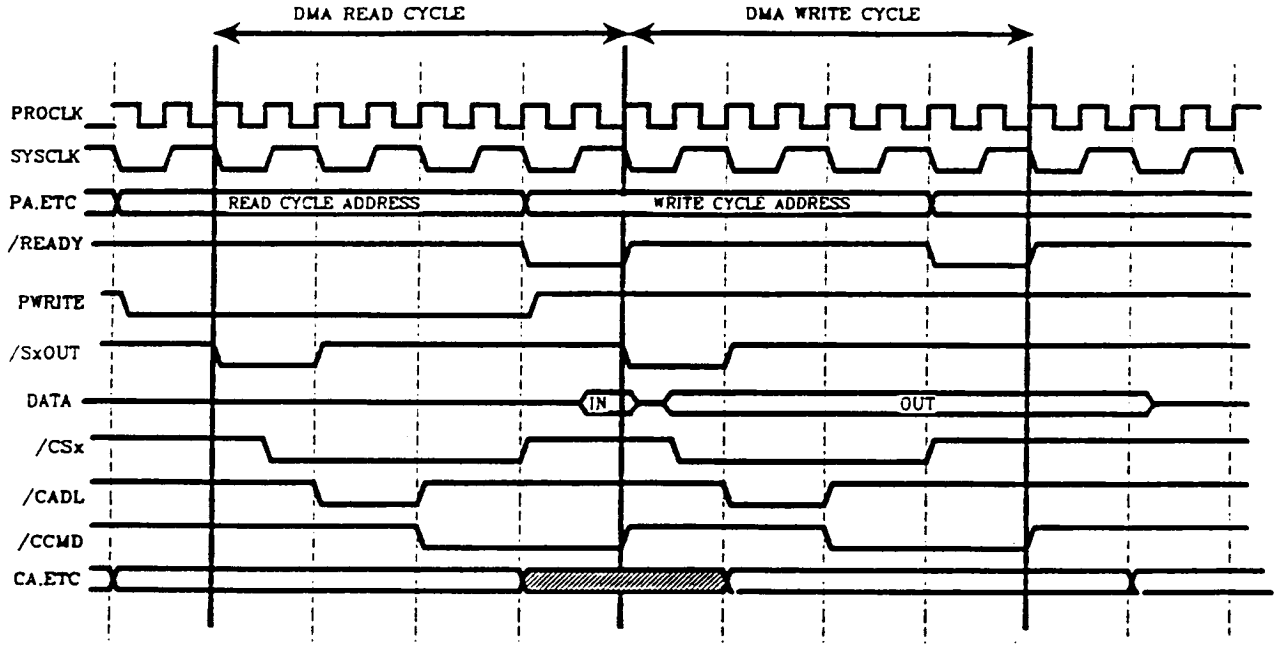


Figure 3.4 - Typical DMA Cycles

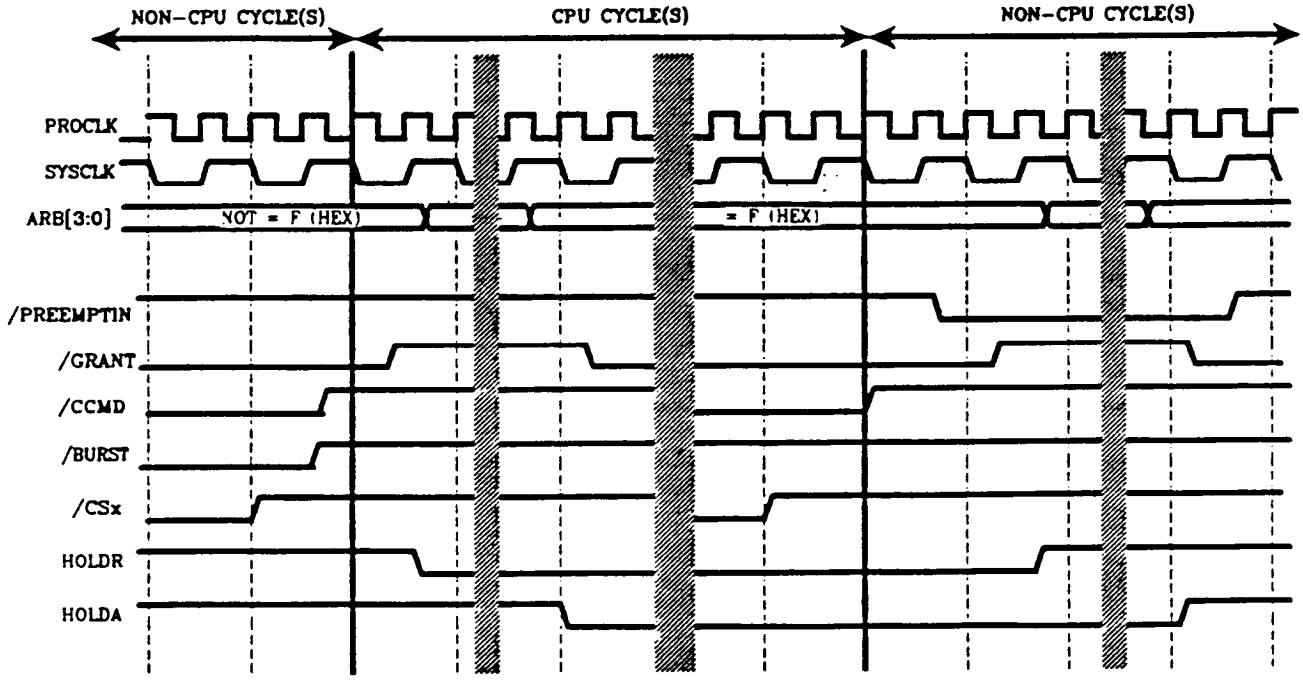


Figure 3.5 - Bus Arbitration Sequences

GC183 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vcc	Supply Voltage	-	7.0	V
Vi	Input Voltage	-0.5	5.5	V
Vo	Output Voltage	-0.5	5.5	V
Top	Operating Temperature	-25	85	C
Tstg	Storage Temperature	-40	125	C

GC183 Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vcc	Supply Voltage	4.75	5.25	V
Ta	Ambient Temperature	0	70	V

GC183 DC Characteristics

Symbol	Parameter	Min	Max	Unit	Conditions	Notes
VIL	Input Low Voltage	VSS	0.8	V	4.75<VDD<5.25	
VIH	Input High Voltage	2.0	VDD	V	4.75<VDD<5.25	
IIL	Input Low Current	-10.0	-	uA	VIN=VSS	
IIH	Input High Current	-	10.0	uA	VIN=VDD	
IILP	I/O with Internal Pull Up	-90	-10	uA	VIN=0.00V	/NMI
IIHP	I/O with Internal Pull Up	N/A	40.0	uA	VIN=VDD	
VOL	Output Low Voltage	VSS	0.4	V	0.0mA<IOL<4.0mA	
VOH	Ouput High Voltage	2.4	VDD	V	-4.0<IOH<-0.0mA	
IOH	Output High Current	-10.0	-80.0	mA	VO=VDD	
IOL	Output Low Current	20.0	110.0	mA	VO=VSS	
IOZL	Output Leakage Current/Low	-10.0	-	uA	VO=VDD	Tri-State (high impedance output)
IOZH	Output Leakage Current/High	-	10.0	uA	VO=VSS	

AC Parameters and Reference Timing Diagrams this page

Pin Symbol	Pin Numbers	Pin Type	Description
CPU AND BUS CONTROLLER INTERFACE			
A20-A23	73-76	O	Address lines 1 and 16 through 23. These are active high, three state outputs used to address the memory and I/O. Note that Address Bit 1 and Address bits 16-23 are not used are not used as inputs to the DMA Controller.
A16-A19	68-71	O	
A12-A15	63-66	IO	
A11	61	IO	
A8-A10	55-57	IO	
A5-A7	50-53	IO	
A2-A4	47-48	IO	
A1	44	O	
/BE0	45	O	Byte Enable 0. A three state, active low signal by the DMA Controller to address I/O and memory.
/BE1	46	O	Byte Enable 1. A three state, active low signal used by the DMA Controller to address I/O and memory.

/BE0 and /BE1 identify the location of the bytes of data on the bus as follows:

/BE0	/BE1	Bits	Location
0	1	8	0 - 7
1	0	8	8-15
0	0	16	0-15
1	1	not used	

/BUSY	32	O	DMA Busy. An active low output which tells the Bus Controller that a DMA transfer or refresh cycle is in progress.
/DMAADL	37	I	DMA Address Latch. An active low input used to qualify data on the address bus.

Pin Symbol	Pin Numbers	Pin Type	Description
/CB0E	114	I	Channel Byte 0 Enable. An active low input from the channel, similar to /BE0 above. This signal is used to address the DMA Controller in the program mode.
/CWLE	113	I	Channel Word Low Enable. An active low input used to steer bytes of data. This signal is used to address the DMA Controller in the program mode.
/CCMD	122	I	Channel Command. An active low input used to qualify data on the data bus.
CMEM	118	I	Channel Memory / -I/O. An active high input used to differentiate between Memory (high) and I/O (low) operations.
/CS0	117	I	Channel Status Bit 0. An active low input used to differentiate between I/O and Memory writes and reads .
/CS1	116	I	Channel Status Bit 1. An active low input used to differentiate between I/O and Memory writes and reads.

/CS0, /CS1, and CMEM are interpreted as follows:

CMEM	/CS0	/CS1	Operation
0	0	1	I/O Write
0	1	0	I/O Read
1	0	1	Memory Write
1	1	0	Memory Read
1	0	0	Interrupt Acknoledge

/S0OUT	81	O	DMA cycle status bit 0. Indicates the type of cycle required by the DMA. The interpretation of the combination of this bit , /S1OUT and PMEM is identical to the table above for /CSO,/CS1 and CMEM
/S1OUT	79	O	DMA cycle status bit 1.
/DMACS	97	O	DMA Chip Select. An active low output which indicates that the DMA Controller is responding to a command directed to it. This signal is used by the Bus Controller to control the bus drivers to properly direct the data bus signals
/GCSENA	78	I	Global chip select enable. Active low signal which enables the internal address decode for access to internal registers. Normally tied to the system processor HLDA.

Pin Symbol	Pin Numbers	Pin Type	Description
HOLDA	31	I	Hold Acknowledge. An active high input driven by the CPU to indicate that the processor has relinquished the bus.
HOLDR	30	O	Hold Request. An active high output used to request that the CPU enter its hold condition.
D0	128	IO	Data Bus. Bi-directional, three-state.
D1-D3	129-131	IO	
D4-D7	133-136	IO	
D8	140	IO	
D9-D12	144-147	IO	
D13-D15	149-151	IO	
/NMI	34	IO	Non-maskable Interrupt. A bi-directional, three-state signal used in an open collector configuration. This signal is generated by the DMA Controller at the end of an arbitration bus time-out to indicate an error on the bus. As an input, this signal forces the central arbitration control point into the arbitration mode.
PMEM	111	IO	Processor Memory / - I/O. This three-state signal idicates whether the current DMA cycle is a Memory (high) or I/O (low) operation. It is provided by the DMA Controller during DMA transfers.
/READY	36	I	Ready. An active low input. It is driven high by the Bus Controller to indicate the end of the current cycle
MICRO CHANNEL INTERFACE			
ARB0-3	94-91	I	Arbitration Bus. These input lines are driven low with the priority level of the arbitrating bus participants.
FDARB0	21	O	Floppy disk arbitration bit 0. The chip drives this line when the floppy disk has a request pending and it is arbitrating for the floppy. This line must be buffered externally to drive the arbitration bus line.
FLARB23	124	O	Floppy disk arbitration bits 2 and 3. The chip drives this line when the floppy disk has a request pending and it is arbitrating for the floppy. This line must be buffered externally through two separate drivers to drive the arbitration bus lines.

Pin Symbol	Pin Numbers	Pin Type	Description
FDREQ	99	I	Floppy disk request. Request for DMA service from the system board floppy disk controller.
/FDACK	100	O	Floppy disk acknowledge. Indicates a grant of the DMA service request to the system board floppy disk controller.
/BURST	89	I	Burst. This active low input indicates that the winner of the arbitration is requesting operation in the burst mode.
/BUSTO	6	O	Bus Time-out. An active low output which indicates an arbitration time-out has occurred. This signal is provided for development use only - there is no system application. It must not be connected to an input or voltage.
/GRANT	88	O	Grant. An active low output indicating the end of an arbitration cycle and authorizing the winning DMA device to begin its DMA cycle.
/PREEMPTIN	126	I	Preempt Input. This active low input is driven by any bus participant to request use of the DMA channel.
/PREEMPT	87	O	Preempt. An active low output indicating a bus arbitration request generated within the DMA Controller. The source of this signal is a refresh request.
/FDPRE	22	O	Floppy disk preempt request. Generated when the system board floppy disk controller has a DMA request pending and the bus is in use. Must be buffered externally and tied to the Micro Channel PREEMPT line.
/TC	85	O	Terminal Count. An active low output indicating that the transfer count of the current DMA transfer has reached zero.
NUMERIC COPROCESSOR INTERFACE			
RDY387	121	O	Ready signal from an installed 80387 to provide a means to insert wait states if required.
/BUSY386	159	O	Provides busy indication to the 80386 processor if required.
/CPUBUSY	157	O	CPU Busy. An active low output from the DMA Controller indicating that the Numeric Coprocessor is busy.
/IRQ13	153	O	Interrupt Request 13. An active low output indicating an error in the Numeric Coprocessor.

Pin Symbol	Pin Numbers	Pin Type	Description
/NCPBUSY	155	I	Numeric Coprocessor Busy. An active low input signal from the Numeric Coprocessor that it is busy with a current operation.
/NCPCS	96	O	Numeric Coprocessor Chip Select. An active low output which indicates that the Numeric Coprocessor has responded to a command addressed to it. This signal is used by the Bus Controller to control the bus drivers to properly direct the bus signals and to avoid bus contentions.
/NCPERR	156	I	Numeric Coprocessor Error. An active low input signalling an error condition in the Numeric Coprocessor.
NCPRST	154	O	Numeric Coprocessor Reset. An active low output which forces an 80287 Numeric Coprocessor to reset. (Note that different reset timing is required for an 80387).
RST387	1	O	Numeric Coprocessor Reset. An active low output which forces an 80387 Numeric Coprocessor to reset. (Note that different reset timing is required for an 80287).
STEN387	119	O	Status enable for an 80387. Enables the status output pins on the numeric coprocessor.
OTHER			
/REFRESH	138	O	Refresh. An active low output signal indicating that a refresh operation is in progress.
CLK119M	83	I	1.19 MHz Clock. Used for Refresh Timing.
CLKPRO	102	I	CPU Clock.
CLKSYS	107	I	System Clock.
/FASTREF	82	I	Fast Refresh. An active low input used to select the fast refresh rate.
INTR	35		Interrupt Request. This active high input signal is used to indicate the presence of any interrupt. This signal is the OR of all interrupt requests.
MASK2	84	O	Mask Register bit 2. This active high output indicates that the mask bit for channel 2 is set. This signal may be used by external logic to disable the arbitration for this channel when the mask bit is set. There is no system application. This pin must not be connected to a voltage or another output.

Pin Symbol	Pin Numbers	Pin Type	Description
/RESET	29	I	System Reset. Active low.
/REQRST	125	I	Request reset. This is a composite signal from the system board for requesting a reset of the system board processor.
/RSTPRO	104	O	Reset processor. This signal is caused by the presence of a /RSTPRO input and the fact that a DMA cycle is not in progress. It assures that partial DMA cycles (and therefore unrecoverable data error conditions) do not occur during a processor reset sequence.
PRORST	58	I	Processor reset. Inhibits initiation of a DMA cycle is a processor reset sequence is in progress.
DIAGNOSTICS/TEST			
/GBURST	90	O	A test point which shows the burst timing within the chip.
/MBURST	105	O	The test point which shows the implied burst timing between a read and write cycle pair which are required to accomplish a DMA cycle.
DOREF	3	O	Test pin that indicates that a refresh is in progress for arbitration test purposes.
/REFREQ	4	I/O	Test point to request refresh from external source. No connection for normal system operation.
DIS100ARB	123	I	Disables the 100 nanosecond arbitration period option if pulled high. Tie high for normal operation.
ENREFRSH	143	I	Enables the internal refresh arbitration circuitry. Provided as a system diagnostic function. Tie high for normal operation.
ENGBURST	142	I	Enables the internal burst mode operation of the microchannel. Provided as a system diagnostic feature. Tie high for normal operation
ENCAP	42	I	Enable central arbitration point. Test and diagnostic input which enables the central arbitration function in the chip. Tie high for normal operation.
ENEOT	38	I	Enable End of Transfer. Enables the EOT output pin if in the high state. This pin is a test and diagnostic aid and must be tied high in the system.
EOT	5	O	Indicates and end of transfer condition which allows arbitration to proceed.

Pin Symbol	Pin Numbers	Pin Type	Description
DIS78BTO	109	I	Disable 7.8 microsecond bus timeout. Disables the specified bus timeout for test and diagnostic purposes. Must be tied high in the system.
/DLYGNT	59	I	Delay grant. If low the grant for a bus access will be delayed during the arbitration sequence. Must be tied high in the system.
/TEST	24	I	Chip test signal. Not used in the system. Must be left unconnected.
T0,T1,T3,T4,T5	27-25,39,41	I	Test inputs. Not used in the system. Connect as shown below.

Input	Function	Usage
T0	No system function	Must be tied high or low
T1	No system function	Must be tied high.
T3	Enhanced 16 Bit Odd Byte Transfer	Tie High
T4	No system function	Must be tied low.
T5	Enable Fast DMA Startup	Tie High

DIAG0-7	19-16,14-11	O	Diagnostic outputs. Must be tied high or grounded.
DIAGIN0-3	9-7	I	Diagnostic test inputs. Must be tied high or grounded in the system.
PAROUT	28	O	Parametric test output. Only for use in manufacturing. Must be unconnected.

MISCELLANEOUS

VDD	23,40,49,62,72, 80,95,120	I	Power
VSS	2,10,15,20,33,43, 54,60,67,7786,98, 101,103,106,108, 115	I	Ground

FEATURES

- 15 Level Triggered Interrupts
- 3 Programmable Timers
- Refresh Rate Counter
- Parallel Port
- System Board Option Configuration
- System Board Peripheral Device Address Decodes

OVERVIEW

The GC186 Peripheral Controller provides the essential support for the standard I/O devices in a PS/2 compatible computer. The use of level sensitive interrupts facilitates interrupt sharing by adapters as well as reducing transient sensitivity of the interrupt mechanism. In addition to the system timer and audio timer common with the AT architecture, there is an additional timer used as a system Watchdog timer. The refresh rate counter provides a refresh request about every 15 microseconds. The parallel port is an integration within the chip of the standard parallel port as found in the AT world. The option configuration controls contained within the chip enable or disable various system board functions. In addition, they provide miscellaneous control functions such as controlling disk drive activity lights or providing a programmed reset capability for the system processor. Address decodes are provided for a variety of system board resident I/O devices including serial ports, floppy disk controller, keyboard controller and the real-time clock and associated CMOS RAM.

BLOCK DIAGRAM

The block diagram of the chip is shown in Figure 4.1. The interrupt control consists of two 8259 equivalent interrupt control chips. Interrupt 2 of the primary interrupt controller is used as the cascade interrupt input for the second interrupt controller. Internal logic within the GC186 chip prevents the controllers from being set to edge-triggered mode.

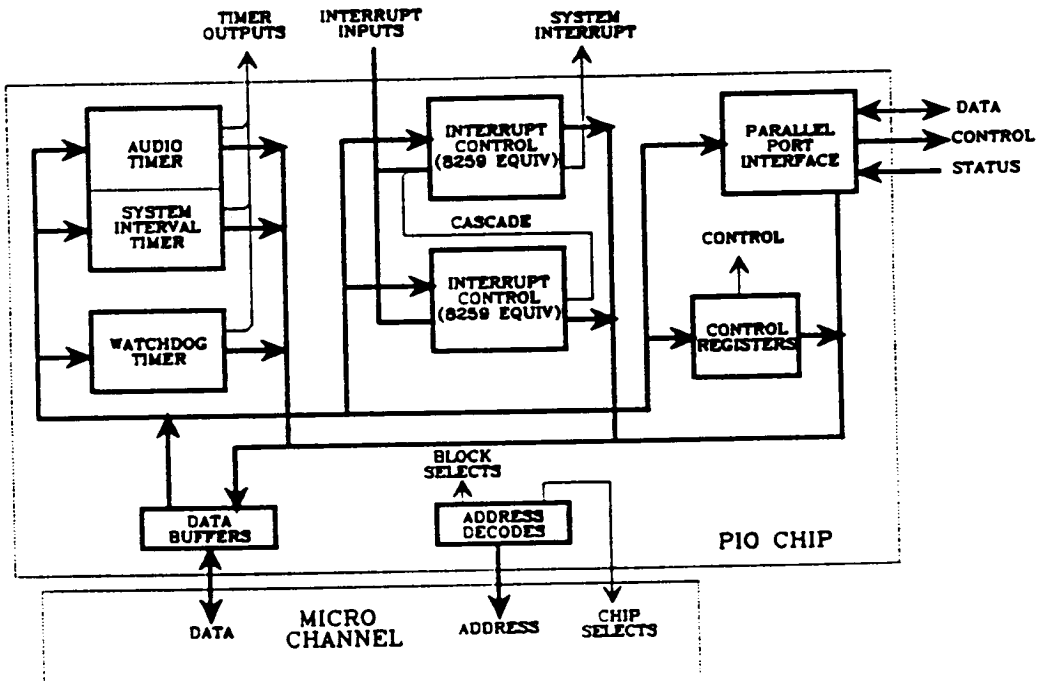


Figure 4.1 - PIO Block Diagram

Two of the timers (0 and 2) are 16 bit presetable down counters which can count in either binary or BCD. Counter 3 is only 8 bits, can be preset, and counts only in binary.

The address decodes take advantage of the availability of address bits and timing signals which are required to select various portions within the chip and develop chip decodes for other peripheral devices within the system. The access decode for the keyboard control provides a special feature which provides the necessary recovery time for accesses to the keyboard controller. This eliminates the necessity of embedding this recovery time requirement within code which deals with the keyboard.

The parallel port is a standard PC parallel port in terms of functionality. The I/O addresses at which the port registers reside are programmed to one of three different ranges to conform with previous generations of personal computers.

There are various control registers contained within the chip which provide controls for the various device blocks within the chip itself and provide support for other devices contained within the system. This allows considerable flexibility in configuring a system including the ability to substitute adapters for system board peripherals if desired.

SYSTEM CONFIGURATION

The Peripheral Controller is configured into the system by interfacing to the Micro Channel bus. It consists largely of programmable registers and counters that receive their data over this bus. During initialization and normal operation, the CPU reads and writes to any one of several I/O Port addresses that are contained within the device. Addressable functions are: interrupt control, programmable counters, option configuration (POS), refresh rate counter, Parallel Port control, and address decoding for several I/O Ports.

When the CPU programs the Peripheral Controller, the CPU treats it like an 8 bit I/O device on the MicroChannel bus. Register I/O addresses and their respective functions including programming information are contained in the next section.

REGISTERS

The accessable portions of the circuit are represented by a set of ports addressable by I/O commands. These are scattered throughout the range of 0020H through 03FFH. The map of ports is as follows:

Address	Function
0020-0021	Interrupt Controller 1
0040, 0042, 0043	Counter Preset Ports
0044, 0047	Counter Control Ports
0061	System Port B
0070	NMI Mask
0091	Feedback Port
0092	System Port A
0094	POS System setup controls
0096	POS Adapter setup controls
00A0 - 00A1	Interrupt Controller 2
0102	System configuration options
0103	Memory configuration options
0278 - 027B	Parallel Port Address Decodes
0378 - 037B	
03BC - 03BF	
02F8 - 02FF	Serial Port Address Decode
03F8 - 03FF	
03F0 - 03F7	Floppy Disk Address Decode

INTERRUPTS

The GC186 provides normal and non-maskable interrut control for the system. The normal interrupts are always level sensitive both to facilitate interrupt sharing and to reduce noise sensitivity of the interrupt mechanism. The interrupt are implemented to function identically to two Intel 8259 Interrupt Controllers with one of the controllers cascaded from IRQ2 on the master controller. Special logic within the chip inhibits the programming of the interrupt sensitivity to edge trigger mode. The addresses for the master interrupt controller are at 20 and 21 Hex and for the slave are at A0 and A1. The interrupt assignments for a compatible system are shown below. NMI is the highest priority.

Interrupt Level Priorities

Level	Function
NMI	Parity,Watchdog Timer, Arb Timout, Channel Check
IRQ0	System Timer Tic
IRQ1	Keyboard
IRQ2	Cascade Interrupt Input
IRQ3	Serial Alternate
IRQ4	Serial Primary
IRQ5	Reserved
IRQ6	Floppy Disk
IRQ7	Parallel Port
IRQ8	Real-Time Clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Mouse
IRQ13	Math Coprocessor Exception
IRQ14	Fixed Disk
IRQ15	Reserved

TIMERS

Three programmable timers are included in the chip. Timers 0 and 2 are 16 bit counters similar in function to those contained in an Intel 8254. Counter 0 is dedicated to the function of system timer. The gate to this timer is always enabled, the clock is driven by the CLK1M input (1.19 MHz) and the clock out produces IRQ0 within the chip. Counting modes 1 and 5 are invalid for this counter and system operation is not predictable if any mode other than 2 or 3 is defined for this counter. Counter 2 is dedicated as the tone generator for the speaker in the computer system. The gate is controlled by bit 0 of I/O port 61 (hex), the clock is driven by CLK1M and the output, after being gated by a control bit, exits the chip as the signal AUDIO. Counter 3 is an 8 bit counter which operates in mode 0 only. The gate is tied internally to IRQ0, the clock comes from the output of counter 0 and the output causes an NMI. The effect is to cause an NMI if the system timer is not recieving interrupt service within the number of timer ticks programmed into the counter. This timer can only be programmed in mode 0.

The programming for timers 0 and 2 use addresses 0040, 0042, and 0043. Timer 3 uses addresses 0044 and 0047. Addresses 0040, 0042, and 0044 contain the counters for timers 0, 2, and 3 respectively. Address 0043 is used to control timers 0 and 2. Address 0047 controls timer 3. For Timers 0 and 2, a byte pointer in the control logic selects bits 0 - 7, or bits 8 - 15, so only a single address is required for access to each timer.

Ports 40, 42 and 44 are the ports for writing a preset count to counter 0, 2 and 3 respectively.

The write-only control byte at address 43 hex which controls counters 0 and 2 is as follows:

Counter Control Bit Assignments
Port 43 Hex

Bits	Label	Function
7,6	SC1,SC0	Counter Select
	0 0	Select Counter 0
	0 1	Reserved
	1 0	Select Counter 2
	1 1	Reserved
5,4	RW1,RW0	Byte Pointer setup
	0 0	Counter Latch Command
	0 1	Select Coutner bits 0 - 7
	1 0	Select Counter bits 8 - 15
	1 1	Select Counter bits 0 - 7 first, then bits 8 - 15
3-1	M2-M0	Mode
	0 0 0 Mode 0	Interrupt on Terminal Count
	0 0 1 Mode 1	Retriggerable One Shot
	0 1 0 Mode 2	Rate Generator
	0 1 1 Mode 3	Square Wave
	1 0 0 Mode 4	Software Retriggerable Strobe
	1 0 1 Mode 5	Hdwr Retriggerable Strobe
0	BCD	0 = Binary count 1 = BCD count

Port 47 Hex is a write-only control port for counter 3. It's bits are defined as follows:

Counter Control Bit Assignments
Port 47 Hex

Bits	Label	Function
7,6	SC1,SC0	Counter Select
	0 0	Select Counter 3
	0 1	Reserved
	1 x	Reserved
5,4	RW1,RW0	Byte Pointer setup
	0 0	Counter Latch Command
	0 1	Select Coutner bits 0 - 7
	1 x	Reserved
3-0	Must be = 0	

SYSTEM BOARD SETUP

Two register addresses are used for setup operations for the system board peripherals. Register 94 Hex enables or disables the system board or VGA setup. The bit assignments of this register are shown below.

System Ports (0061H, 0091H, 0092H, 0094H, 0096H, 0102H and 0103H: The bits at this address are an interface to signals in the system. They are represented as follows:

System Board Setup Enable Register
Port 94 Hex

Bit	Rd/Wr	Function
7	W/R	System Board + Ena/-Setup
6	W/R	Reserved
5	W/R	VGA + En/-Setup
4-0	W/R	Reserved

When bit 7 of Port 94 is set to enable system board setup (set to zero), port 102 Hex controls the state of the system board peripheral devices with the exception of the VGA. The definitions of this port are given below.

System Board I/O Port Control
Port 0102 Hex

Bit	Rd/Wr	Function
7	R/W	Enable extended parallel port
6	R/W	Parallel port select (high)
5	R/W	Parallel port select (low)
4	R/W	Enable system board parallel port
3	R/W	Serial port select
2	R/W	Enable system board serial port
1	R/W	Enable system board floppy disk
0	R/W	Enable system board devices

Note: Bit 3 selects the serial port as port 2 if at zero or to be port 1 if at a one.

PROGRAMMABLE OPTION SELECT

Two ports in the GC186 provide support for the Programmable Option Select function of Micro Channel Architecture machines. Port 96 provides a card selection code and selection enable to select one of 8 adapter cards within a system.

Channel Position Select Register
Port 0096 Hex

Bit	Rd/Wr	Function
7	W/R	Channel reset
6-4	W/R	Reserved
3	W/R	Card select enable
2-0	W/R	Card select bits 2 - 0

Port 91 gives a single bit of indication that a card has been selected.

Card Select Feedback Byte
Port 0091 Hex

Bit	Rd/Wr	Function
0	R	Channel select feedback

MEMORY CONTROL REGISTER

There is a port at address 103 which controls the refresh rate to the memory and the enabling of system board RAM memory. When this port is accessed, the port at address 96 must have bit seven set to a zero to avoid the possibility of selecting one of the adapter cards.

Memory Control Register
Port 0103 Hex (Write Only)

Bit	Function
7-2	Reserved
1	Fast refresh
0	System RAM enable

PARALLEL PORT

The parallel port is compatible with previous PC implementations and at the same time supports an extended mode. This extended mode supports bidirectional data transfers. The parallel port address space has been assigned to three spaces, 0278 - 027B, 0378 - 037B, and 03BC - 03BF to conform to previous versions of personal computers. These address ranges are the address assignments for parallel ports 1 2 or 3 respectively. The address set used is defined by bits 6 and 5 of the register at address 0102. The assignments are as follows:

Parallel Port Assignment

Bit6	Bit5	Data	Status	Ctl
0	0	03BC	03BD	03BE
0	1	0378	0379	037A
1	0	0278	0279	027A
1	1		Undefined	

The data port is a write only port in the compatibility mode. Any reads to the port read back the last data written. In the extended mode, data written to this mode is latched, but is not output to the external world unless the direction control in the control port is set to Write. A read operation to this port in the extended mode yields the most recently written data if the direction control is set to Write. Otherwise the data will be data from an external source placed on the parallel port.

The parallel port includes a Read-Only status port for reading the status of the device attached to the port. The bit assignments for this location are defined below.

Parallel Port Status Bit Assignments

Bit	Name	Function
7	-Busy	0 = Busy, not ready to accept data 1 = Ready to accept data
6	ACK	0 = Peripheral waiting for character
5	PE	0 = Normal operation 1 = Peripheral not ready (out of paper)
4	Select	0 = Peripheral not selected 1 = Peripheral selected
3	-Error	0 = Peripheral error condition 1 = Normal operation
2	IRQ Stat	Used to acknowledge previous transfer
1-0		Reserved

The control byte for the parallel port is a byte wide read and write I/O port. A write to this port latches the least significant 6 bits of the byte written. Only bit 5, the Direction Control bit differs from the control bit assignments for previous versions of the parallel port. These bit assignments are shown in the following table.

Parallel Port Control Bit Assignments

Bit	Name	Function
7-6	Reserved	
5	Direction	0 = Write for extended mode
		1 = Read for extended mode
4	IRQ Enable	0 = No interrupt on ack
		1 = Interrupt when ack inactive
3	Select	1 = Select port device
2	-Initialize	0 = Initialize port device
1	Auto feed	0 = No automatic line feed
		1 = Automatic line feed
0	Strobe	1 = "Clock" data to port device

RT CLOCK, CMOS RAM AND NMI MASK

The register at address 70 Hex contains the NMI mask bit as well as the address for the Real-time clock/CMOS RAM. Bit 7 of this register is the mask for NMI interrupts. Writing a 1 to this bit inhibits interrupts due toa memory parity error or a channel check. The mask bit does not inhibit interrupts due to the Watchdog timer or system channel time-out. The least significant 5 bits of this register provide the address for the Real-time clock and CMOS RAM.

Note: A write to this port must be followed immediately by a read from address 0071 to ensure proper operation of the real-time clock.

Additional I/O port provide data for addresses for the 2K of nonvolatile RAM extension and a byte wide data path to that RAM. A summary of the ports for support of these timer and RAM areas is given below.

RT/CMOS RAM SUPPORT ADDRESSES

Address	Function
0070	Real time clock address
0071	Real time clock data
0074	RAM address (lower)
0075	RAM address (upper)
0076	Ram data

MISCELLANEOUS SYSTEM PORTS

The I/O location at 92 Hex provides a variety of control and status information for the system as described below.

System Control Port A
Port 0092 Hex

Bit	Rd/Wr	Function
7	W/R	Light A
6	W/R	Light B
5	W/R	Reserved
4	R	Watchdog timeout
3	W/R	Password lock
2	W/R	Reserved
1	W/R	A20 gate
0	W/R	Alternate processor reset

The byte at port 61 Hex provides various control and status information for the system board as shown below

System Control Port B
Port 0061 Hex

Bit	Rd/Wr	Function
7	W	Clear interrupt 0
	R	Memory parity check
6	W	Reserved
	R	I/O channel check
5	W	Reserved
	R	Timer 2 output
4	W	Reserved
	R	Refresh detect
3	W/R	I/O check enable not
2	W/R	Memory parity check enable not
1	W/R	Speaker enable
0	W/R	Timer 2 gate

ADDRESS DECODES

A number of peripheral device addresses and address ranges are decoded by the GC186 chip. This takes advantage of the address decode signals which must be available to the chip and provides for an effective system design. The decoded addresses are given below.

System Board Address Decodes

Address	Function
0060,64	Keyboard
0070-76	Real time clock/CMOS RAM
0103	RAM configuration
0278-27B	Parallel port
02F8-2FF	Serial Port 1
03F8-3FF	Floppy disk

GC186 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vcc	Supply Voltage	-	7.0	V
Vi	Input Voltage	-0.5	5.5	V
Vo	Output Voltage	-0.5	5.5	V
Top	Operating Temperature	-25	85	C
Tstg	Storage Temperature	-40	125	C

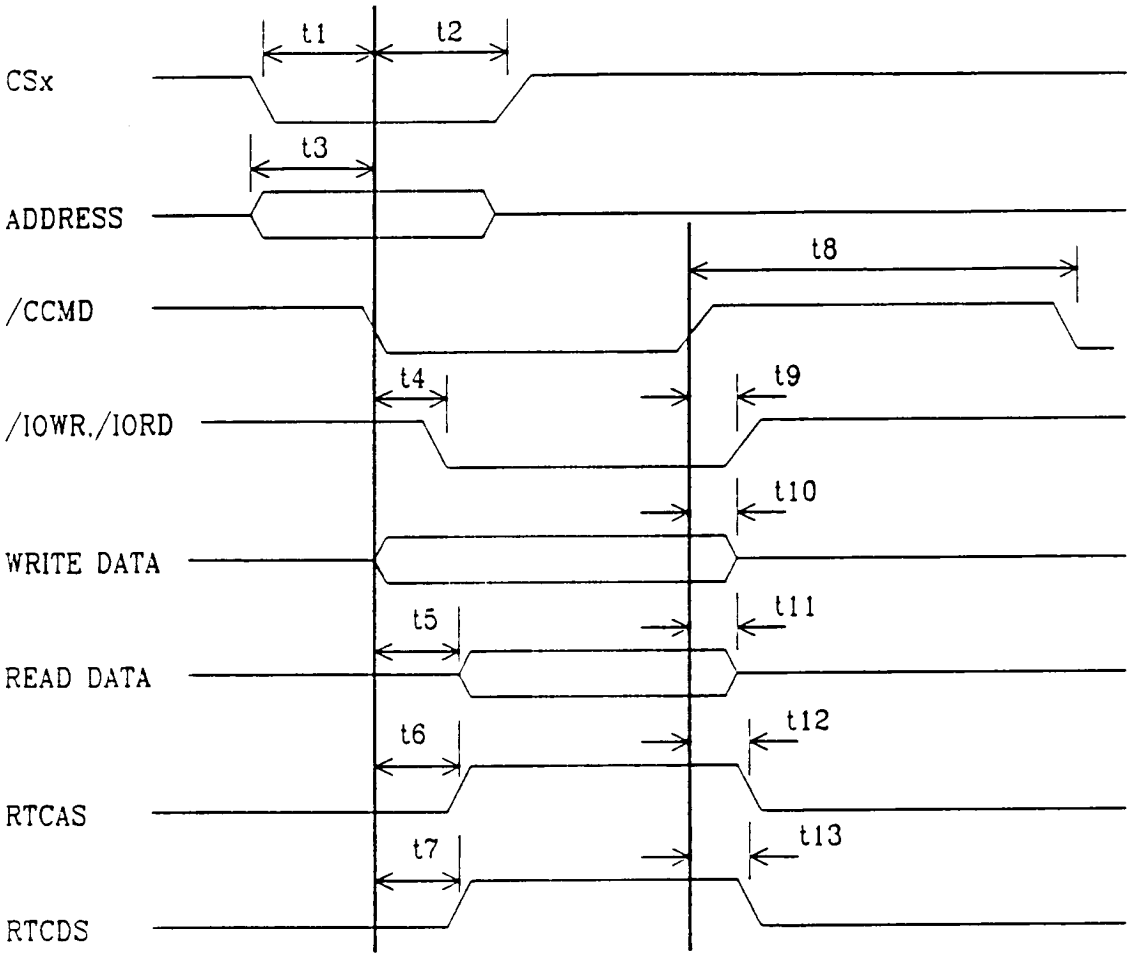
GC186 Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vcc	Supply Voltage	4.75	5.25	V
Ta	Ambient Temperature	0	70	V

GC186 DC Characteristics

Symbol	Parameter	Min	Max	Unit	Conditions	Notes
VIL	Input Low Voltage	VSS	0.8	V	4.75<VDD<5.25	
VIH	Input High Voltage	2.0	VDD	V	4.75<VDD<5.25	
IIL	Input Low Current	-10.0	-	uA	VIN=VSS	
IIH	Input High Current	-	10.0	uA	VIN=VDD	
VOL2	Output Low Voltage - Buffer	VSS	0.4	V	0.0<IOH<8.0ma	PPO-7, CDO-7 ,RD0076, /LITEA
VOH2	Output High Voltage - Buffer	2.4	VDD	V	-8.0<IOL<0.0 ma	LITEB, /IORD, /IOWR
VOL	Output Low Voltage - Normal	VSS	0.4	V	0.0<IOL<4.0mA	All other outputs
VOH	Ouput High Voltage - Normal	2.4	VDD	V	-4.0<IOH<-0.0mA	
IOH	Output High Current	-10.0	-80.0	mA	VO=VDD	
IOL	Output Low Current	20.0	110.0	mA	VO=VSS	
IOZL	Output Leakage Current/Low	-10.0	-	uA	VO=VDD	Tri-State (high impedance out
IOZH	Output Leakage Current/High	-	10.0	uA	VO=VSS	

/NMI (Pin 58 is an Open Drain Output - It conforms to the normal VOL parameter above



Symbol	Parameter	Min	Max
t1	Status setup to /CCMD active	-	5
t2	Status hold time from /CCMD active	5	-
t3	Address setup to /CCMD active	17	-
t4	/IORD, /IOWR delay from /CCMD active	-	22
t5	Read data access from /CCMD active	-	47
t6	RTCAS delay from /CCMD	-	25
t7	RTCDS delay from /CCMD	-	17
t8	/CCMD recovery time	60	-
t9	/IORD, /IOWR inactive from /CCMD inactive	-	15
t10	WRITE DATA hold time	5	-
t11	READ DATA release time	-	22
t12	RTCAS inactive from /CCMD inactive	-	21
t13	RTCDS inactive from /CCMD inactive	-	21

Pin Symbol	Pin Numbers	Pin Type	Description
CPU AND BUS CONTROLLER INTERFACE			
/ALTRC	28	O	Alternate Processor Reset. This output goes to the Bus Controller to direct that the CPU be reset without resetting the entire system. This signal reflects the status of bit 0 in the register at address 0092H.
HOLDA	73	I	Hold Acknowledge. This input signal from the CPU indicates that the CPU has entered the hold state.
INTR	92	O	Interrupt Request. This active high output signals the CPU that an interrupt is pending.
/NMI	109	O	Non-Maskable Interrupt. This active low output indicates that a non-maskable interrupt is pending.
RAMENA	136	O	RAM Enable. This output signal indicates whether the system RAM should be enabled. The status of this line is indicated in bit 0 of the register at address 0103H.
MICROCHANNEL INTERFACE			
GATEC	70	I	Gate command. Input which is internally ANDed with CMD to generate IOWR. Can be used to delay the leading edge and/or hasten the trailing edge of the IOWR signal if required in the system design.
CA0-CA3	87-90	I	Address Bus. These input signals are the low-order bits of the address bus.
CA4-CA7	111-114	I	
CA8-CA9	127-128	I	
/CAUPPER	129	I	Address Bus Upper Bits. This active low input signal indicates that the address bits CA15 - CA10 are all 0, which is the range for addressing the registers in the Peripheral Controller.
/CCMD	61	I	Channel Command. This active low input signals that the address lines on the MicroChannel are valid and instructs the devices connected to the bus to respond accordingly.
CD0-CD3	27-24	IO	Channel Data Bus. These bi-directional lines are the MicroChannel data bus.

Pin Symbol	Pin Numbers	Pin Type	Description
CD4-CD7	16-13	IO	
/CDRST	51	O	Channel Reset. This active low output signal is used as a reset to the channel.
CDSELFBK	52	I	Card Selected Feedback. This input signal indicates that a memory slave or I/O slave is present at the address output by the system CPU.
/CIOCHK	131	O	I/O Channel Check. This active low output signal is used to indicate a serious system error condition.
CMEM	45	I	Memory / I/O. This input signal indicates whether the current Micro-Channel operation is a memory cycle (set to 1) or an I/O cycle (set to 0).
CS1,CS0	47,46	I	These input signals indicate the status of the current cycle:

CMEM	CS1	CS0	Operation
0	0	0	Interrupt Acknowledge
0	1	0	I/O Write
0	0	1	I/O Read
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Memory Write
1	1	0	Memory Read
1	1	1	Reserved

PERRDY	9	O	Peripheral Controller Ready. This handshaking signal to the Micro-Channel indicates that the Peripheral Controller has accepted the signals sent to it.
/CREFRESH	91	I	Channel refresh. Indicates that a refresh operation is currently under way.
PERIPHERAL INTERFACE			
CDSU2-CDSU0	33-31	O	Card Setup. These signals are used with a 3:8 decoder to select one of eight card slots. The CDSUx lines are the encoded slot number. These lines are copies of the appropriate bits of the register at address 0096H.

Pin Symbol	Pin Numbers	Pin Type	Description
CDSUENA	44	O	This signal indicates the validity of the CDSUx card select lines. It would normally be used to enable the external card selection decoder.
/IORD	149	O	I/O Read. This active low output indicates to the peripheral devices that the current cycle is a read operation.
/IOWR	126	O	I/O Write. This active low output indicates to the peripheral devices that the current cycle is a write operation.
/IRQ0	85	I	Active low interrupt input.
/IRQ1	77	I	Active low interrupt input.
/IRQ3	76	I	Active low interrupt input.
/IRQ4-IRQ7	37-34	I	Active low interrupt inputs.
/IRQ8-IRQ11	7-4	I	Active low interrupt inputs.
/IRQ12-IRQ15	157-154	I	Active low interrupt inputs.
PP0 - PP3	67-64	IO	Parallel Port Interface. These bi-directional lines connect to the parallel (printer) port data lines.
PP4-PP7	57-54	IO	
/PPACK	144	I	Parallel Port Acknowledge. This active low input indicates that the parallel port device has received the last character and is ready to receive another one. This line is read in the parallel port status register at bit 6
/PPAFD	134	IO	Parallel Port Automatic Feed. This bi-directional signal indicates whether a line feed should follow after each carriage return (set to 1). The status of this line is indicated in bit 1 of the parallel port control register.
PPBUSY	145	I	Parallel Port Busy. This active low input indicates that the parallel port is busy. The status of this line is indicated in bit 7 of the parallel port status register.
/PPERR	137	I	Parallel Port Error. This active low input indicates that there is an error condition in the device on the parallel port. The status of this line is indicated in bit 3 of the parallel port status register.

Pin Symbol	Pin Numbers	Pin Type	Description
/PPINIT	135	O	Initialize Parallel Port. When this line is set to 0, the parallel port device is activated. This line is controlled by bit 2 of the parallel port control register.
PPPAEND	143	I	End Of Paper . This input indicates that the printer on the parallel port is out of paper. The status of this line is indicated in bit 5 of the parallel port status register.
/PPSELIN	146	I	Parallel Port Selected. This active low input indicates that the device on the peripheral port acknowledges that it has been selected. The status of this line is indicated in bit 4 of the parallel port status register.
/PPSELO	148	O	Select Parallel Port. This active low output selects the parallel port device. The status of this line is indicated in bit 3 of the parallel port control register.
/PPSTB	132	I	Parallel Port Strobe In. This input indicates the status of PPSTBOUT in bit 0 of the parallel port control register.
PPSTBOUT	48	O	Parallel Port Strobe Out. This active high output "clocks" data to the parallel port.
PARPEN	105	O	Parallel Port Enable. Controls the direction of the external parallel port transciever.
SERPIRQ	138	I	Serial port interrupt request. Programmable inside the chip for the interrupt number.
SERPOUT2	141	I	Gate for the serial port interrupt. Companion signal for the interrupt request from the external USART. Both this signal and the interrupt request must be active to cause an interrupt.
OTHER			
AUDIO	93	O	Audio signal output. This is the output of the audio timer.
CLK1M	130	I	1.19 MHz clock used for internally for the timer tick.
IRQSEL	86	I	Selects either latched or unlatched versions of some of the interrupt lines. Must be pulled high during normal system operation.
MOUSEINT	59	I	Interrupt for the system board supported pointing device. Normally would come from the 8042

Pin Symbol	Pin Numbers	Pin Type	Description
INCDEC	17	I	Incomplete decode. If high allows incomplete decodes of the selected I/O ports in order to allow exact compatibility. If in the low state, forces exact decodes.
/RD0101	8	O	Read port 0101H. Decode of the port address ANDed with the IORD.
/RD0103.	10	O	Read port 0103H. Decode of the port address ANDed with the IORD.
/RD076	12	O	Read port 0103H. Decode of the port address ANDed with the IORD.
WR074	125	O	Write port 0074H. Decode of the port address ANDed with the IOWR. Note that the signal is active high to be used with a latch rather than an edge triggered rgister.
WR075	124	O	Write port 0075H. Decode of the port address ANDed with the IOWR. Note that the signal is active high to be used with a latch rather than an edge triggered rgister.
/WR076	96	O	Write port 0076H. Decode of the port address ANDed with the IOWR.
CLK14M	97	I	14 MHz clock. This input signal drives the internal logic in the circuit.
TIMCLK	98	O	1.19 MHz clock. This is the source for this clock.
SYSTIC	103	O	System timer tic. Goes to interrupt zero.
/SYSRST	133	I	System reset. Resets the chip internals.
/FDACK	30	I	Floppy disk acknowledge. Input which controls the buffer when a DMA cycle for transfer of floppy disk data is in progress.
/DBENA	49	O	Data Bus Enable. This active-low output provides the enable signal to the buffers for the data bus between the Peripheral Controller and the MicroChannel.
DEC010X	11	O	Decode Addresses 010X. This output is asserted when an I/O address in the range 0100H - 0107 is selected. These addresses represent the registers used for the Programmable Option Select (POS).
/FASTREF	151	O	Fast refresh select. Comes from programmable port and goes to the DMA chip to indicate that Fast Refresh mode is active. Causes an 835 ns refresh period rather than the normal 15 microsecond period.
/IOOUT	72	O	Controls system buffer chips when an I/O write cycle is in progress.

Pin Symbol	Pin Numbers	Pin Type	Description
/FDCPCS	94	O	Floppy Disk Select. This output is asserted when an I/O address in the range 03F8H - 03FFH is selected. This address range corresponds to the space for the floppy disk.
/KYBDCS	95	O	Keyboard Select. This output is asserted when an I/O address 0060H or 0064H is selected. These addresses correspond to the space for the keyboard.
CMDDLY	58	O	Output of the delay for the keyboard read. Provides the necessary recovery time for this slow peripheral device. Normally paired with STBDLY input.
STBLY	142	I	Input for the keyboard access recovery time. Normally connected to CMDDLY.
/LITEA,/LITEB	74,75	O	Light Drivers. These active low outputs are used to control the fixed disk activity light drivers. These signals correspond to bits 7 and 4 of the register at address 0092H.
MPCENA	153	O	Memory Parity Check Enable. This output signal indicates that the memory parity check information is to be used.
/MPCK	29	I	Memory Parity Check. This active low input indicates the results of the memory parity check. This signal is a 0 when a memory parity error occurs.
PASSA20	50	O	System Control Port A, bit 1. This bit can be used to control address bit A20.
POSENA	84	O	POS Setup Enable Register Bit 7. This active high output signal is bit 7 of the System Board Setup Enable Register (I/O Address 0094).
RTCAS	116	O	Real-Time CMOS RAM Address Strobe: This output strobes the address to the real-time CMOS RAM.
RTCDS	115	O	Real-Time CMOS RAM Data Strobe: This output strobes data to the real-time CMOS RAM.
RTCRD	117	O	Real-Time CMOS RAM Read/Write. This output signal directs the real-time CMOS RAM data direction during data accesses.
/SER1CS	104	O	Serial Port 1 Decode. This output is asserted when I/O addresses 03F8 - 03FF are selected. These addresses correspond to the space for the serial port.

Pin Symbol	Pin Numbers	Pin Type	Description
/TEST	110	I	Test Input. This input is used for functional testing of the circuit and is not used in the system operation.
/VGASET	152	O	Set up VGA. This active low output directs the VGA circuit into the setup mode. This signal reflects the status of bit 5 of the register at address 0094H.
MISCELLANEOUS			
VDD	18,38,60,83,102, 108,123,139,158	I	Power
VSS	3,19-22,43,53,62, 63,68,78,99-101, 107,118,140	I	Ground
RESERVED	1,2,23,39-42, 159,160	I	Reserved for future use. Must not be used in system.

FEATURES

- Dual Functions
- Replace up to 44 TTL Packages
- Substantial Space and Power Savings
- High Performance

OVERVIEW

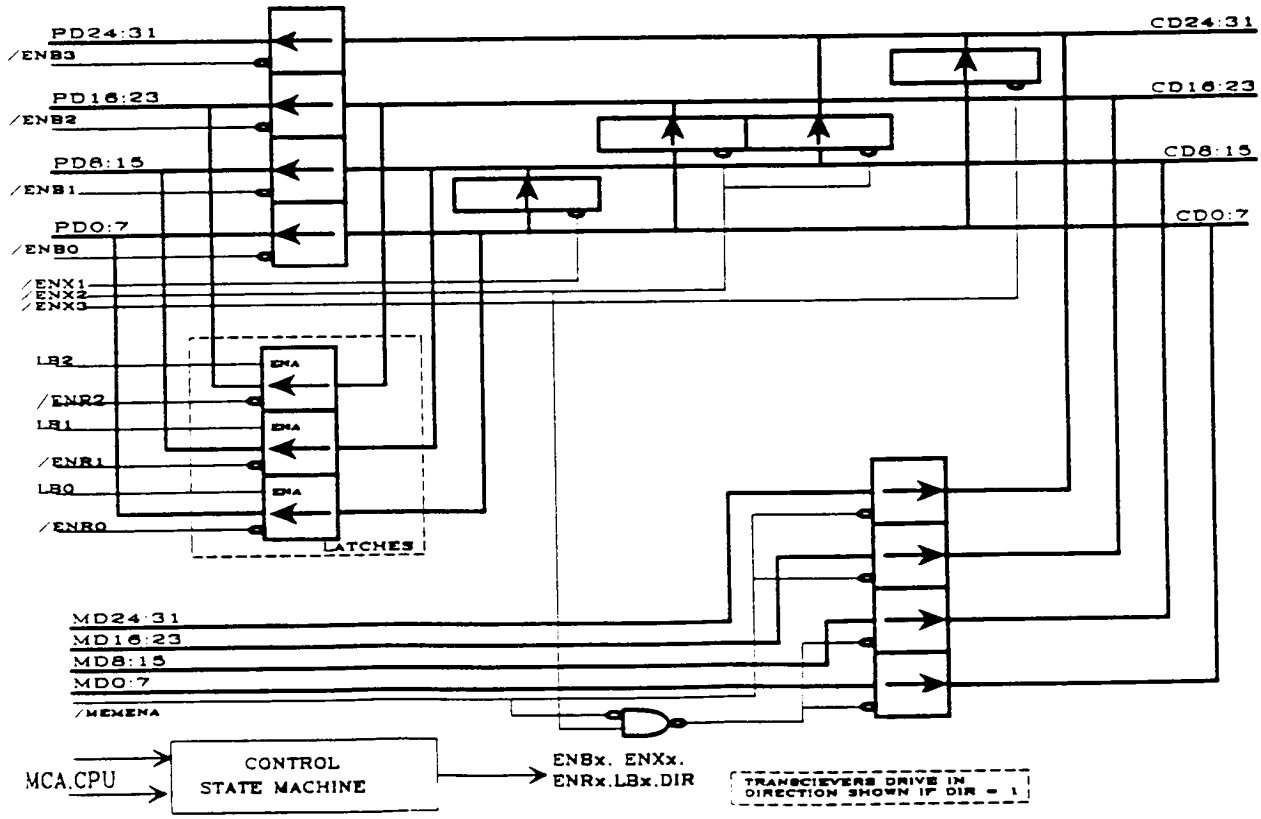
The GC184 is a BiCMOS circuit which is used to eliminate a large number of TTL buffer devices which would otherwise be required for a system implementation. In a 32 bit system it eliminates up to 44 separate IC packages. In addition to the obvious benefits of reduced package count for manufacturing, test and packaging economies, it provides additional functionality when configured as an address buffer.

SYSTEM CONFIGURATION

The GC184 operates either as a data buffer or as an address buffer part. In either case, it provides the requisite buffering, latching and other functions which are required to implement a 32 bit system. For 16 bit wide systems, the unused 16 bits of the system data buses are simply left open. Selection of the function is done throught the ADDRMODE pin. If this pin is left open so that it is pulled high by the internal pullup, then the part functions as an address buffer. If this pin is pulled low, the part acts as a data buffer.

ADDRESS BUFFER CONGIGURATION

In this configuration, three address busses are connected to the chip. The 32 bits of a 386 processor address as well as the byte enable pins constitute the processor address bus. There is a 32 bit Micro Channel address bus and a



20 bit local peripheral address bus. The primary function of the chip is to provide for the proper flow of address information dependent upon the controlling source of any given system cycle. In addition, there are functions added to the chip to further reduce the system package count.

There are a number of reserved pins to provide functionality for future system chip set features which take advantage of the high speed and drive capability of the chip technology.

DATA BUFFER CONFIGURATION

In the data buffer configuration, the 32 bit data buffers for the channel, system processor and system board memory are controlled. Part of this data flow control includes the necessary bus translation to position bytes properly on the bus. This translation requirement occurs during communications between a 32 bit CPU and devices or memory accesses of less than 32 bits. In addition, memory parity is checked and generated within the chip.

The block diagram in Figure 5.1 shows the translation buffers contained in the chip. The Signals which latch and then subsequently read data bytes onto the bus are derived internally from key Micro Channel and system board processor control signals by the internal state machine.

Headland
Technology Inc

Sales Representatives

UNITED KINGDOM
LSI LIMITED
Grenville Place, The Ring
Bracknell, Berkshire
RG12 1BP
United Kingdom
Tel: 011 44 344 426544
Fax: 011 44 344 481039

WEST GERMANY
VIDEO SEVEN/HEADLAND
TECHNOLOGY INC
Luederitzstrasse 13
D6600 Saarbruecken
West Germany
Tel: 011 49 681 33469
Fax: 011 49 681 32391

HEADLAND TECHNOLOGY
Stefan-George-Ring 23
8000 Munich 81
West Germany
Tel: 011 49 89 93009811
Fax: 011 49 89 93009833

Headland Technology Inc.
46221 Landing Parkway
Fremont, CA 94538
Tel 415-656-7800
Fax 415-656-0397