HY5118160B Series

1M x 16-bit CMOS DRAM with 2$\overline{CAS}$

DESCRIPTION

The HY5118160B is the new generation and fast dynamic RAM organized 1,048,576 x 16-bit. The HY5118160B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5118160B to be pack aged in a standard 42/42 pin plastic SOJ, 44/50 pin TSOP-II and Reverse TSOP-II.
The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V ±10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  Max. battery back-up 1.9mW (SL-part)
  Max. CMOS standby 1.7mW (SL-part)
  5.5mW
  Max. TTL standby 11.0mW
  Max. operating

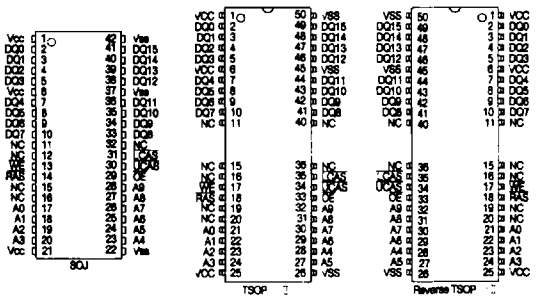
Speed	Power
60	880mW
70	825mW
80	770mW

- **Single power supply of 5V±10%**
- **TTL compatible inputs and outputs**
- **Fast access and cycle time**

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	45ns
80	80ns	20ns	50ns

- **Fast Page mode operation**
- **2$\overline{CAS}$ Inputs for upper and lower byte control**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh and Self Refresh capability**
- **1024 refresh cycles / 256ms (SL-part)**
  1024 refresh cycles / 16ms

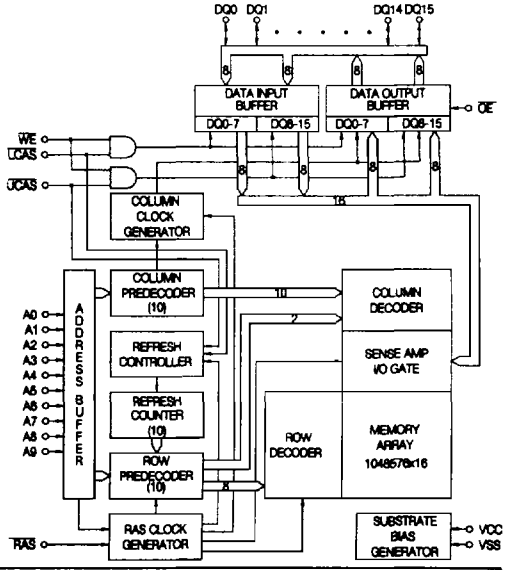
PIN CONNECTION



PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$, $\overline{UCAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A9	Address input
DQ0-DQ15	Data Input/Output
Vcc	Power (+5V)
Vss	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	- 55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	- 1.0 to 7.0	V
VCC	Voltage on VCC Relative to Vss	- 1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	2.4	-	Vcc+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE: All voltages are referenced to VSS.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le V_{CC}$+1.0V All other pins not under test=V_{SS}		-10	10	μA	
I_{LO}	Output Leakage Current (High impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	μA	
I_{CC1}	Vcc Supply Current, Operating	t_{RC} = t_{RC} (min.)	60 70 80	- - -	160 150 140	mA	1,2,3
I_{CC2}	Vcc Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs V_{SS}	 SL-Part	- -	2 1	mA	
I_{CC3}	Vcc Supply Current, $\overline{RAS}$-only Refresh	t_{RC} = t_{RC} (min.)	60 70 80	- - -	160 150 140	mA	1,3
I_{CC4}	Vcc Supply Current, Fast Page mode	t_{PC} = t_{PC} (min.)	60 70 80	- - -	110 100 90	mA	1,2,3
I_{CC5}	Vcc Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ Vcc-0.2V	 SL-part	- -	1 300	mA μA	5
I_{CC6}	Vcc Supply Current, $\overline{CAS}$-before- $\overline{RAS}$ Refresh	t_{RC} = t_{RC} (min.)	60 70 80	- - -	160 150 140	mA	1,2
I_{CC7}	Vcc Supply Current, Battery Back up (SL-part only)	t_{RC} = 250μs, $\overline{CAS}$ = CBR cycling or 0.2V	t_{RAS} ≤ 300ns	-	350	μA	4,5
		$\overline{OE}$ & $\overline{WE}$=Vcc-0.2V or 0.2V A0-A9 = Vcc-0.2V or 0.2V DQ0 -DQ15= -0.2V, Vcc-0.2V or open	t_{RAS} ≤ 1μs	-	450		
I_{CC8}	Vcc Supply Current, Self Refresh (SL-part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤ 0.2V other pins same as I_{CC7}		-	350	μA	5
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -5.0mA		2.4	-	V	

NOTE :

1. I_{CC1},I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading. Specified values are obtained with the output open.
3. I_{CC} is specified as an average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$ =V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.
4. Only t_{RAS}(max.)=1μs is applied to refresh of battery backup but t_{RAS}(max.)=10μs is applied to normal functional operation .
5. I_{CC5}(max.) =300 μA, I_{CC7} and I_{CC8} are applied to SL-part only.

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V ± 10%, VSS=0V, unless otherwise noted.) NOTE3,7,8

#	SYMBOL	PARAMETER	HY5118160BJC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	170	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	95	-	105	-	ns	
5	tRAC	Access Time form $\overline{RAS}$	-	60	-	70	-	80	ns	8,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	8,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	
8	tCPA	Access Time from $\overline{CAS}$ Precharge		35		35		45	ns	8,15
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	8
10	tOFF	Output Buffer Turn-off Delay from $\overline{CAS}$	0	15	0	15	0	15	ns	11
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	6
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	15	-	20	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	40	-	50	-	60	-	ns	
17	tCAS	$\overline{CAS}$ Pulse width	15	10K	15	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	15	45	20	50	20	60	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	20
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	15
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	15
26	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
27	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	15
28	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	13,15
29	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	15
30	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	15
31	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
32	tRWL	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
33	tCWL	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	22
34	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	15,25
35	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	15,25
36	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	18
		SL-part	-	256	-	256	-	256	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	15,16
38	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	-	50	-	50	-	ns	16
39	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	85	-	95	-	105	-	ns	16
40	tAWD	Column Address to $\overline{WE}$ Delay Time.	55	-	60	-	65	-	ns	16

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	5118160BJC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCSR	$\overline{CAS}$ Set-up Time(CBR Cycle)	5	-	5	-	5	-	ns	15
42	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15,23
43	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	15,24
44	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	20
45	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	10	-	10	-	10	-	ns	
46	tOEA	$\overline{OE}$ Access Time	-	15	-	20	-	20	ns	
47	tOED	$\overline{OE}$ to Data Delay	15	-	20	-	20	-	ns	
48	tOEZ	Output Buffer Turn Off Delay Time	0	15	0	15	0	15	ns	11
49	tOEH	$\overline{OE}$ Command Hold Time	15	-	20	-	20	-	ns	
50	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	55	-	65	-	75	-	ns	16
51	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	-	40	-	50	-	ns	
52	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
53	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	-	10	-	10	-	ns	
54	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	µs	
55	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh Cycle)	110	-	130	-	150	-	ns	
56	tCHS	$\overline{CAS}$ Hold Time (Self Refresh Cycle)	50	-	50	-	50	-	ns	

NOTE:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages referenced to V_{SS}.
3. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
4. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In case of changed once or less during a fast page mode cycle (t_{PC}).
5. AC measurements assume t_T = 3ns.
6. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_A = 0 to 70°C) is assured.
8. Measured at V_{OH}=2.4V and V_{OL}=0.4V with a load equivalent to 2TTL load and 100pF.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. t_{OFF}(max.), t_{REZ}(max.) t_{WEZ}(max.) t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. The t_{CRP} requirement should be applicable for $\overline{RAS}$ / $\overline{CAS}$ cycles preceded by any cycle.
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
14. Parameter t_{WP} is a applicable for a late write cycle. For early write cycle., t_{WCH} must be met.
15. These parameters are referenced to $\overline{UCAS}$ or $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and the data output pin will remain open circuit(high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell : If neither of the above sets of condition of the data out (at access time) is interminate.
17. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by RAS high going.
18. 1024 cycles of Burst refresh must be excuted within 16ms after exiting Self Refresh.
19. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
20. t_{CP} and t_{CPT} are measured when both $\overline{LCAS}$ and $\overline{UCAS}$ are high state.
21. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
22. t_{CWL} must be satisfied by both $\overline{LCAS}$ and $\overline{UCAS}$ fpr 16-bits access cycles.
23. t_{CSR} is referenced to the earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
24. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.
25. t_{DS}, t_{DH} is independetly specified for lower byte DQ(0-7), upper byte DQ(8-15).

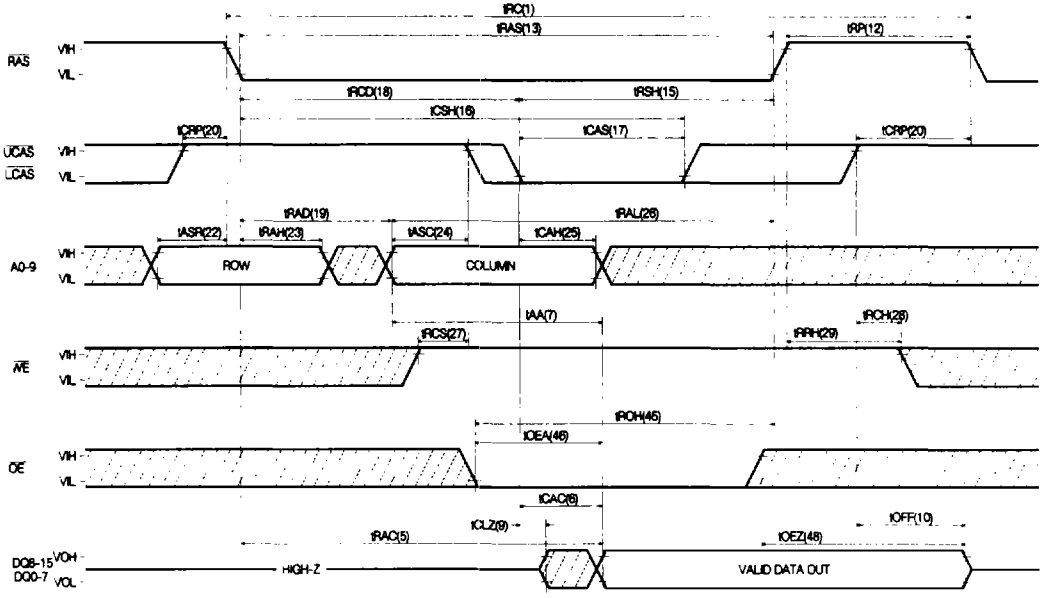
CAPACITANCE

(T_A=25°C, Vcc=5V±10%, Vss=0V, f=1MHz, unless otherwise noted.)

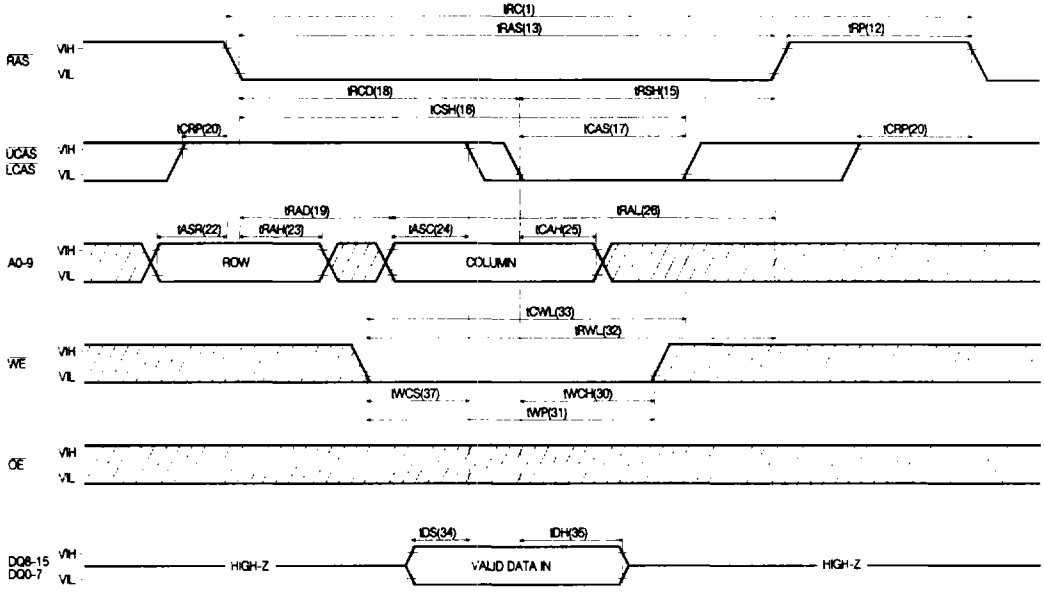
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A9)	-	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$,$\overline{UCAS}$,$\overline{WE}$, $\overline{OE}$)	-	7	pF
C_{DQ}	Data Input/Output Capacitance (DQ0 - DQ15)	-	7	pF

TIMING DIAGRAM

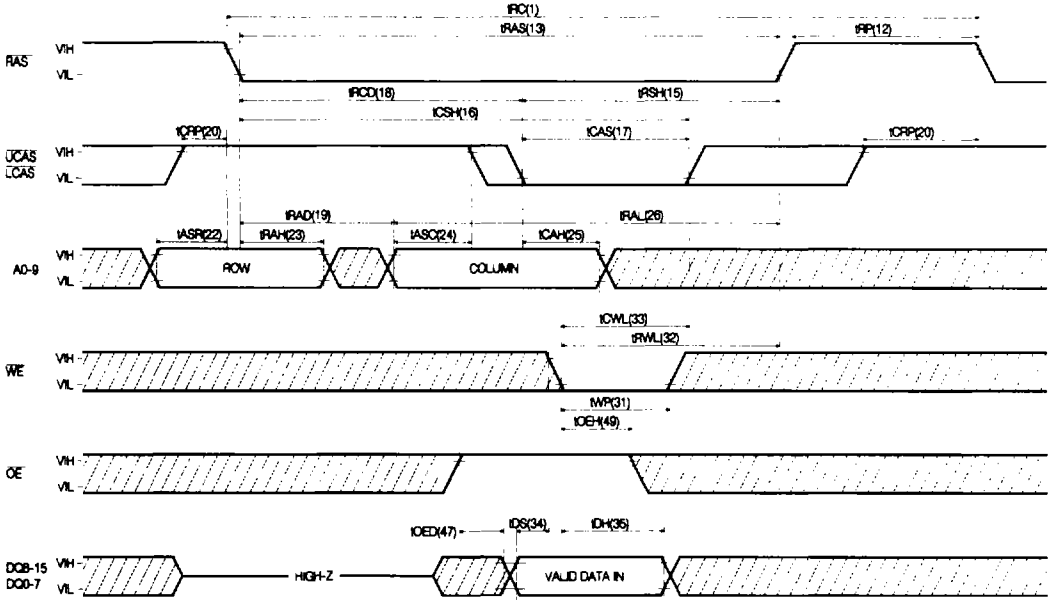
READ CYCLE



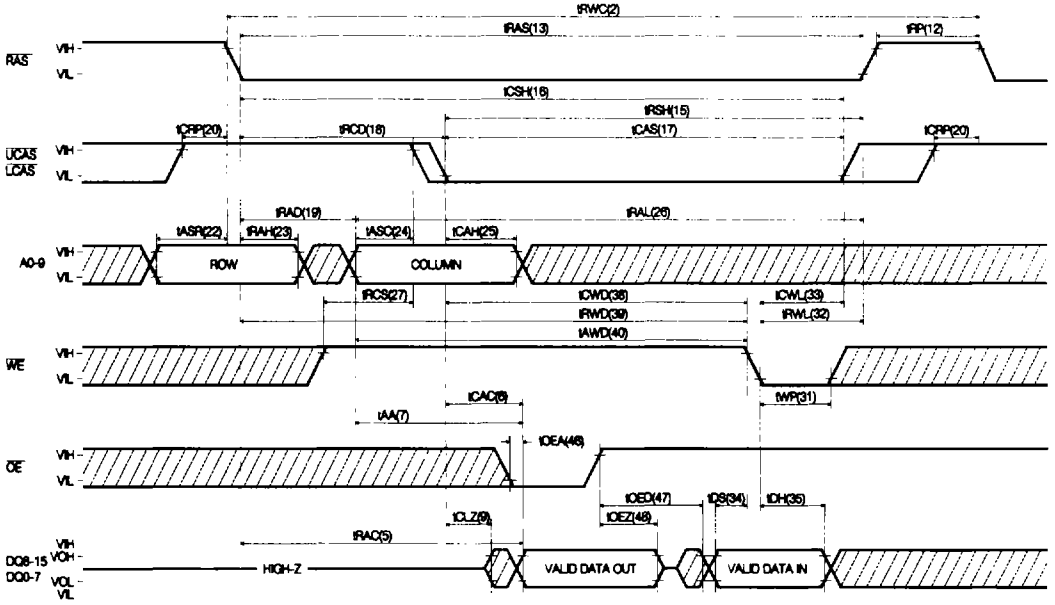
EARLY WRITE CYCLE



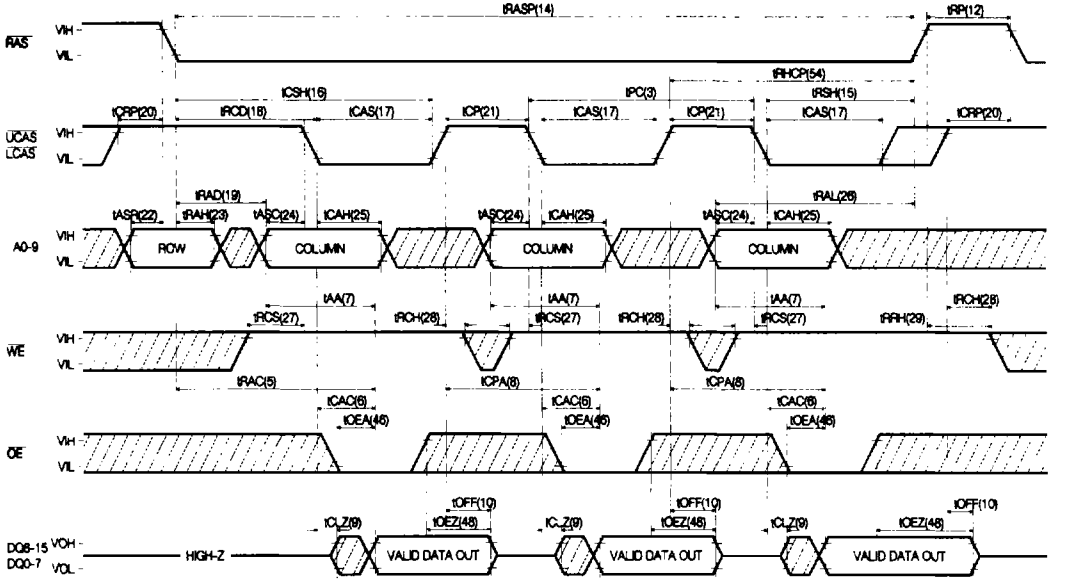
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



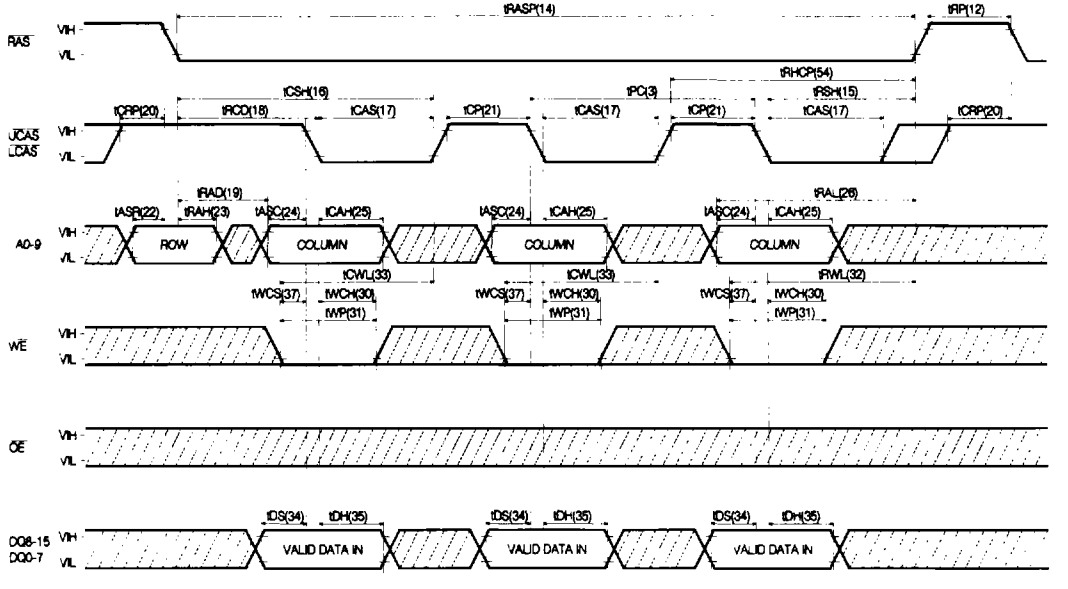
READ-MODIFY-WRITE CYCLE



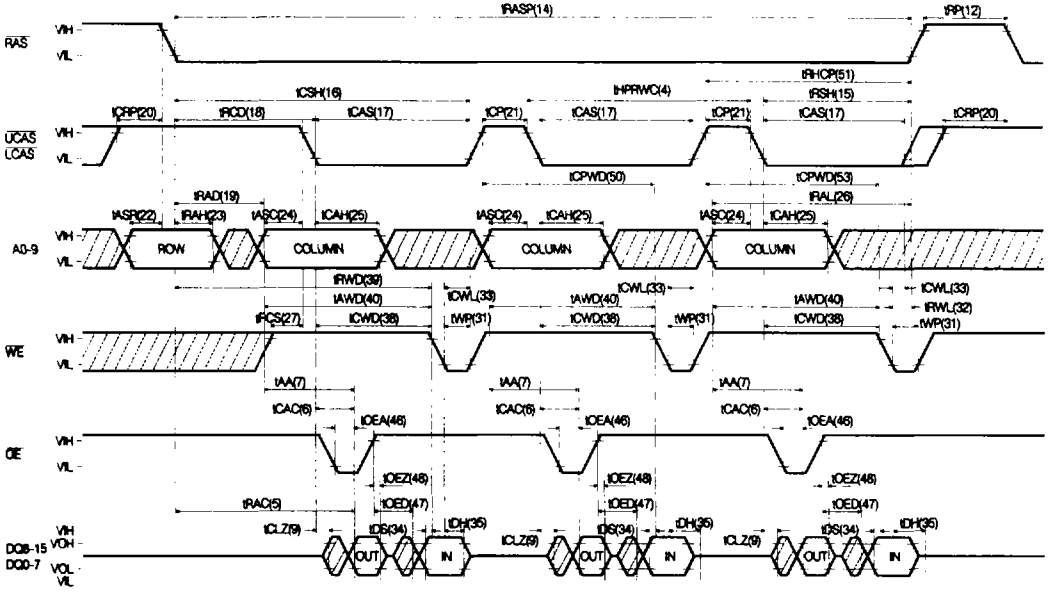
FAST PAGE MODE READ CYCLE



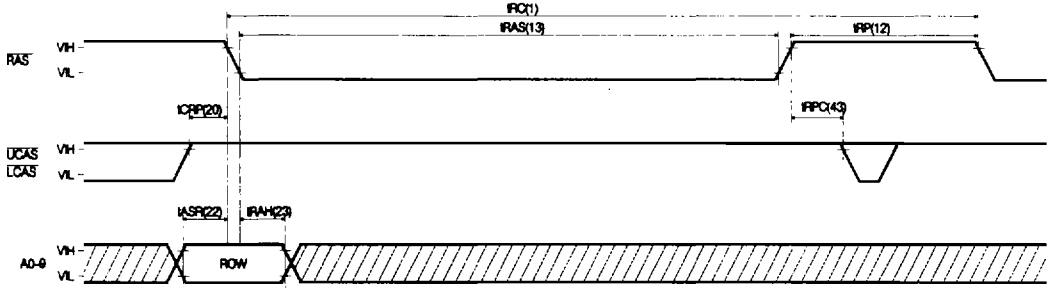
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

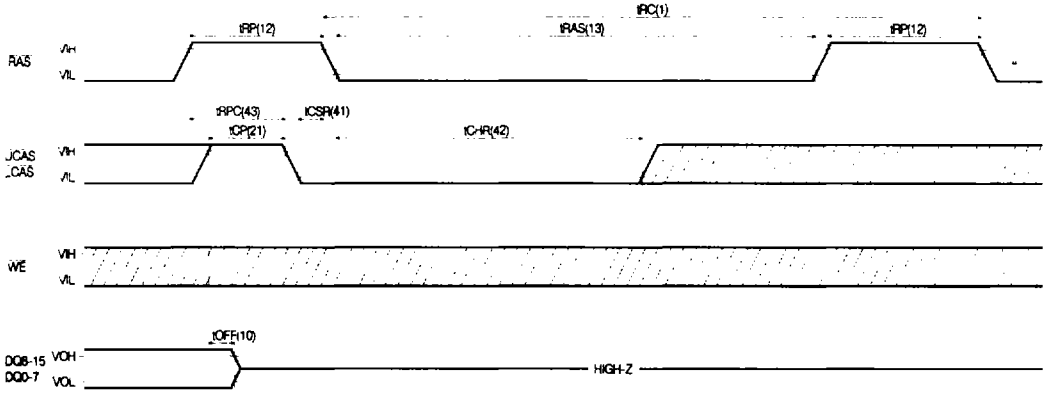


RAS-ONLY REFRESH CYCLE



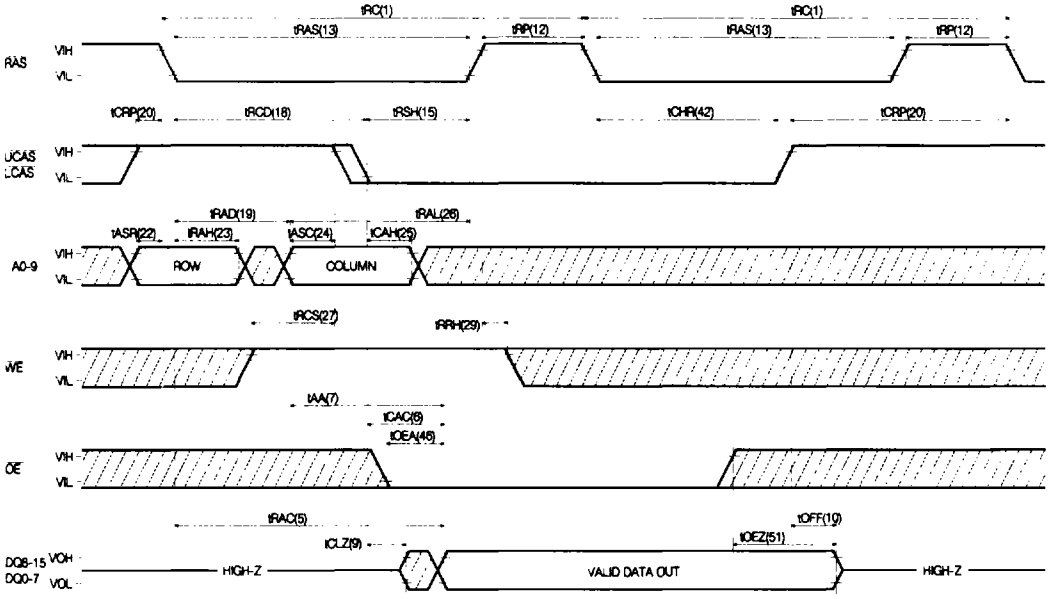
NOTE : $\overline{OE}$ and $\overline{WE}$ ="H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

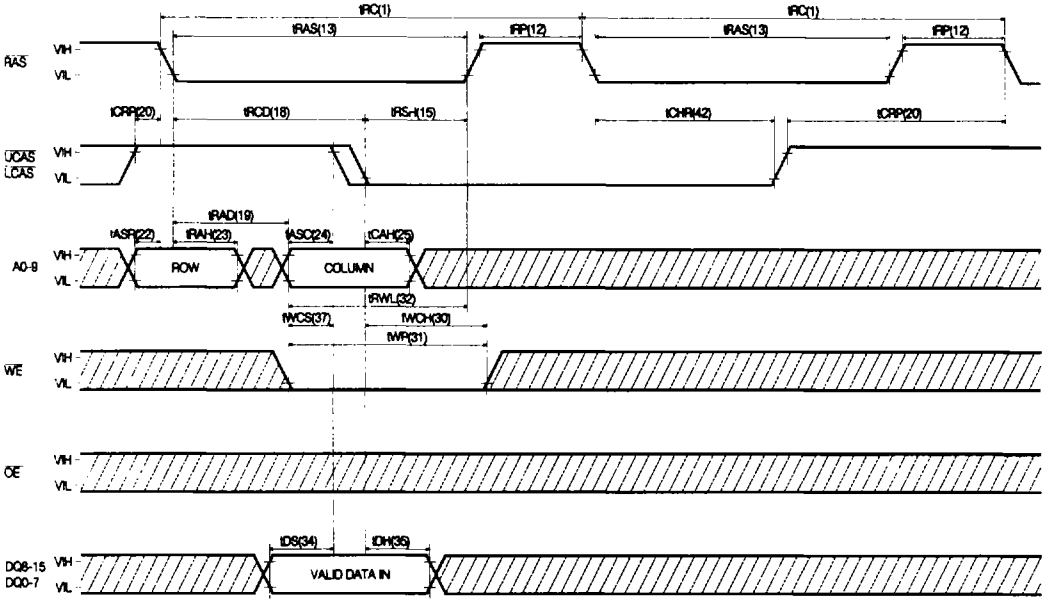


NOTE : A0-9 and $\overline{OE}$ = "H" or "L"

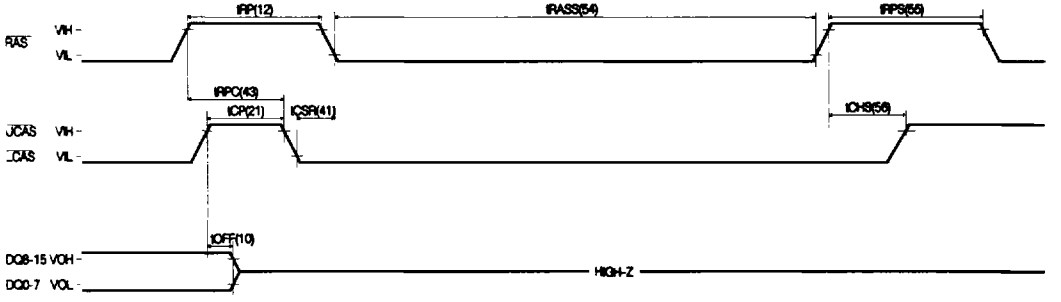
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

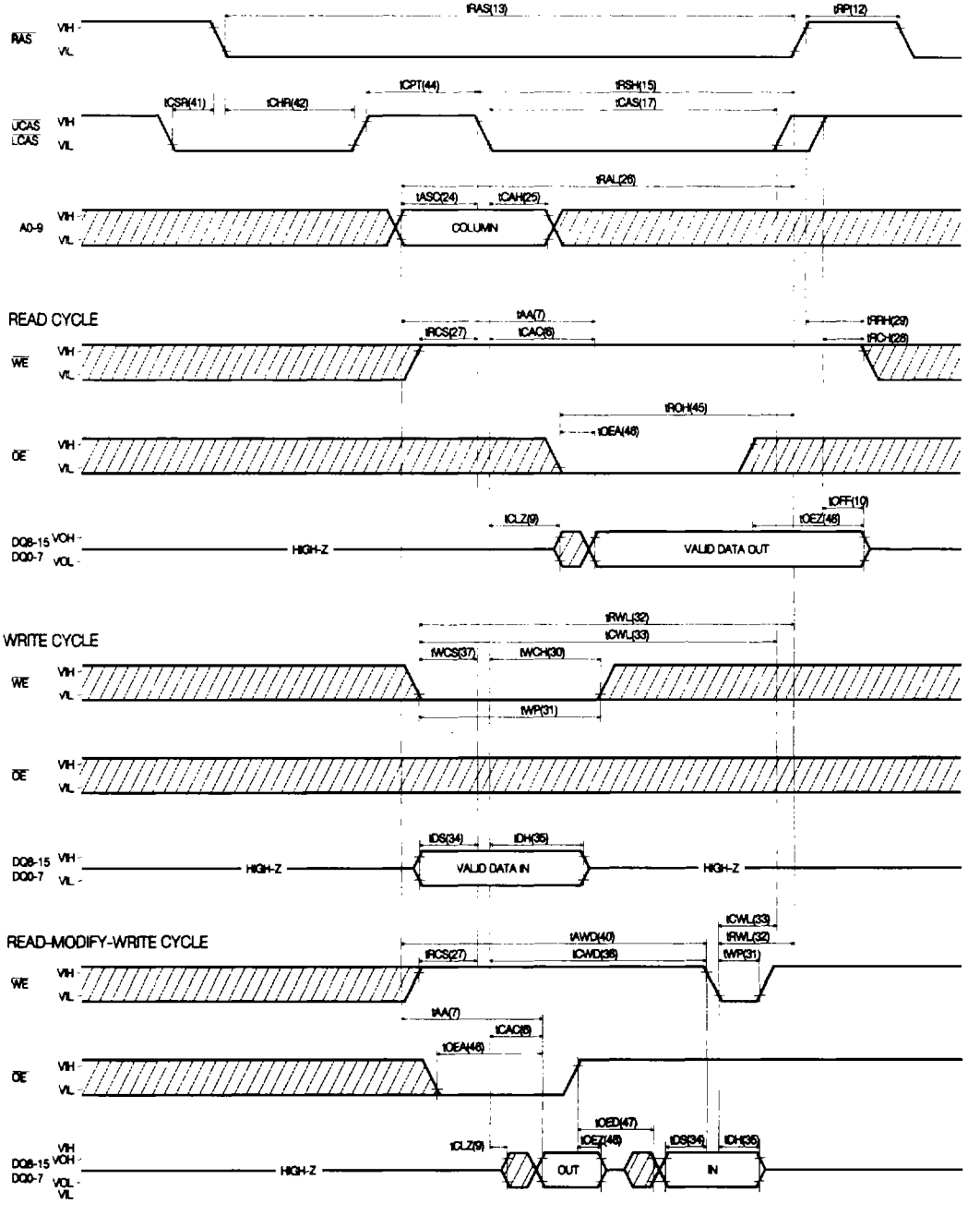


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



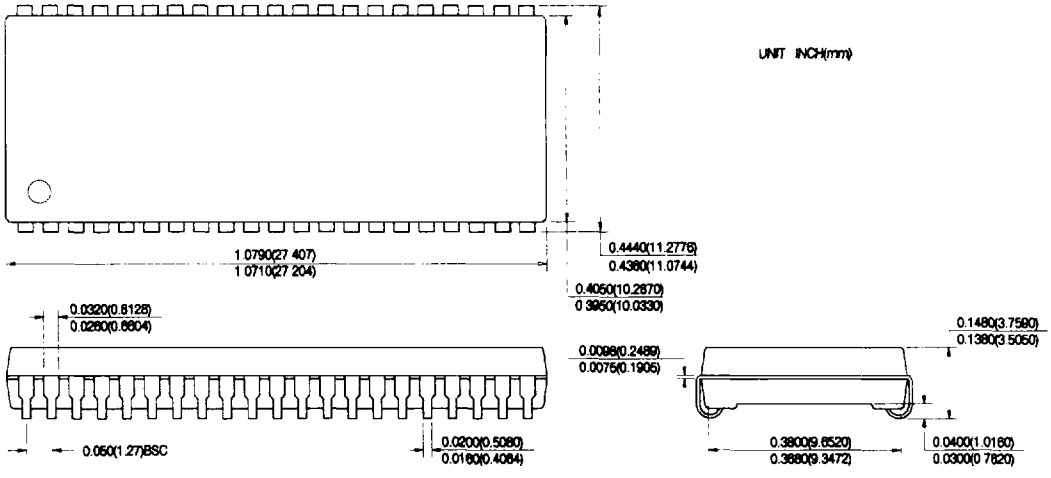
NOTE : A0-9 $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

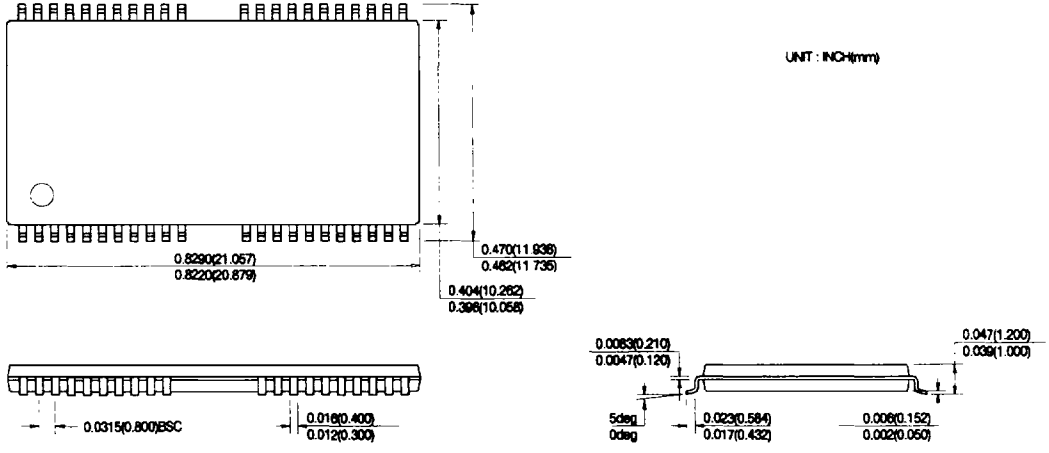


PACKAGE INFORMATION

400 mil 42/42 pin Small Outline J-form Package (JC)



400 mil 44/50 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAG6E
HY5118160BJC	60/70/80		SOJ
HY5118160BSLJC	60/70/80	SL-part	SOJ
HY5118160BTC	60/70/80		TSOP-II
HY5118160BSLTC	60/70/80	SL-part	TSOP-II
HY5118160BRC	60/70/80		TSOP-II(R)
HY5118160BSLRC	60/70/80	SL-part	TSOP-II(R)