OPTi®

PYTHON CHIPSET FOR PENTIUM™ PROCESSORS

82C546 & 82C547 Data Book

Version 1.0

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Table of Contents

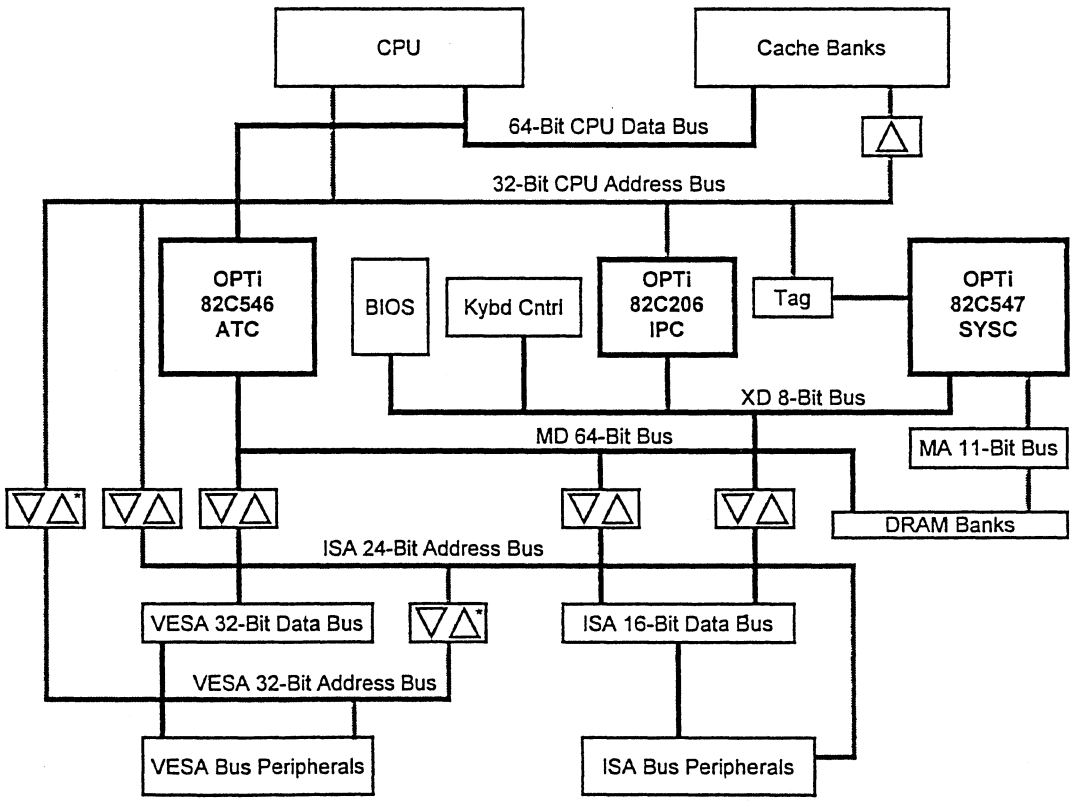
List of Figures

List of Tables

1.0 Features

- 100% PC/AT® compatible
- Fully supports the 3.3V/5.0V Pentium™ processors
- Three chip solution:
  - 82C547 System Controller (SYSC) (160-pin PQFP)
  - 82C546 AT™ Bus Controller (ATC) (208-pin PQFP)
  - 82C206 Integrated Peripherals Controller (IPC) (84-pin PLCC or 100-pin PQFP)
- Two buffer/translator support chips:
  - 82C606A (100-pin PQFP)
  - 82C606B (100 pin PQFP)
- Supports Pentium CPU address pipelining
- 1X clock source, supporting systems running Pentium processor bus clocks up to 60MHz
- Write-back, direct-mapped cache with size selections: 64KB, 128KB, 256KB, 512KB, 1MB, and 2MB
- Programmable cache write policy: write-back or write-through
- Fully programmable cache and DRAM read/write cycles
- Supports 3-2-2-2 cache burst read cycles at 60MHz
- Built-in tag auto-invalidation circuitry
- Support for two programmable non-cacheable memory regions
- Options for cacheable, write-protected, system and video BIOS
- Supports two banks of 64-bit wide DRAMs with 256KB, 512KB, 1MB, 2MB, 4MB and 8MBx36 Page Mode DRAMs
- Supports DRAM configurations up to 128MB
- Supports 3-3-3-3 pipeline DRAM burst cycles
- DRAM post write buffer
- Support for flash ROM
- Shadow RAM option

Figure 1-1 Python-Based System Block Diagram



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Features (Cont.)

- Hidden refresh with CAS-before-RAS refresh supported
- High-performance 32-bit local bus support
- Performance-oriented snoop-line comparator for VL/ISA bus masters
- Extended DMA page register
- Turbo/slow speed selection
- Asynchronous CPU and VL bus interface
- AT bus clock speed programmability
- Transparent 8042 emulation for Fast CPU Reset and GATEA20 generation
- Supports Port 92h, Gate A20, and Fast Reset
- Mixed voltage (3.3V and 5.0V), low-power, high-speed, 0.8-micron CMOS technology

2.0 Overview

The OPTi Python Chipset provides a highly integrated solution for fully compatible, high-performance PC/AT platforms. Together, with OPTi's 82C206 Integrated Peripheral Controller (IPC), this chipset will support the Pentium processor in the most cost effective and feature-rich designs available today. This highly integrated approach provides the foundation for a cost effective platform without compromising performance. The OPTi Python Chipset supplies a powerful solution positioned to deliver value without neglecting quality, compatibility, or reliability.

The Python Chipset is comprised of two chips, the 82C547 System Controller (SYSC) and the 82C546 AT Bus Controller (ATC). A complete Pentium processor solution consists of the Python Chipset and the 82C206 Integrated Peripheral Controller (IPC).

2.1 82C546 (ATC) AT Bus Controller

The 82C546 ATC integrates the AT bus interface and data buffers for transfers between the CPU data bus, local data bus and the DRAM data bus. It also provides the ISA to local bus command translation.

- 208-pin PQFP
- Data bus buffer (host data to memory data)
- Data bus buffer control (ISA to memory)
- Parity generation and detection circuitry
- Keyboard controller chip select
- Local bus interface (ISA to local bus command translation)

2.2 82C547 (SYSC) System Controller

The 82C547 SYSC provides the control functions for the host CPU interface, the 32-bit local bus interface, the 64-bit Level 2 (L2) cache and the 64-bit DRAM bus. The SYSC also controls the data flow between the CPU bus, the DRAM bus, the local bus, and the 8/16-bit ISA bus.

- 160-pin PQFP
- Pentium CPU interface
- DRAM controller
- L2 cache controller
- L1 cache controller
- Local bus interface
- Reset generation
- Arbitration logic
- Data bus buffer control (memory data to/from host data)
- Extended DMA page register
- Keyboard emulation of A20M# and CPU warm reset
- Port B and Port 92h Register

2.3 82C206 (IPC) Integrated Peripherals Controller

The 82C206 IPC provides two DMA controllers, two interrupt controllers, one timer/counter, and a real-time clock in an industry standard single-chip solution for the peripherals attached to the PC/AT peripheral bus.

- 84-pin PLCC or 100-pin PQFP
- Supports four DMA transfer modes
- Special Commands provided for ease of programming

2.4 Support Chips

The 82C606A and 82C606B are two buffer/translation devices used to translate 3.3V signals to 5.0V signal levels in Python motherboard solutions. These devices buffer the CPU address bus to the ISA and VL address buses, the 82C546 ATC's memory data bus to the ISA data bus, the peripheral XD bus to the ISA SA and SD buses. The 82C606A and 82C606B integrate a number of glue logic TTL devices (approximately eleven), hence reducing the amount of TTL on the motherboard.

The 82C606A and 82C606B devices are actually the same device with two strapping options. Pulling the CONF1/2# pin high causes the device to function in the 82C606A Mode. Pulling the CONF1/2# pin low configures the device to function in the 82C606B Mode of operation.

- 100-pin PQFP
- Mixed voltage to support 3.3V to 5.0V signal translation
- Two devices replace approximately eleven TTL devices

3.0 Signal Definitions

Figure 3-1 82C546 ATC Pin Diagram

Table 3-1 82C546 ATC Numerical Pin Cross-Reference List

Pin#	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	SBHE#	53	HLDA1	105	GND	157	MD40
2	XA0	54	AEN16#	106	D21	158	MD39
3	XA1	55	AEN8#	107	D20	159	MD38
4	LA2	56	D63	108	D19	160	MD37
5	MP7	57	D62	109	D18	161	MD36
6	MP6	58	D61	110	D17	162	MD35
7	MP5	59	D60	111	D16	163	MD34
8	MP4	60	GND	112	D15	164	GND
9	MP3	61	VCC3	113	D14	165	VCC
10	VCC	62	D59	114	VCC3	166	MD33
11	MP2	63	D58	115	D13	167	MD32
12	MP1	64	D57	116	D12	168	MD31
13	MP0	65	D56	117	D11	169	MD30
14	ATCLK	66	D55	118	D10	170	MD29
15	GND	67	D54	119	GND	171	MD28
16	LCLK	68	D53	120	D9	172	MD27
17	0WS#	69	GND	121	D8	173	MD26
18	CHRDY	70	D52	122	D7	174	GND
19	M16#	71	D51	123	D6	175	MD25
20	IO16#	72	D50	124	D5	176	MD24
21	LDEV#	73	D49	125	D4	177	MD23
22	LDEN#	74	D48	126	D3	178	MD22
23	LDIR#	75	D47	127	D2	179	MD21
24	MRD#	76	D46	128	D1	180	MD20
25	MWR#	77	D45	129	D0	181	MD19
26	VCC	78	VCC3	130	VCC	182	MD18
27	IORD#	79	D44	131	MD63	183	VCC
28	IOWR#	80	D43	132	MD62	184	MD17
29	RFSH#	81	D42	133	MD61	185	MD16
30	ALE	82	D41	134	MD60	186	MD15
31	LMEM#	83	D40	135	MD59	187	MD14
32	HDMDOE#	84	D39	136	MD58	188	MD13
33	MDHDOE#	85	D38	137	MD57	189	MD12
34	DWE#	86	D37	138	MD56	190	MD11
35	DLE#	87	GND	139	MD55	191	MD10
36	LD/C#	88	D36	140	MD54	192	GND
37	LRDY#	89	D35	141	MD53	193	MD9
38	GND	90	D34	142	GND	194	MD8
39	LW/R#	91	D33	143	MD52	195	MD7
40	LM/IO#	92	D32	144	MD51	196	MD6
41	LADS#	93	D31	145	MD50	197	MD5
42	LBE3#	94	D30	146	MD49	198	MD4
43	VCC	95	D29	147	VCC	199	MD3
44	LBE2#	96	GND	148	MD48	200	GND
45	LBE1#	97	VCC3	149	MD47	201	VCC
46	LBE0#	98	D28	150	MD46	202	MD2
47	PERR	99	D27	151	MD45	203	MD1
48	RESET	100	D26	152	MD44	204	MD0
49	BOFF#	101	D25	153	MD43	205	SDEN#
50	P6X#/LMCS#	102	D24	154	MD42	206	SDIR1#
51	INTA#	103	D23	155	MD41	207	SDIR2#
52	LREQ#	104	D22	156	GND	208	KBDCS#

Table 3-2 82C546 ATC Alphabetical Pin Cross-Reference List

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
0WS#	17	D45	77	LDEV#	21	MD45	151
AEN16#	54	D46	76	LDIR#	23	MD46	150
AEN8#	55	D47	75	LM/IO#	40	MD47	149
ALE	30	D48	74	LRDY#	37	MD48	148
ATCLK	14	D49	73	LREQ#	52	MD49	146
BOFF#	49	D50	72	LW/R#	39	MD50	145
CHRDY	18	D51	71	M16#	19	MD51	144
D0	129	D52	70	MD0	204	MD52	143
D1	128	D53	68	MD1	203	MD53	141
D2	127	D54	67	MD2	202	MD54	140
D3	126	D55	66	MD3	199	MD55	139
D4	125	D56	65	MD4	198	MD56	138
D5	124	D57	64	MD5	197	MD57	137
D6	123	D58	63	MD6	196	MD58	136
D7	122	D59	62	MD7	195	MD59	135
D8	121	D60	59	MD8	194	MD60	134
D9	120	D61	58	MD9	193	MD61	133
D10	118	D62	57	MD10	191	MD62	132
D11	117	D63	56	MD11	190	MD63	131
D12	116	DLE#	35	MD12	189	MDHD0E#	33
D13	115	DWE#	34	MD13	188	MP0	13
D14	113	GND	15	MD14	187	MP1	12
D15	112	GND	38	MD15	186	MP2	11
D16	111	GND	60	MD16	185	MP3	9
D17	110	GND	69	MD17	184	MP4	8
D18	109	GND	87	MD18	182	MP5	7
D19	108	GND	96	MD19	181	MP6	6
D20	107	GND	105	MD20	180	MP7	5
D21	106	GND	119	MD21	179	MRD#	24
D22	104	GND	142	MD22	178	MWR#	25
D23	103	GND	156	MD23	177	P6X#/LMCS#	50
D24	102	GND	164	MD24	176	PERR	47
D25	101	GND	174	MD25	175	RESET	48
D26	100	GND	192	MD26	173	RFSH#	29
D27	99	GND	200	MD27	172	SBHE#	1
D28	98	HDMDOE#	32	MD28	171	SDEN#	205
D29	95	HLDA1	53	MD29	170	SDIR1#	206
D30	94	INTA#	51	MD30	169	SDIR2#	207
D31	93	IO16#	20	MD31	168	VCC	10
D32	92	IORD#	27	MD32	167	VCC	26
D33	91	IOWR#	28	MD33	166	VCC	43
D34	90	KBDCS#	208	MD34	163	VCC	130
D35	89	LMEM#	31	MD35	162	VCC	147
D36	88	LA2	4	MD36	161	VCC	165
D37	86	LADS#	41	MD37	160	VCC	183
D38	85	LBE0#	46	MD38	159	VCC	201
D39	84	LBE1#	45	MD39	158	VCC3	61
D40	83	LBE2#	44	MD40	157	VCC3	78
D41	82	LBE3#	42	MD41	155	VCC3	97
D42	81	LCLK	16	MD42	154	VCC3	114
D43	80	LD/C#	36	MD43	153	XA0	2
D44	79	LDEN#	22	MD44	152	XA1	3

Figure 3-2 82C547 SYSC Pin Diagram

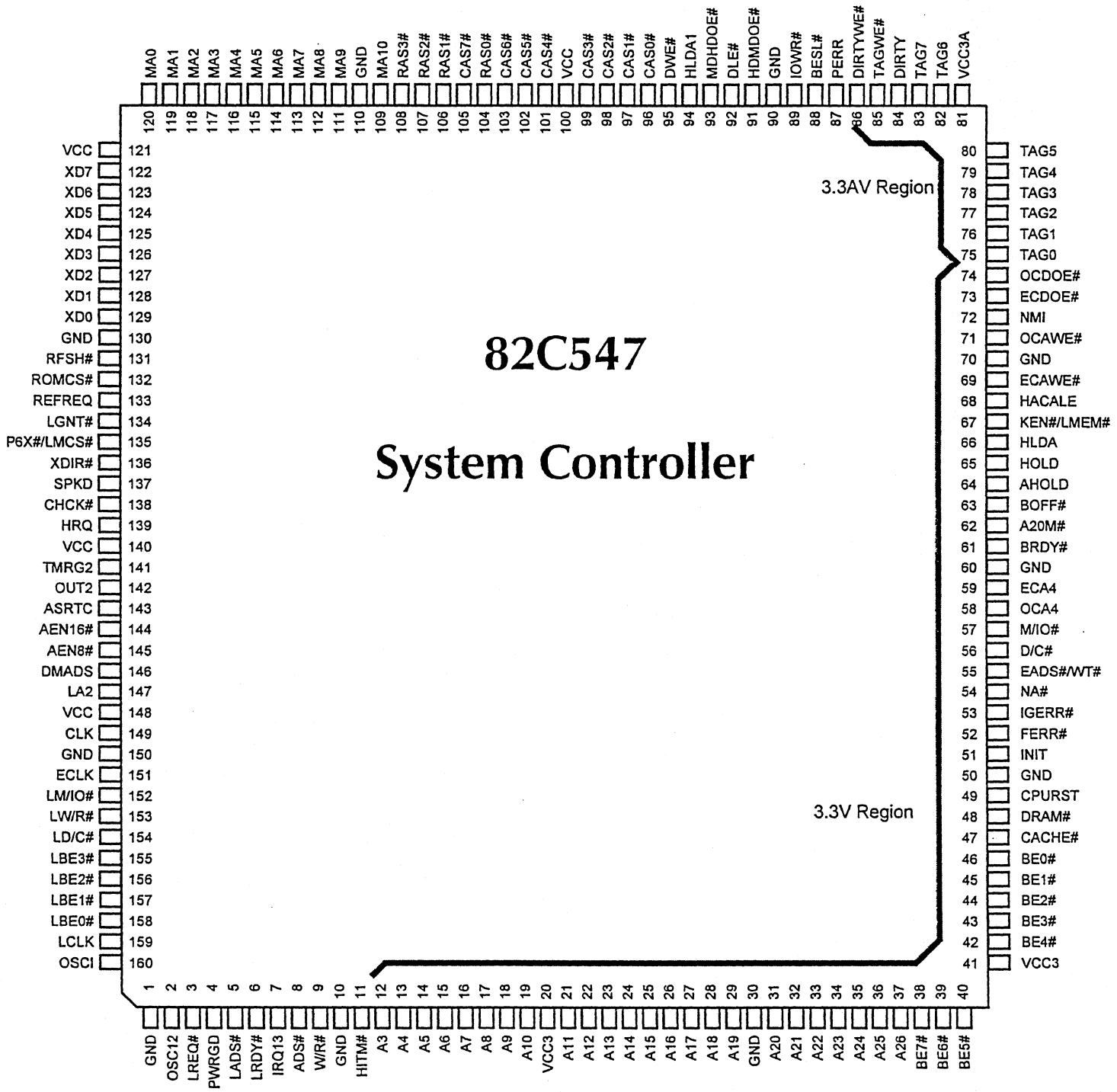


Table 3-3 82C547 SYSC Numerical Pin Cross-Reference List

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GND	41	VCC3	81	VCC3A	121	VCC
2	OSC12	42	BE4#	82	TAG6	122	XD7
3	LREQ#	43	BE3#	83	TAG7	123	XD6
4	PWRGD	44	BE2#	84	DIRTY	124	XD5
5	LADS#	45	BE1#	85	TAGWE#	125	XD4
6	LRDY#	46	BE0#	86	DIRTYWE#	126	XD3
7	IRQ13	47	CACHE#	87	PERR	127	XD2
8	ADS#	48	DRAM#	88	BESL#	128	XD1
9	W/R#	49	CPURST	89	IOWR#	129	XD0
10	GND	50	GND	90	GND	130	GND
11	HITM#	51	INIT	91	HDMDOE#	131	RFSH#
12	A3	52	FERR#	92	DLE#	132	ROMCS#
13	A4	53	IGERR#	93	MDHDOE#	133	REFREQ
14	A5	54	NA#	94	HLDA1	134	LGNT#
15	A6	55	EADS#/WT#	95	DWE#	135	P6X#/LMCS#
16	A7	56	D/C#	96	CAS0#	136	XDIR#
17	A8	57	M/IO#	97	CAS1#	137	SPKD
18	A9	58	OCA4	98	CAS2#	138	CHCK#
19	A10	59	ECA4	99	CAS3#	139	HRQ
20	VCC3	60	GND	100	VCC	140	VCC
21	A11	61	BRDY#	101	CAS4#	141	TMRG2
22	A12	62	A20M#	102	CAS5#	142	OUT2
23	A13	63	BOFF#	103	CAS6#	143	ASRTC
24	A14	64	AHOLD	104	RAS0#	144	AEN16#
25	A15	65	HOLD	105	CAS7#	145	AEN8#
26	A16	66	HLDA	106	RAS1#	146	DMADS
27	A17	67	KEN#/LMEM#	107	RAS2#	147	LA2
28	A18	68	HACALE	108	RAS3#	148	VCC
29	A19	69	ECAWE#	109	MA10	149	CLK
30	GND	70	GND	110	GND	150	GND
31	A20	71	OCAWE#	111	MA9	151	ECLK
32	A21	72	NMI	112	MA8	152	LM/IO#
33	A22	73	ECDOE#	113	MA7	153	LW/R#
34	A23	74	OCDOE#	114	MA6	154	LD/C#
35	A24	75	TAG0	115	MA5	155	LBE3#
36	A25	76	TAG1	116	MA4	156	LBE2#
37	A26	77	TAG2	117	MA3	157	LBE1#
38	BE7#	78	TAG3	118	MA2	158	LBE0#
39	BE6#	79	TAG4	119	MA1	159	LCLK
40	BE5#	80	TAG5	120	MA0	160	OSCI

Table 3-4 82C547 SYSC Alphabetical Pin Cross-Reference

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A3	12	BRDY#	61	HLDA1	94	OSCI	160
A4	13	CACHE#	47	HOLD	65	OUT2	142
A5	14	CAS0#	96	HRQ	139	P6X#/LMCS#	135
A6	15	CAS1#	97	IGERR#	53	PERR	87
A7	16	CAS2#	98	INIT	51	PWRGD	4
A8	17	CAS3#	99	IOWR#	89	RAS0#	104
A9	18	CAS4#	101	IRQ13	7	RAS1#	106
A10	19	CAS5#	102	KEN#/LMEM#	67	RAS2#	107
A11	21	CAS6#	103	LA2	147	RAS3#	108
A12	22	CAS7#	105	LADS#	5	REFREQ	133
A13	23	CHCK#	138	LBE0#	158	RFSH#	131
A14	24	CLK	149	LBE1#	157	ROMCS#	132
A15	25	CPURST	49	LBE2#	156	SPKD	137
A16	26	D/C#	56	LBE3#	155	TAG0	75
A17	27	DIRTY	84	LCLK	159	TAG1	76
A18	28	DIRTYWE	86	LD/C#	154	TAG2	77
A19	29	DLE#	92	LGNT#	134	TAG3	78
A20	31	DMADS	146	LM/IO#	152	TAG4	79
A20M#	62	DRAM#	48	LRDY#	6	TAG5	80
A21	32	DWE#	95	LREQ#	3	TAG6	82
A22	33	EADS#/WT#	55	LW/R#	153	TAG7	83
A23	34	ECA4	59	M/IO#	57	TAGWE#	85
A24	35	ECAWE#	69	MA0	120	TMRG2	141
A25	36	ECDOE#	73	MA1	119	VCC	100
A26	37	ECLK	151	MA2	118	VCC	121
ADS#	8	FERR#	52	MA3	117	VCC	140
AEN8#	145	GND	1	MA4	116	VCC	148
AEN16#	144	GND	10	MA5	115	VCC3	20
AHOLD	64	GND	30	MA6	114	VCC3	41
ASRTC	143	GND	50	MA7	113	VCC3A	81
BE0#	46	GND	60	MA8	112	W/R#	9
BE1#	45	GND	70	MA9	111	XD0	129
BE2#	44	GND	90	MA10	109	XD1	128
BE3#	43	GND	110	MDHDOE#	93	XD2	127
BE4#	42	GND	130	NA#	54	XD3	126
BE5#	40	GND	150	NMI	72	XD4	125
BE6#	39	HACALE	68	OCA4	58	XD5	124
BE7#	38	HDMDOE#	91	OCAWE#	71	XD6	123
BESL#	88	HITM#	11	OCDOE#	74	XD7	122
BOFF#	63	HLDA	66	OSC12	2	XDIR#	136

Figure 3-3 82C606A Pin Diagram

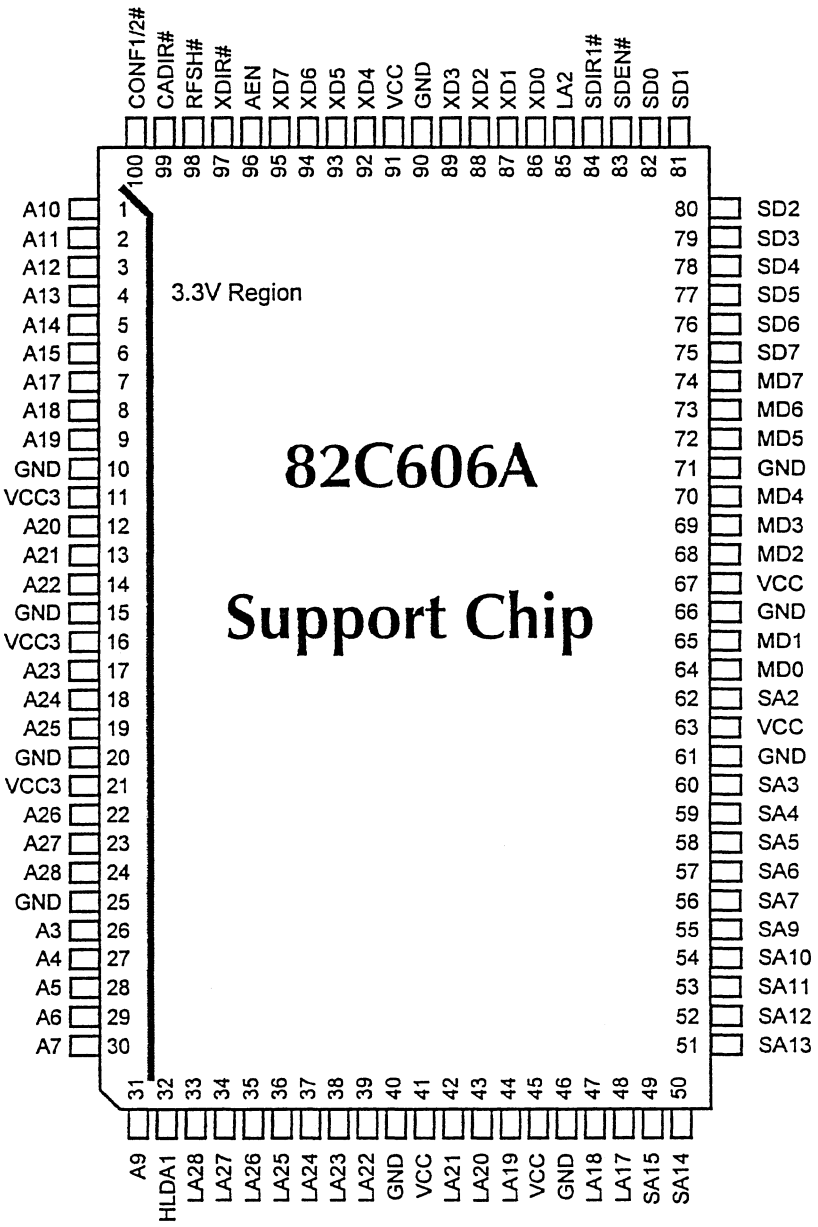


Table 3-5 82C606A Numerical Pin Cross-Reference

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	A10	26	A3	51	SA13	76	SD6
2	A11	27	A4	52	SA12	77	SD5
3	A12	28	A5	53	SA11	78	SD4
4	A13	29	A6	54	SA10	79	SD3
5	A14	30	A7	55	SA9	80	SD2
6	A15	31	A9	56	SA7	81	SD1
7	A17	32	HLDA1	57	SA6	82	SD0
8	A18	33	LA28	58	SA5	83	SDEN#
9	A19	34	LA27	59	SA4	84	SDIR1#
10	GND	35	LA26	60	SA3	85	LA2
11	VCC3	36	LA25	61	GND	86	XD0
12	A20	37	LA24	62	VCC	87	XD1
13	A21	38	LA23	63	SA2	88	XD2
14	A22	39	LA22	64	MD0	89	XD3
15	GND	40	GND	65	MD1	90	GND
16	VCC3	41	VCC	66	GND	91	VCC
17	A23	42	LA21	67	VCC	92	XD4
18	A24	43	LA20	68	MD2	93	XD5
19	A25	44	LA19	69	MD3	94	XD6
20	GND	45	VCC	70	MD4	95	XD7
21	VCC3	46	GND	71	GND	96	AEN
22	A26	47	LA18	72	MD5	97	XDIR#
23	A27	48	LA17	73	MD6	98	RFSH#
24	A28	49	SA15	74	MD7	99	CADIR#
25	GND	50	SA14	75	SD7	100	CONF1/2#

Table 3-6 82C606A Alphabetical Pin Cross-Reference

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A3	26	CADIR#	99	LA28	33	SD2	80
A4	27	CONF1/2#	100	MD0	64	SD3	79
A5	28	GND	10	MD1	65	SD4	78
A6	29	GND	15	MD2	68	SD5	77
A7	30	GND	20	MD3	69	SD6	76
A9	31	GND	25	MD4	70	SD7	75
A10	1	GND	40	MD5	72	SDEN#	83
A11	2	GND	46	MD6	73	SDIR1#	84
A12	3	GND	61	MD7	74	VCC	41
A13	4	GND	66	RFSH#	98	VCC	45
A14	5	GND	71	SA2	63	VCC	62
A15	6	GND	90	SA3	60	VCC	67
A17	7	HLDA1	32	SA4	59	VCC	91
A18	8	LA2	85	SA5	58	VCC3	11
A19	9	LA17	48	SA6	57	VCC3	16
A20	12	LA18	47	SA7	56	VCC3	21
A21	13	LA19	44	SA9	55	XD0	86
A22	14	LA20	43	SA10	54	XD1	87
A23	17	LA21	42	SA11	53	XD2	88
A24	18	LA22	39	SA12	52	XD3	89
A25	19	LA23	38	SA13	51	XD4	92
A26	22	LA24	37	SA14	50	XD5	93
A27	23	LA25	36	SA15	49	XD6	94
A28	24	LA26	35	SD0	82	XD7	95
AEN	96	LA27	34	SD1	81	XDIR#	97

Figure 3-4 82C606B Pin Diagram

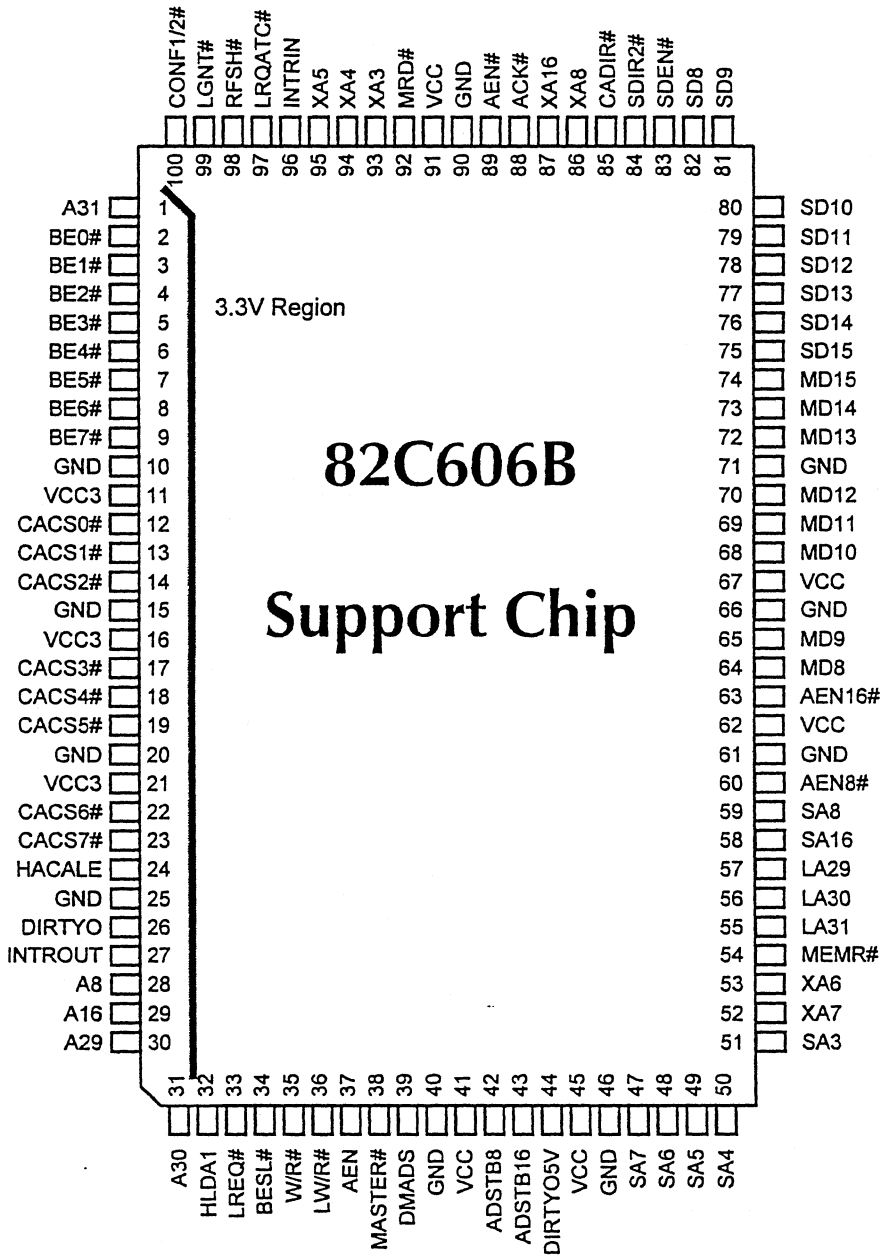


Table 3-7 82C606B Numerical Pin Cross-Reference

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	A31	26	DIRTYO	51	SA3	76	SD14
2	BE0#	27	INTROUT	52	XA7	77	SD13
3	BE1#	28	A8	53	XA6	78	SD12
4	BE2#	29	A16	54	MEMR#	79	SD11
5	BE3#	30	A29	55	LA31	80	SD10
6	BE4#	31	A30	56	LA30	81	SD9
7	BE5#	32	HLDA1	57	LA29	82	SD8
8	BE6#	33	LREQ#	58	SA16	83	SDEN#
9	BE7#	34	BESL#	59	SA8	84	SDIR2#
10	GND	35	W/R#	60	AEN8#	85	CADIR#
11	VCC3	36	LW/R#	61	GND	86	XA8
12	CACS0#	37	AEN	62	VCC	87	XA16
13	CACS1#	38	MASTER#	63	AEN16#	88	ACK#
14	CACS2#	39	DMADS	64	MD8	89	AEN#
15	GND	40	GND	65	MD9	90	GND
16	VCC3	41	VCC	66	GND	91	VCC
17	CACS3#	42	ADSTB8	67	VCC	92	MRD#
18	CACS4#	43	ADSTB16	68	MD10	93	XA3
19	CACS5#	44	DIRTYO5V	69	MD11	94	XA4
20	GND	45	VCC	70	MD12	95	XA5
21	VCC3	46	GND	71	GND	96	INTRIN
22	CACS6#	47	SA7	72	MD13	97	LRQATC#
23	CACS7#	48	SA6	73	MD14	98	RFSH#
24	HACALE	49	SA5	74	MD15	99	LGNT#
25	GND	50	SA4	75	SD15	100	CONF1/2#

Table 3-8 82C606B Alphabetical Pin Cross-Reference

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A8	28	CACS4#	18	LA31	55	SD9	81
A16	29	CACS5#	19	LGNT#	99	SD10	80
A29	30	CACS6#	22	LREQ#	33	SD11	79
A30	31	CACS7#	23	LRQATC#	97	SD12	78
A31	1	CADIR#	85	LW/R#	36	SD13	77
ACK#	88	CONF1/2#	100	MASTER#	38	SD14	76
ADSTB8	42	DIRTYO	26	MD8	64	SD15	75
ADSTB16	43	DIRTYO5V	44	MD9	65	SDEN#	83
AEN	37	DMADS	39	MD10	68	SDIR2#	84
AEN#	89	GND	10	MD11	69	VCC	45
AEN8#	60	GND	15	MD12	70	VCC	62
AEN16#	63	GND	20	MD13	72	VCC	67
BE0#	2	GND	25	MD14	73	VCC	83
BE1#	3	GND	40	MD15	74	VCC	91
BE2#	4	GND	46	MEMR#	54	VCC3	11
BE3#	5	GND	61	MRD#	92	VCC3	16
BE4#	6	GND	66	RFSH#	98	VCC3	21
BE5#	7	GND	71	SA3	51	W/R#	35
BE6#	8	GND	90	SA4	50	XA3	93
BE7#	9	HACALE	24	SA5	49	XA4	94
BESL#	34	HLDA1	32	SA6	48	XA5	95
CACS0#	12	INTRIN	96	SA7	47	XA6	53
CACS1#	13	INTROUT	27	SA8	59	XA7	52
CACS2	14	LA29	57	SA16	58	XA8	86
CACS3#	17	LA30	56	SD8	82	XA16	87

3.1 Signal Descriptions

3.1.1 82C546 ATC Signal Descriptions

Signal Name	Pin No.	Signal Type	Signal Description
3.1.1.1 Clock and Reset Interface Signals			
LCLK	16	I	**Local Bus Clock:** This clock is used by local bus devices and to derive the AT clock signal.
ATCLK	14	O	**AT Bus Clock:** Derived from an internal division of LCLK. ATCLK = LCLK/ 2,3,4,5.
RESET	48	I	**System Reset:** Output by the 82C547 (CPURST) in response to a PWRGD input.
3.1.1.2 Data Bus Interface Signals			
D[63:0] (3.3 V)	56:59, 62:68, 70:77, 79:86, 88:95, 98:104, 106:113, 115:118, 120:129	I/O	**CPU Data Bus:** These pins are connected directly to the CPU's data bus.
MD[63:0]	131:141, 143:146, 148:155, 157:163, 166:173, 175:182, 184:191, 193:199, 202:204	I/O	**Memory Data Bus:** These pins are connected directly to the system DRAM and are buffered to generate the ISA SD data bus and the local LD data bus.
PERR	47	O	**Parity Error:** Indicates that parity check detected a parity error during a read from the DRAM.

82C546 ATC Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
MP[7:0]	5:9, 11:13	I/O	**Memory Parity:** As outputs, these lines are only driven when DWE# is active. As inputs, they are used as strapping pins that are sampled at reset time to configure the 82C546 ATC as follows: **AT Clock Selection** **MP1 MP0 Selection** 0 0 LCLK/5 0 1 LCLK/4 1 0 LCLK/3 1 1 LCLK/2 **Back-to-Back AT I/O Cycle Select** **MP2 Function** 0 Slow - add 12 AT clocks to back-to-back I/O cycles 1 Fast - add 2 AT clocks to back-to-back I/O cycles **LDEV# Sample Select** **MP3 Function** 0 Sample LDEV# at the end of the second T2 1 Sample LDEV# at the end of the first T2 **Local Bus Disable Select** **MP4 Function** 0 VL bus disabled 1 VL bus enabled **Internal Test Mode Select** **MP5 Function** 0 Reserved 1 Normal Operation **82C546 Power Plane Select** **MP6 Function** 0 D[63:0] on 3.3V power plane for operation with 3.3V Pentium processor 1 D[63:0] on 5.0V power plane for operation with Pentium processor **82C822 Select** **MP7 Function** 0 82C822 is installed 1 82C822 is not installed
3.1.1.3 Local Bus Interface Signals			
LA2	4	I	**Local Bus Address Line 2:** This address line is used for address decoding and to distinguish high bytes[7:4] from low bytes[3:0] on the 64-bit address bus.
LBE[3:0]#	42, 44:46	I/O	**Local Byte Enable Bits 3 through 0:** Normally inputs, these signals become outputs during AT DMA or bus master cycles.
LADS#	41	I/O	**Local Bus Address Strobe:** Normally an input, this signal becomes an output during AT DMA or bus master cycles.
LRDY#	37	I/O	**Local Ready:** Normally an input, this signal will be driven when CPU, DMA, or AT masters are accessing AT slaves.

82C546 ATC Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
LM/IO#	40	I/O	**Local Memory/IO:** Normally an input, but becomes an output during AT DMA or bus master cycles.
LD/C#	36	I/O	**Local Data/Control:** Normally an input, becomes an output during AT DMA or bus master cycles.
LW/R#	39	I/O	**Local Write/Read:** Normally an input, becomes an output during AT DMA or bus master cycles.
LDEV#	21	I	**Local Device Indication:** Sampled if the cycle is not in the system memory area.
LDEN#	22	O	**Local Bus Data Buffer Enable:** Activated when: 1) CPU local bus write cycle 2) CPU local bus read from local device 3) AT DMA or master write cycle 4) AT DMA or master read from local device 5) Local bus master cycle
LDIR#	23	O	**Local Bus Data Buffer Direction Control:** Activated when: 1) CPU local bus read from local device 2) AT DMA or master read from local device 3) Normally is low for local bus master and becomes high for local bus master read cycle
3.1.1.4 Buffer Control Interface Signals			
MDHDOE#	33	I	**Memory Data to Host Data Output Enable:** This is used by the 82C546 ATC to distinguish: 1) Reads from DRAM 2) Reads from local slave or local bus slave 3) INTA# cycles 4) Non-CPU cycles and secondary cache write-hits
HDMDOE#	32	I	**Host Data to Memory Data Output Enable:** This is used by the 82C546 ATC to distinguish: 1) Writes to DRAM 2) Non CPU cycles and secondary cache read-hits
DLE#	35	I	**Data Latch Enable:** This is used by the 82C546 ATC to distinguish: 1) Writes to DRAM 2) Reads from DRAM 3) Read DRAM parity data
SDEN#	205	O	**System Data Bus Output Enable:** Output enable signal for the buffers between the MD and SD data buses.
SDIR1#	206	O	**Direction Control #1:** Direction control for the buffer between the MD[7:0] and SD[7:0] data buses.

82C546 ATC Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
SDIR2#	207	O	**Direction Control #2:** Direction control for the buffer between the MD[15:8] and SD[15:8] data buses.
3.1.1.5 Bus Arbitration Interface Signals			
AEN8#	55	I	**Address Enable 8-Bit:** The 82C547 SYSC monitors this signal to decode 8-bit DMA cycles.
AEN16#	54	I	**Address Enable 16-Bit:** The 82C547 SYSC monitors this signal to decode 16-bit DMA cycles.
RFSH#	29	I	**Refresh:** This signal is used by the ATC to distinguish AT refresh cycles and DMA or master cycles.
BOFF#	49	I	**Back-off:** This signal indicates that an inquire cycle is in progress.
LREQ#	52	I	**Local Bus Master Request:** Local bus master cycle request from a bus master on the local bus.
HLDA1	53	I	**AT DMA or Master Hold Acknowledge:** Indicates a hold acknowledge in response to a DMA or master hold request.
3.1.1.6 AT Bus Interface Signals			
XA0	2	I/O	**System Address XA0:** This signal is an output except during master or 8-bit DMA cycles when it serves as an input.
XA1	3	I/O	**System Address XA1:** This signal is an output except during master or DMA cycles when it serves as an input.
CHRDY	18	I/O	**Channel Ready:** This is normally an input from the AT bus which is pulled low (not ready) by a slow memory or I/O device to lengthen memory or I/O cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a read/write command. This pin becomes an output when AT DMA or a master accesses local memory or a local I/O device, and will be driven low until LRDY# is received. This is a Schmitt-trigger input pin.
0WS#	17	I	**Zero Wait State:** This input is from the AT bus and is a Schmitt-trigger input pin.
IO16#	20	I/O	**16-bit I/O Slave:** AT bus signal to indicate a 16-bit I/O slave is responding. This is a Schmitt-trigger input pin.
M16#	19	I/O	**16-bit Memory Slave:** An AT bus signal which indicates that a 16-bit memory slave is responding. M16# is normally an input, however, it becomes an output when a master accesses local memory. This is a Schmitt-trigger input pin.
IORD#	27	I/O	**AT I/O Read:** Normally an output, this pin becomes an input during master and DMA cycles.
IOWR#	28	I/O	**AT I/O Write:** Normally an output, this pin becomes an input during master and DMA cycles.
MRD#	24	I/O	**AT Memory Read:** Normally an output, this pin becomes an input during master and DMA cycles.

S82C546 ATC Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
MWR#	25	I/O	**AT Memory Write:** Normally an output, this pin becomes an input during master and DMA cycles.
ALE	30	O	**Address Latch Enable:** ALE indicates the start of an AT cycle and is externally buffered before connection to the AT bus. It is high during non-CPU cycles.
SBHE#	1	I/O	**System Byte High Enable:** Indicates a transfer on the upper bytes of the AT data bus SD[15:8]. Normally an output, this pin becomes an input during master cycles.
3.1.1.7 Miscellaneous Interface Signals			
KBDCS#	208	O	**Keyboard Controller Chip Select:** The 82C547 SYSC decodes accesses to the keyboard controller and issues this chip select signal when necessary.
INTA#	51	O	**Interrupt Acknowledge:** This signal goes to the 82C206 IPC to indicate that the processor is executing an interrupt acknowledge cycle.
DWE#	34	I	**DRAM Write Enable:** Used to enable the memory parity bits, MP[7:0].
LMEM#	31	I	**Local Memory Accessed Indication:** This signal is used for two purposes. The first is for generating M16# during AT master cycles. Secondly, this serves as a local device indication during local bus master cycles.
P6X#/LMCS#	50	I	**Port 6Xh Address Decode:** This signal is asserted on all memory accesses below 1MB. Port 6Xh is decoded as follows: A[15:7] = 0 A[6:5] = 1 A[4:3] = 0 Others bits = don't care.
3.1.1.8 Power and Ground Pins			
GND	15, 38, 60, 69, 87, 96, 105, 119, 142, 156, 164, 174, 192, 200	I	**Ground Connection**
VCC	10, 26, 43, 130, 147, 165, 183, 201	I	**Power Connection:** +5.0V
VCC3	61, 78, 97, 114	I	**Power Connection:** +3.3V

3.1.2 82C547 SYSC Signal Descriptions

Signal Name	Pin No.	Signal Type	Signal Description
3.1.2.1 Clock and Reset Interface Signals			
PWRGD	4	I	**Power Good:** This input reflects the "wired-OR" status of the external reset switch and Power Good status from power supply.
CPURST (3.3V)	49	O	**CPU Reset:** When active (high), this signal resets the CPU. CPURST is active in response to PWRGD only and is guaranteed to be active for 1 ms such that CLK and VCC are stable.
INIT	51	O	**CPU Initialize:** Emulated keyboard reset, I/O Port 92h bit 0's low-to-high transition or a Shutdown cycle will trigger INIT. INIT will be valid for a minimum of 16 CLKs when active.
CLK	149	I	**Clock:** This input is used as the master single frequency clock to the 82C547 SYSC.
ECLK	151	I	**Early Clock:** This clock should be two to five ns earlier than CLK.
LCLK	159	I/O	**Local Bus Clock:** This clock is used by local bus devices. Depending upon strapping of the XD1 pin at power-on reset, this can be either an input or output. LCLK = CLK/2.
OSCI	160	I	**Oscillator Input:** This 14.31818MHz oscillator input monitors the AT bus oscillator frequency. It provides the clock source for the OSC12 output. OSCI must be externally buffered to provide adequate drive for the AT bus.
OSC12	2	O	**Oscillator divided by 12:** OSCI is internally divided by 12 to provide this 1.19MHz output for use in the PC/AT counter/timer subsystem in the 82C206 IPC.
3.1.2.2 Data Bus Interface Signals			
A[26:24], A[16:8] (3.3V)	37:35, 26:21, 19:17	I/O	**CPU Address Bus:** Normally inputs, these pins are driven out during DMA cycles to snoop the internal Pentium processor cache
A[23:17], A[7:3] (3.3V)	34:31, 29:27, 16:12	I	**CPU Address Bus:** Inputs only, these pins are not driven during DMA cycles.
DRAM#	48	I	**DRAM Status:** This is a status signal to indicate that CPU address lines A[31:27] are all low. A single level of external decoding can be used if complete decoding is required. DRAM# must be asserted to enable the DRAM and cache controllers.
BE[7:0]# (3.3V)	38:40, 42:46	I/O	**CPU Byte Enable Bits 7 through 0:** These eight signals identify the byte(s) involved in a data transfer. They are inputs for CPU cycles and outputs for master and DMA cycles.
M/IO#	57	I	**Memory/IO:** CPU memory or I/O access indication. This signal along with D/C#, W/R#, and BE[7:0]# comprise the bus definition signals used to decode the type of cycle in progress.
D/C#	56	I	**Data/Control:** CPU data or control status. This signal along with M/IO#, W/R#, and BE[7:0]# comprise the primary bus signals used to decode the type of cycle in progress.

82C547 SYSC Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
W/R#	9	I	**Write/Read:** CPU write or read cycle status. This signal along with M/IO#, D/C#, and BE[7:0]# comprise the primary bus signals used to decode the type of cycle in progress.
ADS#	8	I	**Address Status:** Input from the CPU to indicate valid address and bus cycle definition is present on the bus.
BRDY# (3.3V)	61	O	**Burst Ready:** The CPU's burst ready input. Used by the chipset to terminate all cycles on the bus.
NA# (3.3V)	54	O	**Next Address:** This signal is connected to the CPU's NA# pin to request pipelined addressing for local memory cycles.
KEN#/ LMEM# (3.3V)	67	O	**Cache Enable and Local Memory:** This pin is connected to the KEN# input of the Pentium processor and is used to determine whether the current cycle is cacheable. This signal is also the local memory access signal and indicates a local DRAM cycle for the 82C546 ATC.
EADS#/WT#	55	O	**External Address Valid and Write Control:** This output has two functions. It indicates that a valid address has been driven onto the Pentium processor address bus by an external device. This address will be used to perform an internal cache invalidation cycle when the Pentium processor samples EADS# active. It is also used to control write-back or write-through policy for the primary cache during CPU cycles.
FERR#	52	I	**Floating Point Coprocessor Error:** This input causes two operations to occur. IRQ13# is triggered and IGERR# is enabled. An I/O write to Port F0h will set IGERR# low when FERR# is low.
HITM#	11	I	**Hit Internal Cache:** Indicates that the CPU has had a hit on a modified line in its internal cache during an inquire cycle. Used to prepare for write-back.
CACHE#	47	I	**Cacheable Cycle:** Used to indicate a cacheable cycle. Indicates the CPU will be doing a burst read or write.
A20M# (3.3V)	62	O	**CPU Gate A20 Control:** This signal is derived from keyboard GATEA20 emulation and Port 92h, bit 1.
IGERR# (3.3V)	53	O	**Ignore Coprocessor Error:** Normally high, after FERR# goes low and an I/O write to Port F0h, IGERR# will go low. When FERR# goes high, IGERR# is driven high.
IRQ13	7	O	**Numeric Coprocessor Interrupt Request:** An FERR# forces IRQ13 high and an I/O write to F0h resets it low.
3.1.2.3 VL Bus Interface Signals			
LA2	147	I/O	**Local Bus Address Line 2:** Derived from the CPU byte enables BE[7:0]# and driven out during CPU cycles. LA2 becomes an input during non-CPU cycles.
LBE[3:0]#	155:158	I/O	**Local Byte Enables 3 through 0:** Derived from the CPU byte enables BE[7:0]# and driven out during CPU cycles. Becomes an input during non-CPU cycles.

82C547 SYSC Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
LADS#	5	I/O	**Local Bus Address Strobe:** During CPU cycles when the 82C547 SYSC detects that the current cycle is not accessing local memory (cache and DRAM), it will start a local bus cycle by sending out LADS#. Two local cycles might be necessary when the CPU accesses more than four bytes of data. During non-CPU cycles, the 82C547 SYSC monitors LADS# to respond to a local memory access request.
LRDY#	6	I/O	**Local Ready:** The local bus cycle will be terminated by asserting LRDY# during a CPU cycle. The 82C547 SYSC terminates local memory (primary cache, secondary cache, and DRAM) requests by asserting LRDY# when other masters own the bus.
LM/IO#	152	I/O	**Local Memory/IO:** Local memory or I/O access indication. This signal along with LD/C#, LW/R#, and LBE[3:0]# comprise the primary bus definition signals used to decode the type of local cycle in progress. This pin is an output during CPU cycles and an input during non-CPU cycles.
LD/C#	154	I/O	**Local Data/Control:** Local data or control status. This signal along with LM/IO#, LW/R#, and LBE[3:0]# comprise the primary bus signals used to decode the type of local cycle in progress. This pin is an output during CPU cycles and an input during non-CPU cycles.
LW/R#	153	I/O	**Local Write/Read:** Local write or read cycle status. This signal along with LM/IO#, LD/C#, and LBE[3:0]# comprise the primary bus signals used to decode the type of local cycle in progress. This pin is an output during CPU cycles and an input during non-CPU cycles.
3.1.2.4 Cache Interface Signals			
ECDOE# (3.3V)	73	O	**Even Bank Cache Output Enable:** This external cache output enable strobe corresponds to one bank of 64-bit data.
OCDOE# (3.3V)	74	O	**Odd Bank Cache Output Enable:** This external cache output enable strobe corresponds to one bank of 64-bit data.
ECAWE# (3.3V)	69	O	**Even Bank Cache Write Enable:** This external cache write enable strobe corresponds to one bank of 64-bit data.
OCAWE# (3.3V)	71	O	**Odd Bank Cache Write Enable:** This external cache write enable strobe corresponds to one bank of 64-bit data.
TAGWE# (3.3V)	85	O	**Tag RAM Write Enable:** This control strobe is used to update the tag RAM with the valid tag of the accessed cache line during external cache read-miss cycles.
DIRTYWE# (3.3V)	86	O	**Dirty RAM Write Enable:** This control strobe is used to update the dirty bit RAM when a cache write hit occurs. A cache write hit will set the dirty bit for the currently accessed cache line.
TAG[7:0] (3.3V)	83:82, 80:75	I/O	**Tag RAM Data Bits 7 through 0:** Normally these bits are input signals, however, they become outputs whenever TAGWE# is activated to write new tags to the tag RAM.
DIRTY	84	I	**Dirty Bit:** This input signal represents the dirty bit of the tag RAM and is used to indicate whether a corresponding cache line has been over-written.

82C547 SYSC Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
ECA4 (3.3V)	59	O	**Even Cache Address 4:** Connected to the cache SRAMs address bit 4 of the even bank.
OCA4 (3.3V)	58	O	**Odd Cache Address 4:** Connected to the cache SRAMs address bit 4 of the odd bank.
HACALE (3.3V)	68	O	**Cache Address Latch Enable:** Used to latch the cache address into a transparent latch.
BESL# (3.3V)	88	O	**Byte Enables Selected Low:** Normally low, this signal is driven high during CPU write cycles and non-CPU cycles.
3.1.2.5 System DRAM Interface Signals			
DWE#	95	O	**DRAM Write Enable:** This signal is typically buffered externally before connection to the WE# input of the DRAMs.
RAS[3:0]#	108:106, 104	O	**Row Address Strobe Bits 3 through 0:** Each RAS# signal corresponds to a unique DRAM bank. These signals are typically not buffered externally before connection to the RAS# input of the DRAMs.
CAS[7:0]#	105, 103:101, 99:96	O	**Column Address Strobe Bits 7 through 0:** The CAS# outputs correspond to the eight bytes for DRAM Banks 0 and 1. Each DRAM bank has a 64-bit data bus. These signals are typically connected directly to the DRAMs through a damping resistor.
MA[10:0]	109, 111:120	O	**Memory Address Bus Bits 10 through 0:** This bus is the multiplexed row/column address lines to the DRAM.
PERR	87	I	**Parity Error:** This input signal from the 82C546 ATC is qualified by the internal parity checking signal to generate an NMI if parity checking is enabled and a parity error occurs.
3.1.2.6 Bus Arbitration Interface Signals			
HRQ	139	I	**Hold Request:** An input from the 82C206 IPC requesting a DMA or master cycle.
HOLD (3.3V)	65	O	**CPU Hold Request:** This output signal is connected to the HOLD input of the CPU and is used to request that the CPU allow another bus master complete control of its buses. In response to HOLD going active, the CPU will float most of its output and I/O pins and then assert HLDA.
HLDA	66	I	**Hold Acknowledge:** This input is connected to the CPU's HLDA line and indicates when the CPU has relinquished bus control to a local bus master.
HLDA1	94	O	**Bus Master Request Acknowledge:** This output is high for HRQ. HLDA1 indicates a hold acknowledge in response to a DMA or master hold request.
AEN8#	145	I	**8-bit Address Enable:** The 82C547 SYSC monitors this signal to decode 8-bit DMA cycles.
AEN16#	144	I	**16-bit Address Enable:** The 82C547 SYSC monitors this signal to decode 16-bit DMA cycles.

82C547 SYSC Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
RFSH#	131	I/O	**Refresh:** Normally, this is an output to indicate AT refresh cycles, however, it becomes an input signal during DMA or master cycles. The refresh interrupt request comes from the 8254 (integrated within the 82C206 IPC) via the OUT1 pin. In a PC/AT-compatible design, Timer1 (8254) is programmed as a rate generator to produce a 15 µs periodic signal used for interrupt requests for refresh cycles. If slow refresh DRAMs are being used, this period may be programmed to 60 µs.
AHOLD (3.3V)	64	O	**CPU Address Hold:** Used to tristate the CPU's address bus for internal cache snooping.
BOFF# (3.3V)	63	O	**CPU Back-off:** Used to abort the current CPU cycle.
LREQ#	3	I	**Local Bus Master Request:** A local bus master cycle request from a bus master on the local bus. LREQ# is asserted when the local bus master needs control of the local bus.
LGNT#	134	O	**Local Bus Master Grant:** This signal indicates that the local bus master has control of the local bus.
REFREQ	133	I	**Refresh Request:** A refresh request signal from the 82C206 IPC.
3.1.2.7 Data Buffer Interface Signals			
MDHDOE#	93	O	**Memory Data to Host Data Output Enable:** This signal is asserted on CPU reads from DRAM, reads from a local or AT bus slave, and INTA cycles. This signal is also asserted on writes to the cache if there is a cache hit.
HDMDOE#	91	O	**Host Data to Memory Data Output Enable:** This signal is asserted on writes to DRAM.
DLE#	92	O	**Data Latch Enable:** This signal is asserted on DRAM reads and writes.
3.1.2.8 Miscellaneous Interface Signals			
NMI (3.3V)	72	O	**Non-Maskable Interrupt:** This signal is activated when a parity error from a local memory read is detected or when the CHCK# signal from the AT bus is asserted (and the corresponding control bit in Port B is also enabled).
TMRG2	141	O	**Timer 2 Gate Control:** This signal is used as the GATE2 input (for Counter2) into the 8254 counter/timer logic of the 82C206 IPC. In PC/AT-compatible designs, Counter2 is used in tone generation for the speaker.
SPKD	137	O	**Speaker Data:** SPKD is a function of OUT2 and Port 61h, bit 1.
OUT2	142	I	**Timer 2 Output:** This signal is used as the OUT2 input.
ASRTC	143	O	**Real-time Clock (RTC) Address Strobe:** This signal is asserted for accesses to the RTC or CMOS RAM of the 82C206 IPC. It is connected to the AS input of the 82C206 IPC.
DMADS	146	I	**DMA Address Strobe:** Used to latch XD[7:0] and convert to A[16:9] or A[15:8] depending on the status of ADSTB8 and ADSTB16 signals from the 82C206 IPC.

82C547 SYSC Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
CHCK#	138	I	**AT Channel Check:** An NMI will be generated if this signal is driven active and NMI and CHCK# are enabled in the internal registers of the 82C547 SYSC.
XDIR#	136	O	**XD Bus Direction Control:** This signal is asserted when accessing I/O ports below 100h, INTA# cycles, and ROMCS# cycles.
P6X#/LMCS#	135	O	**Port 6Xh Address Decode and Lower Megabyte Chip Select:** This signal is asserted on all memory accesses below 1MB. Port 6Xh Address is decoded as follows for I/O cycles: A[15:7] = 0, A[6:5] = 1, A[4:3] = 0, Other bits = don't care.
XD[7:0]	122:129	I/O	**XD Data Bus bits 7 through 0:** This bus serves several purposes. It is used for internal register programming, DMA address latching, and as the refresh address [9:2] during refresh cycles. **Power-on Reset strapping option:** XD0 = High, MDHDOE# goes high at end of last T2 XD0 = Low, MDHDOE# goes high at beginning of last T2 XD1 = High, LCLK is output = CLK/2 XD1 = Low, LCLK is input to 82C547 SYSC XD3 = High, fast VL bus clock disabled (40MHz) XD3 = Low, fast VL bus clock enabled (50MHz) XD4 = High, tag/dirty 5.0V devices XD4 = Low, tag/dirty 3.3V devices
ROMCS#	132	O	**BIOS ROM Chip Select:** Goes active on both reads and writes to the ROM area to support flash ROM support. Note that the ROM cycles will be treated as AT cycles.
IOWR#	89	I	**AT I/O Write:** This signal is used to intercept commands to I/O Ports 60h and 64h to emulate the keyboard controller, allowing the generation of the fast GATEA20 and fast INIT signals.
3.1.2.9 Ground and Power Pins			
GND	1, 10, 30, 50, 60, 70, 90, 110, 130, 150	I	**Ground Connection**
VCC	100, 121, 140, 148	I	**Power Connection:** +5.0V
VCC3	20, 41	I	**Power Connection:** +3.3V
VCC3A	81	I	**Power Connection +3.3Vor +5.0V:** Sets tag and dirty RAM device voltage types. Attach to 3.3V for 3.3V tag/dirty RAM or attach to 5.0V for 5.0V tag/dirty RAM.

3.1.3 82C606A Signal Descriptions

Signal Name	Pin No.	Signal Type	Signal Description
3.1.3.1 CPU Interface Signals			
A[28:17], A[15:9], A[7:3]	24:22, 19:17, 14:12, 9:1, 31:26	I/O	**CPU Address Bus Bits 28 through 3:** Normally inputs from the CPU, these pins are driven out during DMA and master cycles.
3.1.3.2 ISA/VL/Memory Bus Interface Signals			
SA[15:9], SA[7:2]	49:55, 56:60, 63	I/O	**ISA System Address Bus Bits 15 through 9 and 7 through 2:** These pins are normally outputs and become inputs during DMA and master cycles. This bus carries a portion of the ISA address bus needed to interface the 5.0 volt ISA bus to the 3.3 volt CPU address bus.
SD[7:0]	75:82	I/O	**ISA System Data Bus Bits 7 through 0:** Normally outputs, these pins become inputs during DMA and master cycles. This bus carries the lower 8-bits of the ISA data bus.
LA2	85	I/O	**VL Address Bus Bit 2:** This pin is normally an input and becomes an output during DMA and master cycles.
LA[28:17]	33:39, 42:44, 47, 48	I/O	**VL Address Bus Bits 28 through 17:** These pins are normally outputs and become inputs during DMA and master cycles. This bus carries a portion of the VL address bus needed to interface the 5.0 volt VL bus to the 3.3 volt CPU address bus.
MD[7:0]	74:72 70:68, 65, 64	I/O	**Memory Data Bus Bits 7 through 0:** These pins are inputs during ISA and VL bus write cycles and become outputs during ISA and VL bus read cycles.
XD[7:0]	95:92, 89:86	I/O	**XD Bus Bits 7 through 0:** This bus carries the DMA latched address and is used for the refresh address bits [9:2] during refresh cycles.
HLDA1	32	I	**AT DMA or Master Hold Acknowledge:** Indicates a hold acknowledge in response to a DMA or master hold request.
3.1.3.3 Buffer Control Interface Signals			
AEN	96	I	**DMA Address Enable:** This input indicates that a DMA or refresh cycle is taking place and is used to tristate the 82C606A pins for the SD/XD internal logic.
CADIR#	99	I	**CPU Address Direction:** This input is used to control the bidirectional data buffers between the CPU address bus and the ISA/VL address buses. This input is high during CPU cycles and goes low during master cycles.
CONF1/2#	100	I	**Configuration Select:** This input is used to select whether the 82C606 operates in the A or B configuration. Pulling this input high will cause the device to operate as an 82C606A and tying this pin to ground will cause the device to operate as an 82C606B.
RFSH#	98	I	**Refresh:** This input is used to tri-state out the ISA and VL address bus drivers during refresh cycles. This signal is also used to drive XD[5:0] onto the SA[7:2] pins for the current refresh address.

82C606A Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
SDEN#	83	I	**SD Bus Output Enable:** This input is used to enable the buffer between the MD[7:0] and SD[7:0] data buses.
SDIR1#	84	I	**Direction Control #1:** This input is used to control the data path direction for the buffer between the MD[7:0] and SD[7:0] data buses.
XDIR#	97	I	**XD Bus Direction:** This input signal is used to control the direction of the data buffer between the XD[7:0] and SD[7:0] buses. The data direction is XD-to-SD when the input is low and SD-to-XD when the input is high.
3.1.3.4 Ground and Power Pins			
GND	10, 15, 20, 25, 40, 46, 61, 66, 71, 90	I	**Ground Connection**
VCC	41, 45, 62, 67, 91	I	**Power Connection:** +5.0V
VCC3	11, 16, 21	I	**Power Connection:** +3.3V

3.1.4 82C606B Signal Definitions

Signal Name	Pin No.	Signal Type	Signal Description
3.1.4.1 CPU/Cache Interface Signals			
BE[7:0]#	9:2	I	**CPU Byte Enable Bits 7 through 0:** These inputs from the CPU are used to determine which cache byte or bytes are currently being read or written.
BESL#	34	I	**Byte Enable Select Low:** This input from the SYSC is used to enable all cache byte chip selects during cache read cycles. (Cache reads are performed eight bytes at a time).
CACS[7:0]#	23, 22, 19:17, 14:12	O	**Cache Chip Selects Bits 7 through 0:** These outputs are derived from the CPU byte enables for write cycles to the cache, and from the BESL# input for cache read cycles.
A[31:29], A16, A8,	1, 31, 30, 29, 28	I/O	**CPU Address Bus bits 31 through 29, 8, and 16:** Normally inputs from the CPU, these pins are driven out during DMA and master cycles. A8 and A16 are used to differentiate between 8- and 16-bit DMA and master cycles.
HACALE	24	I	**Cache Address Latch Enable:** This input is used to latch the CPU byte enables to generate the cache chip select outputs.
DIRTYO	26	O	**Dirty Bit Out:** This 3.3V output signal represents the dirty bit of the tag RAM and is used to indicate whether a corresponding cache line has been overwritten.
DIRTYO5V	44	O	**Dirty Bit Out 5.0V:** This is a 5.0V version of the DIRTYO signal.
3.1.4.2 ISA/VL Bus Interface Signals			
LA[31:29]	55:57	I/O	**VL Address Bus Bits 31 through 29:** These pins are normally outputs and become inputs during DMA and master cycles. This bus carries a portion of the VL address bus needed to interface the 5.0 volt VL bus to the 3.3 volt CPU address bus.
MD[15:8]	74:72, 70:68, 65, 64	I/O	**Memory Data Bus Bits 15 through 8:** This is the data bus interface which is used to generate the ISA SD data bus. Normally inputs, these pins become outputs during DMA and master cycles.
MEMR#	54	I/O	**ISA Memory Read:** This signal is the ISA bus memory read attached to the ISA bus. This pin becomes an input during master cycles.
MRD#	92	I/O	**ISA Memory Read:** This signal is the ISA bus memory read attached to the 82C546 ATC. This pin becomes an output during master cycles.
W/R#	35	I	**Write/Read:** CPU write or read cycle status. Used to generate the DIRTYO and DIRTYO5V signals.
SA[7:3]	47:51	O	**ISA System Address Bus Bits 7 through 3:** These pins are normally outputs and become inputs during DMA and master cycles. This bus carries a portion of the ISA address bus needed to interface the 5.0V ISA bus to the 3.3V CPU address bus.
SA8	59	I/O	**ISA System Address Bus Bit 8:** This pin is normally an output and is an input during master cycles. It is used to differentiate between 8- and 16-bit DMA cycles.
SA16	58	I/O	**ISA System Address Bus Bit 16:** This pin is normally an output and is an input during master cycles. It is used to differentiate between 8- and 16-bit DMA cycles.

82C606B Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
SD[15:8]	75:82	I/O	**ISA System Data Bus Bits 15 through 8:** This bus carries the 16-bit ISA data bus. These pins are normally outputs and become inputs during DMA and master cycles.
3.1.4.3 Buffer Control Interface Signals			
AEN8#	60	I	**Address Enable 8:** This input from the 82C206 IPC is used with the AEN16# input to control the steering logic for the CA8/XA8 and CA16/XA16 signal pins.
AEN16#	63	I	**Address Enable 16:** This input from the 82C206 IPC is used with the AEN8# input to control the steering logic for the CA8/XA8 and CA16/XA16 signal pins.
SDEN#	83	I	**ISA Data Bus Enable:** This input is used to enable the drivers for driving the ISA data bus from the MD bus.
SDIR2#	84	I	**ISA Data Bus Direction Control #2:** This bit is used to control the direction of the most significant byte of the ISA data bus to or from the MD bus.
XA[7:3]	52, 53, 95:93	I/O	**XA Bus Interface Bits 7 through 3:** These signals are outputs except during master or DMA cycles when they serve as inputs.
XA8	86	I/O	**XA Bus Interface Bit-8:** This bit is normally an output and becomes an input during 16-bit DMA and master cycles.
XA16	87	I/O	**XD Bus Interface Bit-16:** This bit is normally an output and becomes an input during 8-bit DMA and master cycles.
3.1.4.4 Miscellaneous Interface Signals			
ADSTB8	42	I	**Address Strobe 8:** This input from the 82C206 IPC indicates that an 8-bit DMA cycle is taking place.
ADSTB16	43	I	**Address Strobe 16:** This input from the 82C206 IPC indicates that a 16-bit DMA cycle is taking place.
AEN	37	O	**DMA Address Enable:** This output indicates that a DMA or refresh cycle is taking place.
AEN#	89	O	**DMA Address Enable:** This is an inverted version of AEN.
ACK#	88	O	**DMA Acknowledge:** This output goes low to indicate that an HLDA1 has been received for a pending DMA cycle.
CADIR#	85	O	**CPU Address Direction:** This output is used to control the data buffers between the CPU address bus and the ISA/VL address buses. This signal is high during CPU cycles and low during master cycles.
CONF1/2#	100	I	**Configuration Select Pin:** This input is used to select whether the 82C606 operates in the A or B configuration. Pulling this input high will cause the device to operate as an 82C606A and tying this pin to ground will cause the device to operate as an 82C606B.
DMADS	39	O	**DMA Address Strobe:** Indicates that the 82C206 IPC has a DMA cycle in progress.

82C606B Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
HLDA1	32	I	**Hold Acknowledge 1:** Indicates that the 82C547 SYSC has received a hold acknowledge in response to a DMA or master hold request.
INTRIN	96	I	**Interrupt In:** This input is attached to the INTR pin of the 82C206 IPC.
INTROUT	27	O	**Interrupt Out:** This output is connected to the INTR 3.3 volt input of the Pentium CPU and does the 5 volt to 3.3 volt level translation.
LGNT#	99	I	**Local Bus Master Grant:** This input is asserted when a local bus master needs control of the local bus.
LREQ#	33	I	**Local Bus Master Request:** This input is asserted when the local bus master gains control of the local bus.
LW/R#	36	I	**Local Write/Read:** Indicates the data direction for local bus cycles.
LRQATC#	97	O	**VL Local Request Latched:** This output is the latched local bus request and is asserted when the local bus master grant is received.
MASTER#	38	I	**Master Cycle in Progress:** This input indicates that an ISA bus master has gained control of the ISA bus.
RFSH#	98	I	**Refresh:** When asserted, this input indicates that a refresh cycle is in progress.
3.1.4.5 Ground and Power Pins			
GND	10, 15, 20, 25, 40, 46, 61, 66, 71, 90	I	**Ground Connection**
VCC	41, 45, 62, 67, 91	I	**Power Connection:** +5.0V
VCC3	11, 16, 21	I	**Power Connection:** +3.3V

4.0 Functional Description

A complete Pentium processor solution consists of:

- Python Chipset (82C546 ATC and 82C547 SYSC)
- 82C206 Integrated Peripherals Controller (IPC)
- 82606A or 82C606B Support Chips (eliminates eleven TTL devices on motherboard)

The sub-sections that follow will give detailed operational information on how these devices interact with each other and the Pentium microprocessor.

4.1 Reset Logic

The PWRGD input to the 82C547 SYSC is used to generate the CPU and the system reset (CPURST). PWRGD is a "cold reset" which is generated when either PWRGD goes low (from the power supply, indicating a low power condition) or the system reset button is activated. When PWRGD is sensed active, CPURST will go active and will remain active for at least 1ms after PWRGD goes inactive. Please refer to Figure 4-1.

The INIT signal is used to initialize the Pentium CPU during warm resets. INIT is generated for the following cases:

- When a shutdown condition is decoded from the CPU bus definition signals, the 82C547 SYSC will assert INIT for 15 T-states.
- Keyboard reset to I/O Port 64h.
- Fast reset to I/O Port 92h.

4.2 System Clocks

4.2.1 CPU and SYSC Clocks

The 82C547 SYSC uses two high frequency clock inputs, CLK and ECLK.

The clock signals that go to the CPU and the SYSC CLK inputs are required to be in the same phase and have minimum skew between them. The skew between the SYSC CLK and CPU clock must meet t100 timing requirement. The SYSC CLK is a single-phase clock which is used to sample all host CPU synchronous signals and for the 82C547's internal state machines.

ECLK is used for generating some critical signals for the host CPU and the cache/DRAM controller logic. ECLK is required to be in the same phase as CLK but ahead of CLK. The delay from ECLK to CLK must meet the delay timing of t101. Typically, one gate delay from ECLK to CLK meets the 82C547 CLK delay requirements. Figure 4-2 shows the typical CPU and SYSC clock distribution circuit.

4.2.2 VL Bus Clocks

The 82C546 and 82C547 require LCLK for the VL bus interface. The phase and frequency of LCLK to the chipset and the VL bus connector is required to be the same and the allowable skew between them must be within 2ns.

LCLK can be generated from the 82C547 or from an external clock source. LCLK's source and maximum speed is determined during the power-on reset (POR) sequence in the 82C547. Figure 4-4 gives the power-on reset and LCLK relationship.

When LCLK is generated from the 82C547 it will always be one-half of the CLK frequency. Distribution for an internal LCLK source is shown in Figure 4-3. For more than one VL bus slot, an external LCLK source is recommended. The clock distribution for such a method is shown in Figure 4-4.

Figure 4-1 Reset Timing

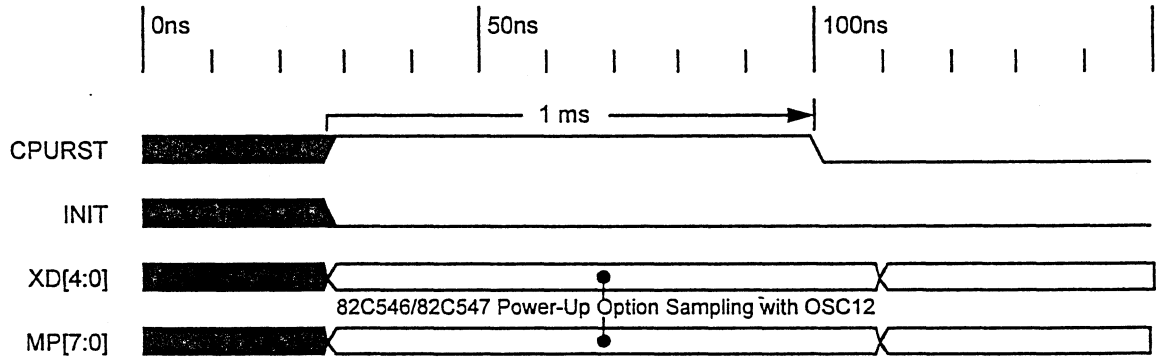


Figure 4-2 CPU and SYSC Clock Distribution

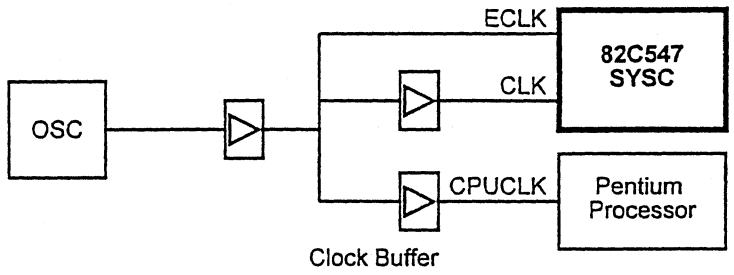


Figure 4-3 Clock Distribution Method for Single VL Bus Connector

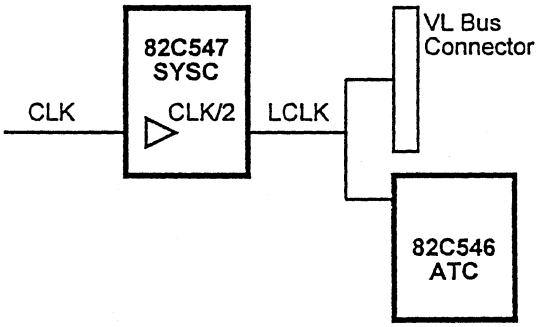


Figure 4-4 Clock Distribution Method for Multiple VL Bus Connectors

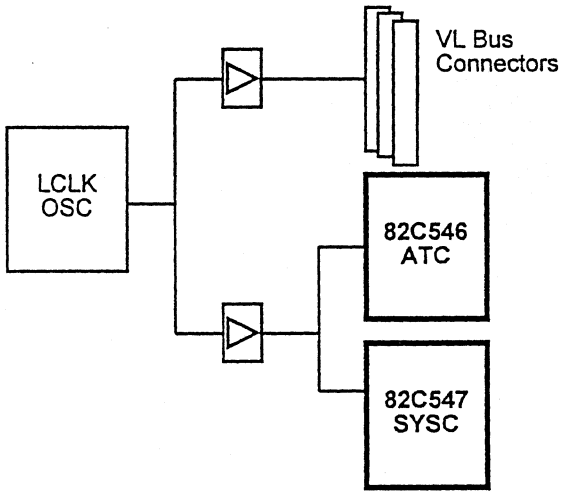


Table 4-1 Power-On Reset and LCK Relationship

Power-on Status		LCLK Source	LCLK Frequency	LCLK Buffer Direction in the 82C547
XD1	High	82C547	CLK2	Output
	Low	External	Required VL Bus Frequency	Input
XD3	High	50MHz Disabled	40MHz Maximum	
	Low	50MHz Enabled	50MHz Maximum	

4.2.3 AT Bus Clocks

The 82C546 generates the AT bus clock (ATCLK) from an internal division of LCLK. The ATCLK frequency is programmable and can be set to any of the four clock division options. The AT clock frequency is selected during the power-up reset sequence of the 82C546. This allows the system designer to tailor the AT bus clock frequency to support a wide range of system designs and performance platforms. Refer to Table 4-2

Table 4-2 Power-On Reset and LCLK to ATCLK Relationship

Power-On Status of				
MP1	MP0	LCKL Divisor	LCLK Frequency (MHz)	ATCLK Frequency (MHz)
0	0	LCLK/5	50 to 40	10 to 8
0	1	LCLK/4	33	8.25
1	0	LCLK/3	25 to 20	8.33 to 6.6
1	1	LCLK/2	20 to 16	10 to 8

4.3 Cache Subsystem

The integrated cache controller, which uses a direct-mapped, bank-interleaved scheme dramatically boosts the overall performance of the local memory subsystem by caching writes as well as reads (write-back modes). Cache memory can be configured as one or two banks and sizes of 64KB, 128KB, 256KB, 512KB, 1MB, and 2MB are supported. Two programmable non-cacheable regions are provided. The cache controller operates in non-pipeline or pipeline mode, with a fixed 32-byte line size (optimized to match a Pentium processor burst linefill) in order to simplify the motherboard's design without increasing cost or degrading system performance. The secondary cache operates independently and in addition to the CPU's internal cache.

The 82C547's cache controller has a built-in tag comparator which improves system performance while reducing component count on the system board. The controller features a 64-bit wide data bus with 32-byte CPU burst support. The controller supports cache sizes of 64KB, 128KB, 256KB, 512KB, 1MB, and 2MB. The schemes supported by the cache controller are: write-back and direct-mapped. An optional write-through operation is also supported.

The cache controller uses a 32-byte secondary cache line size. It supports read and write bursting in a 3-2-2-2 burst for cache reads and a 4-2-2-2 burst for writes. The 8-bit tag has a "dirty" bit option for the write-back cache. The cache controller uses standard 3.3V SRAMs in single or dual banks with interleaving for optimum cache performance.

The 82C547 SYSC has a strapping option through the VCC3A pin (pin 81) which allows the selection of 3.3 or 5.0 volt tag and dirty RAMs. Connecting the VCC3A pin to the 3.3V power plane allows the use of 3.3V RAMs. Connecting the VCC3A pin to the 5.0V power plane allows faster, lower-cost 5.0V tag and dirty RAMs to be used. Table 4-3 shows the power-on reset and I/O buffer selection.

Table 4-3 Power-On Reset and I/O Buffer Select

Power-On Status of XD4	I/O Buffer Selection
High	Tag and dirty SRAM selected as 5.0V devices.
Low	Tag and dirty SRAM selected as 3.3V devices.

4.3.1 CPU Burst Mode Control

The Python Chipset fully supports the 64-bit wide data path for the Pentium processor's burst read/write cycles. The 82C547's cache and DRAM controllers insure that data is burst into the CPU whenever the Pentium processor requests a burst linefill or a burst write to the system memory.

The 82C547 SYSC contains separate burst counters to support DRAM and external cache burst cycles. The DRAM controller performs a burst for the L2 cache read-miss linefill cycle (DRAM to L2 cache and CPU) and the cache controller burst supports the Pentium processor's burst linefill for the L2 cache hit cycle (L2 cache to the Pentium CPU). The Pentium CPU's quad-word burst address sequencing is used for all system memory burst cycles.

4.3.2 Cache Cycle Types

Listed below are some cache terminology and cycle definitions that are chipset specific:

- **Cache Hit/Miss Cycles:** These cycles generated by comparing the high-order address bits (for the memory cycle in progress) with the stored tag bits from previous cache entries. When a match is detected and the location is cacheable, a cache hit cycle takes place. If the comparator does not detect a match or a non-cacheable location is accessed (based on the internal non-cacheable region registers), then the current cycle is a cache miss.

  A cache hit/miss decision is always made at the end of the first T2 for a non-pipeline cycle and at the end of the first T2P for a pipeline cycle. This enables the SRAM read/write cycle to begin after the first T2 or T2P. The cacheable decision is based on the DRAM bank decodes and the chipset configuration registers for non-system memory areas and non-cacheable area definitions. If the access falls outside the system memory area, it is always non-cacheable.

- **Dirty Bit:** A mechanism for monitoring coherency between the cache and system memory. Each tag entry has a corresponding dirty bit to indicate whether the data in the represented cache line has been modified since it was loaded from system memory. This allows the 82C547 to determine whether the data in the system memory is "stale" and needs to be updated before a new memory location is allowed to overwrite the currently indexed cache entry.

- **Linefill Cycle:** This cycle occurs for a cache read-miss cycle. It is a data read of the new address from the system memory and a corresponding write to the cache. The tag data will also be updated with the new address.

- **Castout Cycle:** Occurs for a cache read-miss cycle, but only if the cache line that is being replaced is "dirty". In this cycle, the "dirty" cache line is read from the cache and written to the system memory. The upper address bits for this cycle are provided by the tag data bits.
- **Write-back Cycle:** A write-back consists of performing a castout cycle followed by a linefill cycle. The write-back cycle causes an entire cache line (32 bytes) to be written back to memory followed by a line burst from the new memory location into the cache and to the CPU simultaneously. The advantages of performing fast-write cycles to the cache (for a write-hit) typically outweigh the cycle overhead incurred by the write-back scheme.

4.3.3 Cache Operation

4.3.3.1 L2 Cache Read-Hit

In write-back or write-through modes, the secondary cycle provides data to the CPU. The 82C547 SYSC follows the Pentium CPU's burst protocol to fill the processor's internal cache line.

The cache controller will sample CACHE# from the CPU at the end of T1 and perform a burst read if CACHE# is sampled active. The first cache read-hit for a cycle is always one wait state. If a read cycle can be converted to a burst, the read cycle is extended for an additional three words continuing at one wait state per cycle. To achieve the burst at this rate, the hit or miss decision must be made before BRDY# is returned to the CPU at the end of the second T2. Please refer to Figure 4-5.

The cache hit comparator in the 82C547 SYSC compares the data from the tag RAM with the higher address bits from the CPU bus. The output of this comparator generates the BRDY# signal to the Pentium CPU. BRDY# will go inactive to add wait states depending on the number of wait states programmed. Refer to Table 4-4 for the tag compare table.

If two SRAM banks are used, address bit A4 from the CPU will be the least significant address bit that goes to the data SRAMs. The data output for each SRAM bank is controlled by a separate output enable for each SRAM bank (OCDOE# and ECDOE#). The OCDOE# and ECDOE# generation for the leadoff cycle is based on address bit A3 from the CPU. The two signals OCDOE# and ECDOE# will interleave the data read from the two cache banks in a burst cycle. If one SRAM bank is used, address bit A3 from the CPU will be the least significant address bit that goes to the SRAMs and the output enable ECDOE# will be active for the complete cycle.

4.3.3.2 L2 Cache Write-Hit Cycle

In the write-through mode, data is always written to the SRAM and to the system memory. The "dirty" bit is not used. When the write to the system memory is completed, BRDY# is returned to the CPU.

In the write-back mode for a write-hit case, the data is written only to the cache (the system memory is not updated) and the "dirty bit" is always made "dirty". To complete the leadoff cycle in four clocks, the "dirty" bit must be written within the specified time as shown in Figure 4-6. To facilitate this, the SRAM that contains the "dirty" bit has separate data-in and data-out pins.

The cache controller will sample CACHE# from the CPU at the end of T1 and execute a burst write if CACHE# is sampled active, otherwise the cycle will end in a single write. If two banks are used, the cycle is completed in a 4-2-2-2 burst. The write enable signals OCAWE# and ECAWE# to the SRAM banks are based on address bit A3 from the CPU and will interleave writes to the two banks. If a single bank is used, ECAWE# will remain active for the entire write cycle.

For writes, only the byte requested by the CPU can be written to the cache. This is done by using the BEx# from the CPU to control the SRAM chip selects.

Figure 4-5 L2 Cache Read-Hit Cycle

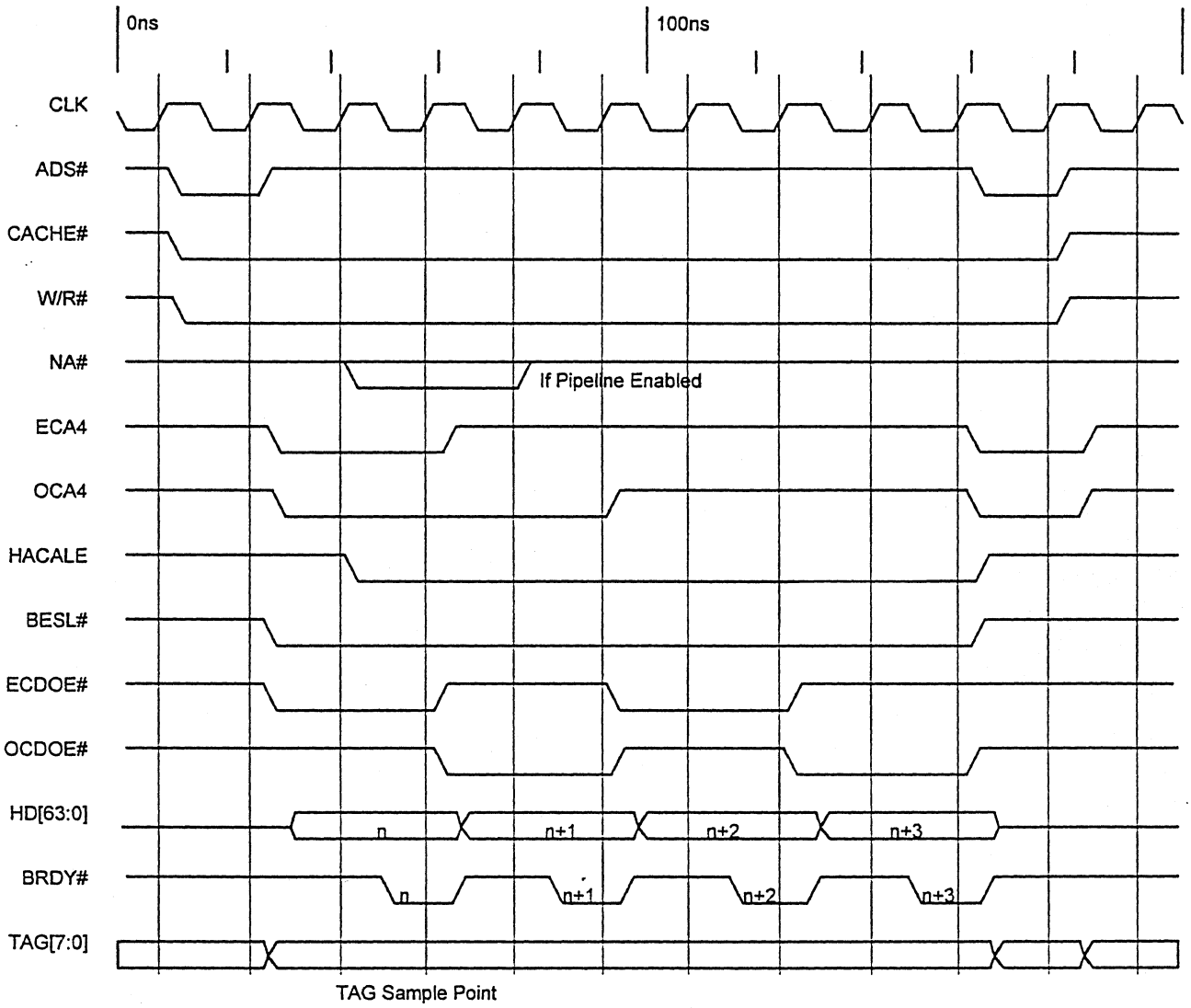


Figure 4-6 Write-Hit Burst Cycle for the Write-Back Mode (Double Bank)

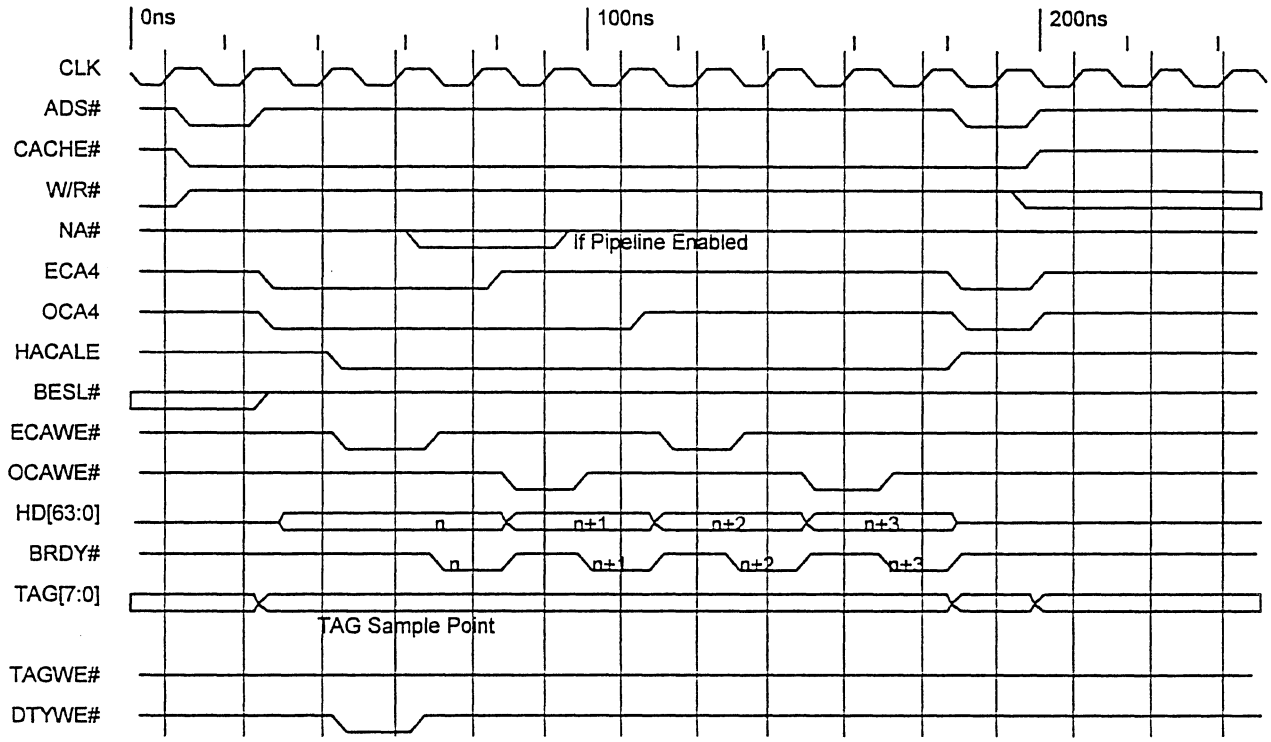
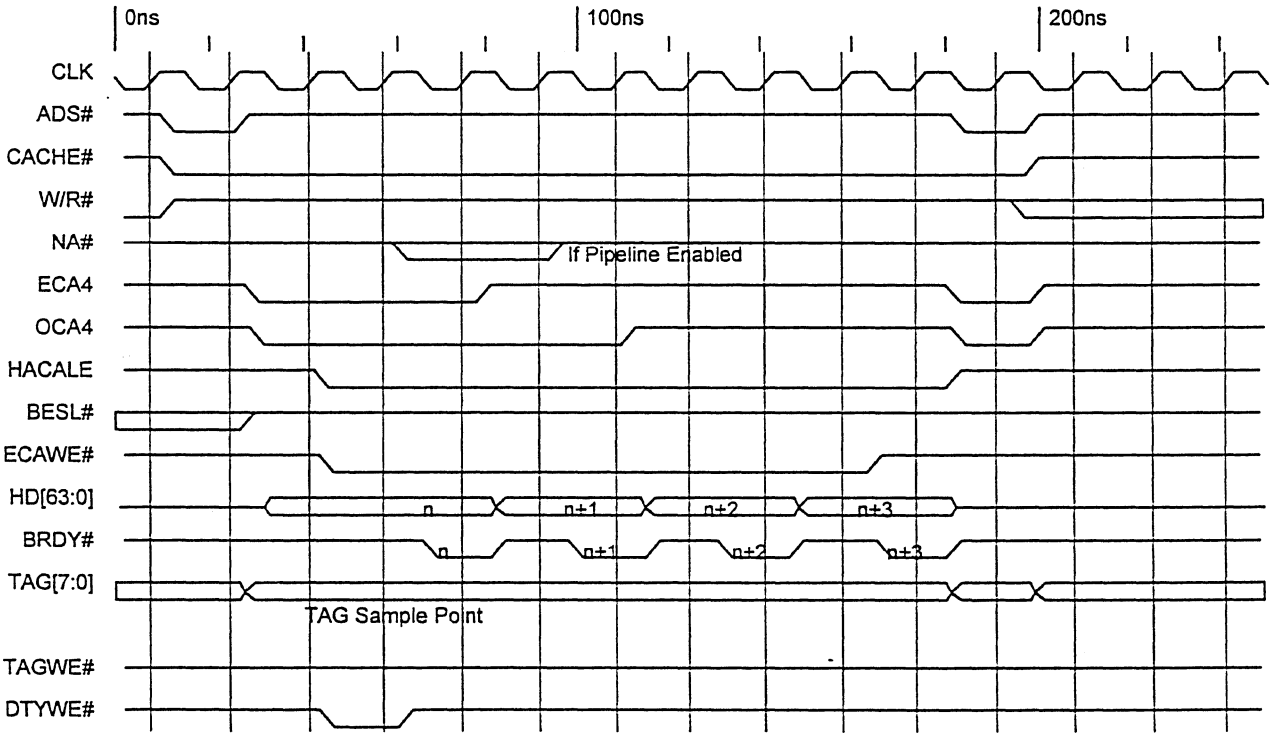


Figure 4-7 Write-Hit Burst Cycle for the Write-Back Mode (Single Bank)



4.3.3.3 L2 Cache Read-Miss

In the write-back mode there are two cache read-miss cases depending on the status of the "dirty" bit.

- **Case 1:** Read-miss of a "clean" cache line

In this case, only a linefill cycle is executed. The L2 cache line that is to be replaced with a new line from the DRAM will just be overwritten. The linefill cycle is done by reading the new data from the system memory first and then the data is simultaneously written to both the CPU (following burst protocol for the Pentium CPU) and to the secondary cache. Please refer to Figure 4-8.

The sequence for Case 1 linefill is:

System memory read transitions to write to the L2 cache + CPU read.

The cache controller will update the tag data bits and the "dirty" bit in the background during the linefill cycle. At the end of T1, if the CACHE# signal from the CPU is negated, a linefill cycle will not be executed. Instead, only the eight bytes requested by the CPU will be read from the system memory. The tag and the "dirty" bit will not be updated.

- **Case 2:** Read-miss with cache line "dirty"

The cache line for this case has been modified and valid data is only in the L2 cache. Before this line is overwritten in the cache, the modified line must first be written to the system memory by performing a castout cycle. After the completion of the castout cycle, a linefill cycle is executed. The linefill cycle is performed by reading the new data from the system memory and then simultaneously writing this data to the CPU (following burst protocol for the Pentium CPU) and to the secondary cache. Refer to Figure 4-9.

The sequence for Case 2 is:

Read the "dirty" line from the L2 cache transitions to write to the system memory transitions to a new line read from system memory transitions to write to the L2 cache + CPU read.

The cache controller will update the tag data bits and the "dirty" bit in the background during the castout cycle. If the CACHE# signal from the CPU is inactive, then the eight bytes requested by the CPU will be read from the system memory. The tag and the "dirty" bit are not updated. The exception to this type of handling for a non-burst request from the CPU is if the 82C547 SYSC is programmed with the L1 cache disabled and the L2 cache enabled in some address region. Please refer to Section 2.5.3.10, "Cacheability and Write Protection", Method 2 for this exception handling.

4.3.3.4 L2 Cache Write-Miss

In both the write-back or write-through modes the data is not written to the SRAM and the tag data remains unchanged. The data is written only to the system memory. Refer to Figure 4-10.

If the write buffer is available, it is stored there and the cycles are posted writes to the DRAM. If the target is a local peripheral or the AT bus, the cache controller will not be active.

Figure 4-8 L2 Cache Read-Miss Clean Burst of 8-3-3-3 (Linefill Cycle)

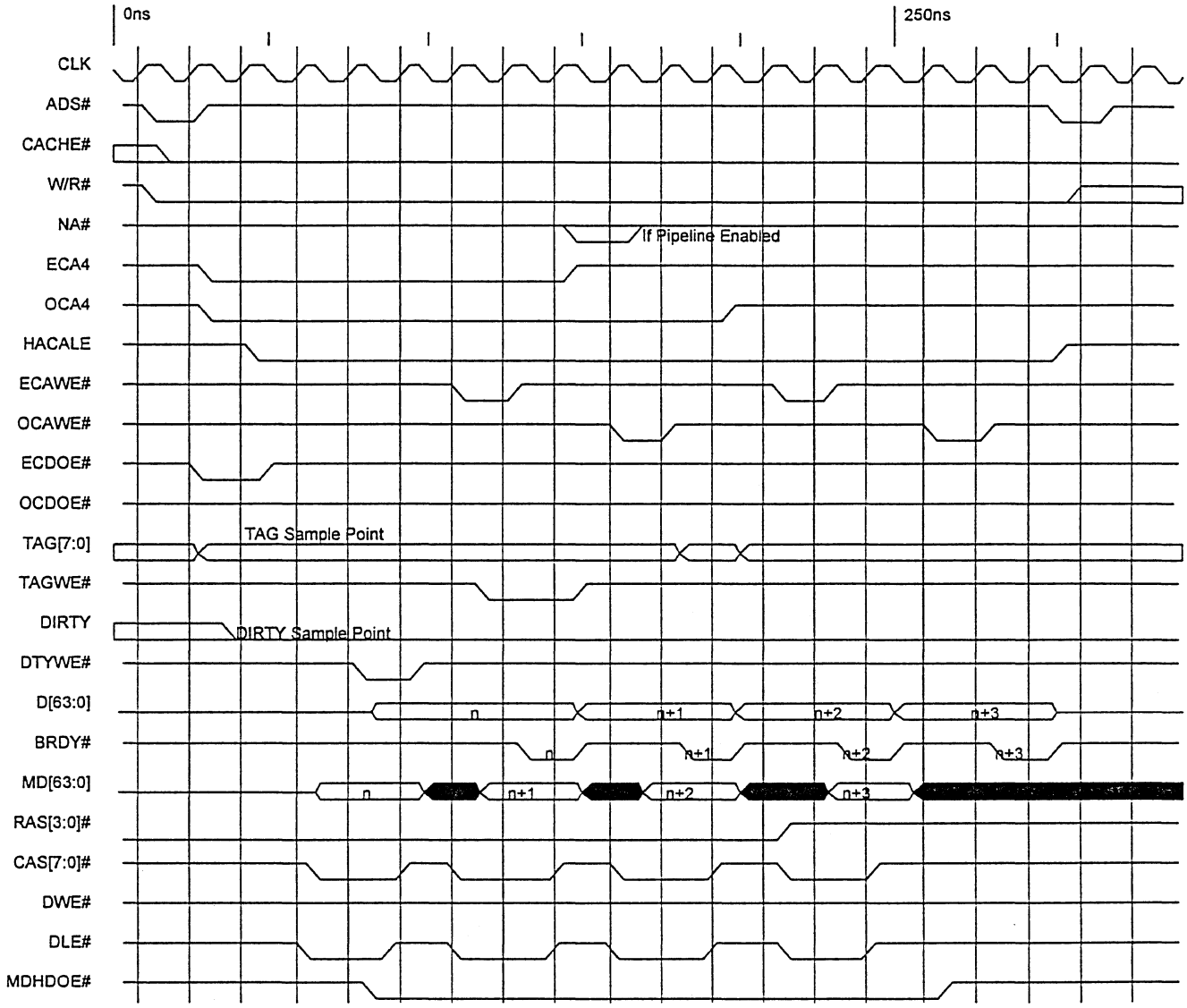
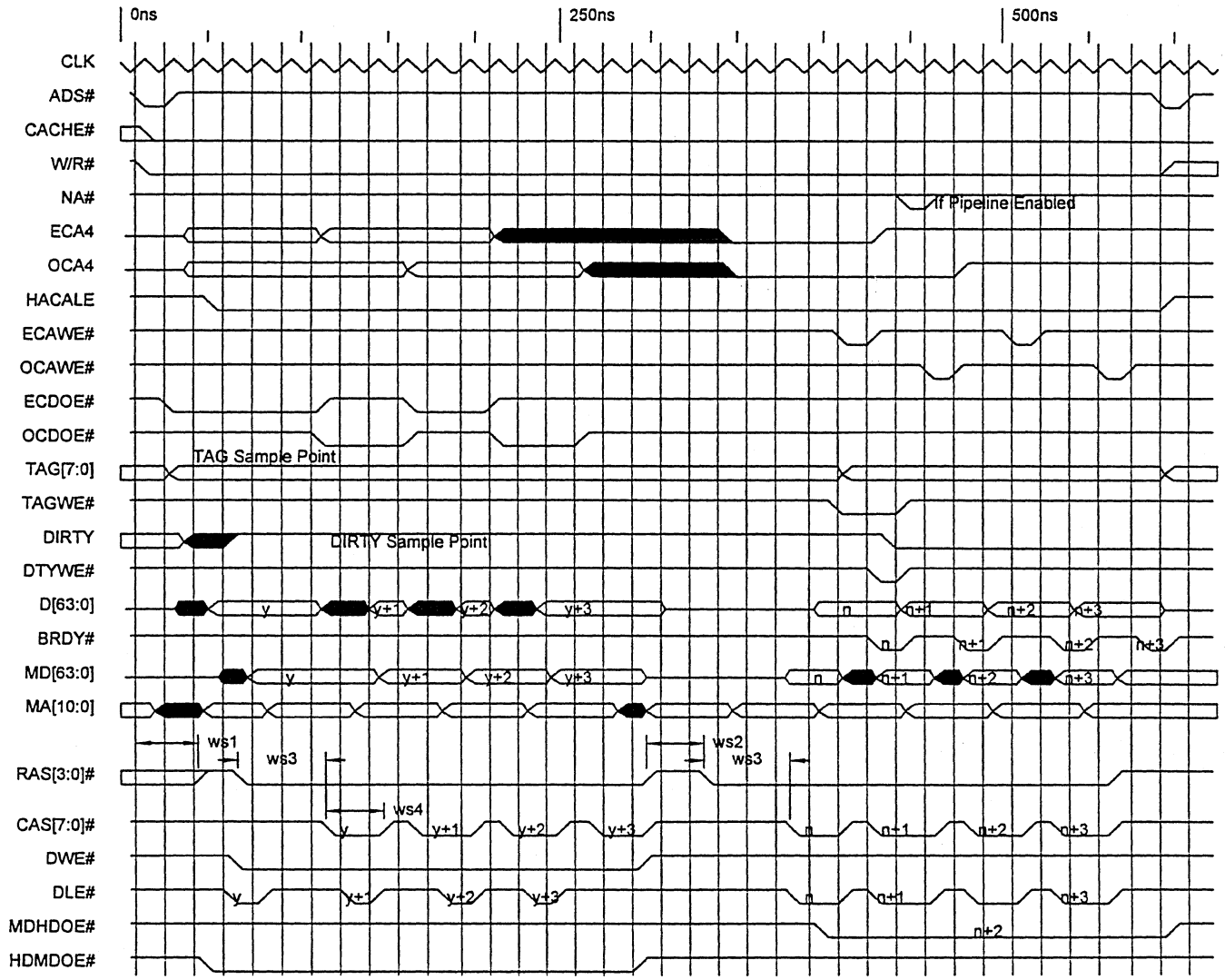
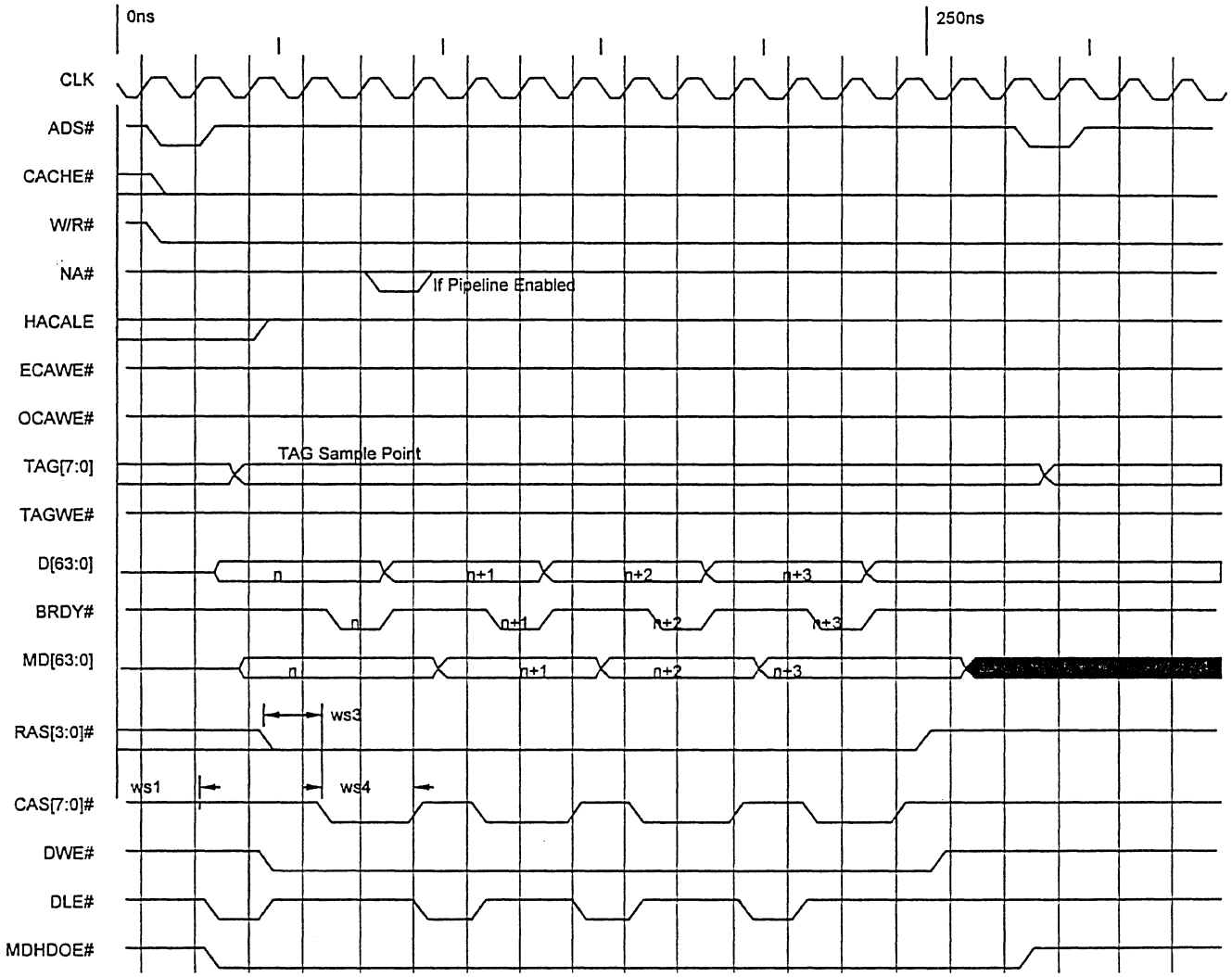


Figure 4-9 L2 Cache Read-Miss Dirty Cycle



Notes: ws1: Program 4 CLKs
ws3: Program 3-4 CLKs
ws4: Program 2-3 CLKs

Figure 4-10 L2 Cache Write-Miss Burst (4-3-3-3)



Notes: ws1: Program 3-4 CLKs
ws3: Program 3-4 CLKs
ws4: Program 2-3 CLKs

4.3.3.5 Tag Compare Table

The upper address bits used to compare for an L2 cache hit status will depend on the total L2 cache size. Table 4-4 shows the address bits from the CPU bus and the tag data bit used in the 82C547 SYSC's tag comparator. Figure 4-11 shows the block diagram of the L2 cache structure.

4.3.3.6 Cache Critical Paths

An external 74AHCT126 is used to enable the A3 and A4 address bits from the CPU to the SRAMs until the end of the first T2 for the leadoff cycle. At the end of the first T2, the cache controller will drive A3 and A4 to the SRAMs and HACALE will disable A3 and A4 from the CPU.

The critical path for the SRAM address access is the A3 and A4 bits and the data delay time. The address delay to the SRAMs is reduced to the 74AHCT126 control signal delay HACALE and the propagation delay through the 74AHCT126.

- MARGIN = (3 CLK) - (tHACALE + tAHCT126pd + tAASRAM + tPentium processor data setup)

The OE access time of the SRAMs is a critical path. It consists of the clock to OCDOE# and ECDOE# timing, the SRAM tOE timing and the CPU setup time.

- MARGIN = (2 CLK) - (tOE + tAOE SRAM + tPentium processor data setup)

The write pulse width is the critical SRAM parameter for writes, as well as the tag RAM read path. The hit/miss decision must be made and BRDY# driven active for the L2 cache read-hit case.

- MARGIN = (3 CLK) - (tPentium processor addr delay + tAASRAM + t587 TAG setup + tPentium processor BRDY# setup)

The chip select to each data SRAM is controlled by BESL# from the 82C547 SYSC and BEx# from the CPU. Since BESL# is normally active, the SRAM chip select will not be in the critical timing path for data access time during a read cycle. For write cycles, BESL# will go inactive with W/R# from the CPU and the write to the SRAM will be controlled by BEx#.

Please refer to the section on SRAM requirements for more information about SRAM timing.

Figure 4-11 L2 Cache Structure Block Diagram

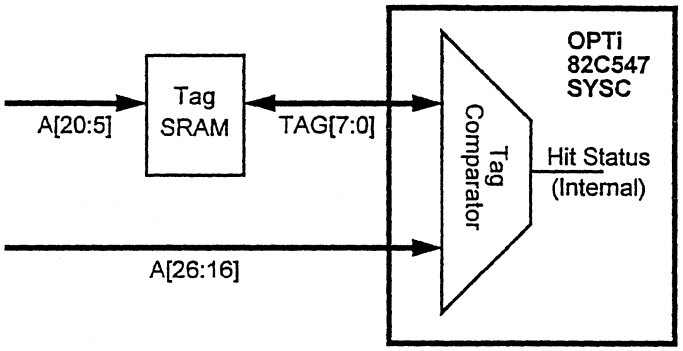


Table 4-4 Tag Compare

Tag Data	L2 Cache Size					
	64KB	128KB	256KB	512KB	1MB	2MB
TAG0	A16	A24	A24	A24	A24	A24
TAG1	A17	A17	A25	A25	A25	A25
TAG2	A18	A18	A18	A26	A26	A26
TAG3	A19	A19	A19	A19	X	X
TAG4	A20	A20	A20	A20	A20	X
TAG5	A21	A21	A21	A21	A21	A21
TAG6	A22	A22	A22	A22	A22	A22
TAG7	A23	A23	A23	A23	A23	A23
DIRTY	Dirty	Dirty	Dirty	Dirty	Dirty	Dirty

4.3.3.7 Single Bank Cache Verses Double Bank Cache

The 82C547 SYSC supports one or two 64-bit cache banks. Two cache banks are required to interleave and utilize the performance advantages of this cache scheme. Cache sizes of 128KB, 512KB, and 2MB are double bank caches, while 64KB, 256KB, and 1MB are single bank cache. When using a double bank configuration, the even and odd banks receive the same address lines.

In order to support cache burst cycles at elevated frequencies and still utilize conventional speed SRAMs, a bank interleave cache access method is employed. To do a burst read at a 3-2-2-2 rate, a new double word of data must be provided on every alternate clock. At 60MHz this is every 33ns.

- Address access requirement of the SRAM = (tAASRAM) = (2 CLK) - (tA3 delay from 82C547 + tPentium processor data setup)

Since the A3 delay and the CPU data setup time will take more than 15ns, less than 18ns is left, which requires higher speed SRAMs. To avoid this, two banks of SRAMs are interleaved on a double-word basis. The addresses are applied to the cache memory one cycle early and the SRAM output enable signal is used to select if the even or odd bank data will be enabled to the CPU data bus. Since the output enable time is about one-half that of the address access time, the 82C547 SYSC can achieve a high performance cache burst mode without using higher speed SRAMs. This also reduces the requirements on the address access time, allowing 15ns data SRAM parts to be used.

4.3.3.8 Cache Initialization

On power-up, the tag RAM will contain random data and the L2 cache will contain no valid bits. This means that the power-up default is that the cache must be initialized before it is enabled. The advantage of this validation scheme is that no valid bits are necessary for power-up and expensive SRAM can be conserved.

Initialization Procedure 1: The cache is initialized by configuring the cache controller to the write-through mode. This will cause all the cache read-miss cycles to fill the cache with valid data. This can done by reading a block of system memory that is greater than or equal to the size of the cache. Once the cache is initialized, it is always valid. After this is done, the write-back cache can then be initialized. This is done by first enabling the cache controller to the write-back mode. Then, by reading a block of system memory that is greater than or equal to twice the size of the cache, the "dirty" bits will be cleared and the L2 cache will be valid.

Initialization Procedure 2: This procedure uses the cache controller in Test Mode 1 and Test Mode 2 as defined in Index Register 02h and Index Register 07h.

The upper bits of an address is written to Index Register 07h. The cache controller is now set to Test Mode 2. Writing a block equal to the size of the cache to the system memory will write the contents of Index Register 07h to the tag. The cache controller is now configured in the write-through mode and reading a block of system memory equal to the size of the cache will make the data in the cache valid. Next, by reading a block of system memory which is greater than or equal to twice the size of the cache, the "dirty" bits will be cleared and the L2 cache will be valid.

Disabling the Cache: Disabling of a write-back cache cannot be done by just turning off the cache enable bit in the 82C547 chipset register. This is because there may still be valid data in the cache that has not been written to the system memory. Disabling write-back cache without flushing the valid data can result in unpredictable behavior or a system crash.

This can be avoided by first reading a cacheable memory block twice the size of the cache. "Twice the size" of the cache is required to make sure every location gets a read-miss, which will cause a castout cycle if the cache line is "dirty". The cache can then be disabled. Note that no writes should occur during this process.

4.3.3.9 Write-Back Cache with DMA/ISA Master/VL Master Operations

The L1 and the L2 cache contain the only valid copy (MODIFIED) of the data. The 82C547 SYSC will execute an inquire cycle to the L1 cache for all master accesses to the system memory area. This will increase the bus master cycle time for every access to the system memory which will also decrease the bus master performance. The Python Chipset provides the option of a snoop-line comparator to increase the performance of a bus master with the L1 cache.

The L1 cache inquire cycle begins with the CPU relinquishing the bus with the assertion of HLDA. On sampling HLDA active, the 82C547 SYSC will assert AHOLD and BOFF#. The address will flow from the master to the CPU bus and the 82C547 SYSC will assert EADS# for one CPU clock. If the CPU does not respond with the assertion of HITM#, the 82C547 SYSC will complete the cycle from the L2 cache or the system memory. If HITM# was asserted, the 82C547 SYSC will expect a castout cycle from the L1 cache and in response BOFF# is negated till the end of the castout cycle.

DMA/Master Read Cycle:
Table 4-5 shows the action taken by the 82C547 SYSC based on the L1 and L2 cache status for the bus master read from the system memory area. The L1 cache castout cycle will be completed in the burst order provided by the CPU and will be written to the L2 cache or the system memory based on the L2 cache status. The required bytes are then read back for the master read cycle completion. A read-hit in the L1 cache will always invalidate the L1 cache line.

Table 4-5 DMA/Master Read Cycle Summary

DMA/Master Read Cycle		Data Source	Type of Cycle for L1 Cache	Type of Cycle for L2 Cache	Type of Cycle for DRAM
L1 Cache	L2 Cache				
Hit	Hit	L2 Cache	Invalidate	Read the Bytes Requested	No Change
HITM#	Hit	L1 Cache	Castout, Invalidate	Write CPU Data, Read Back the Bytes Requested	No Change
Hit	Miss	DRAM	Invalidate	No Change	Read the Bytes Requested
HITM#	Miss	L1 Cache	Castout, Invalidate	No Change	Write CPU Data, Read Back the Bytes Requested
Miss	Hit	L2 Cache	No Change	Read the Bytes Requested	No Change
Miss	Miss	DRAM	No Change	No Change	Read

HITM# = L1 Cache Modified

Figure 4-12 AT DMA/Master Read (L1 Cache Line Clean)

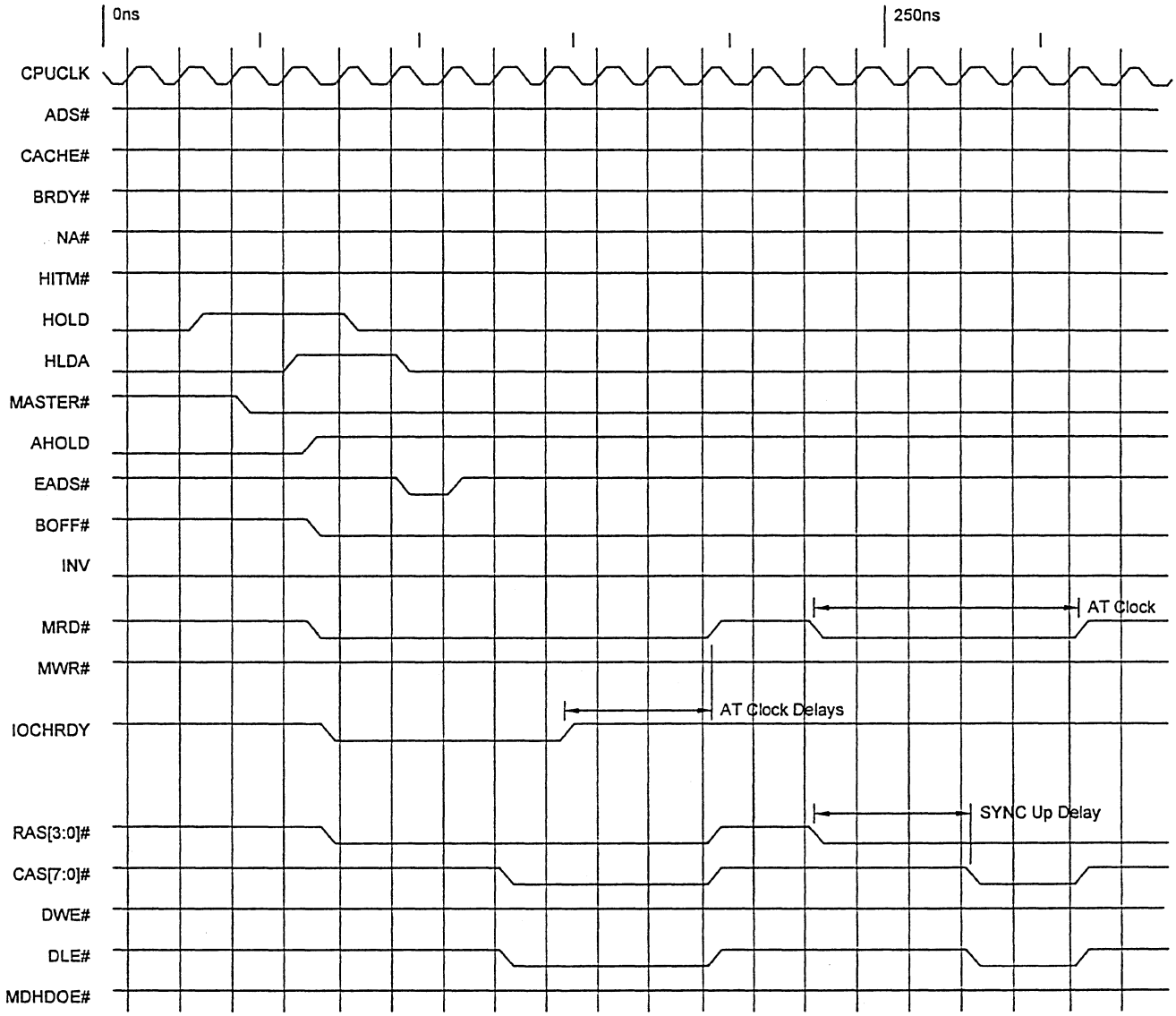
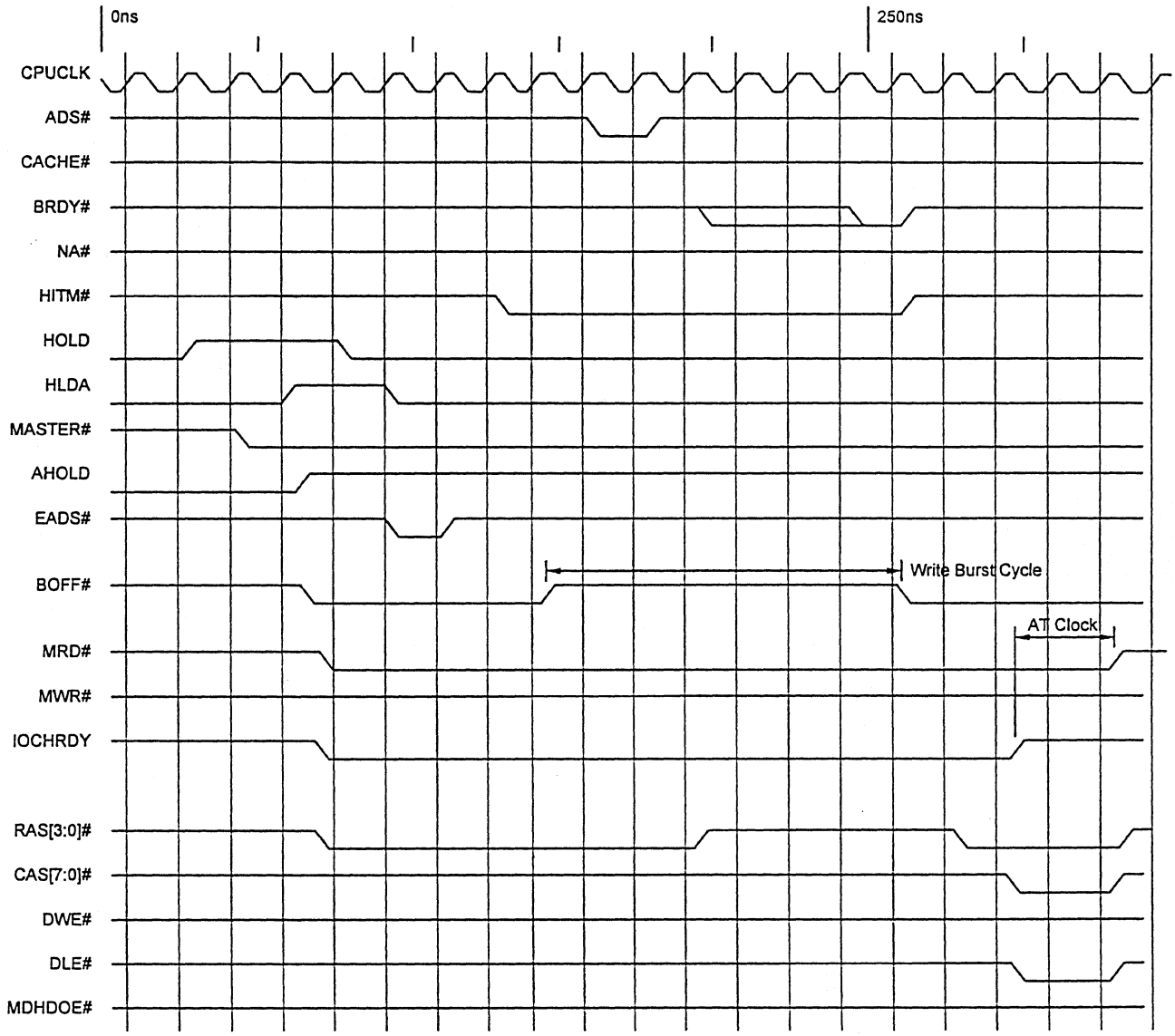


Figure 4-13 AT DMA/Master Read (L1 Cache Line Modified)



4.3.3.10 DMA/Master Write Cycle

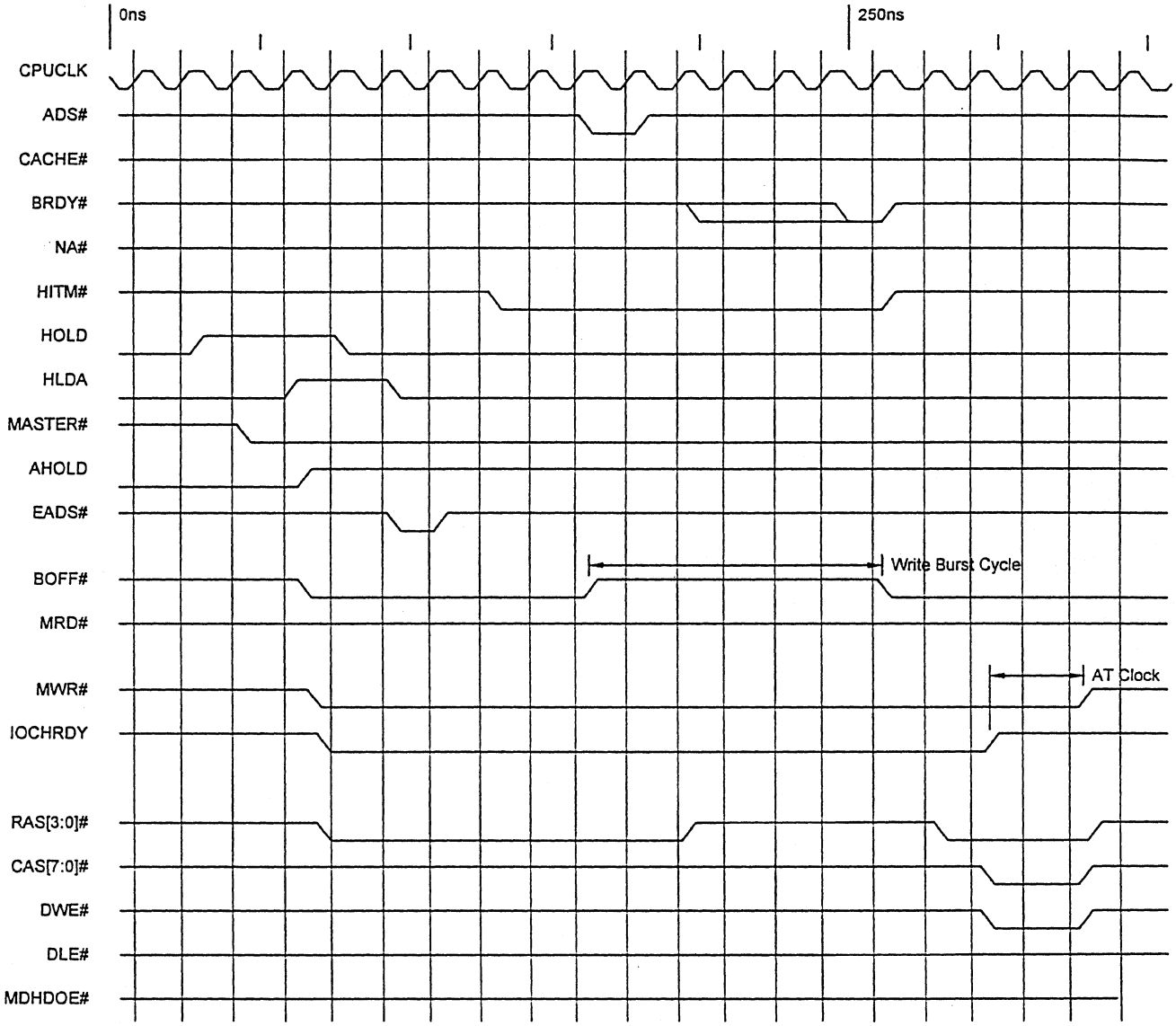
Table 4-6 shows the action taken by the 82C547 based on the L1 and L2 cache status for a bus master write to the system memory area. A master write to the L2 cache will always be in the write-through mode. The L1 cache castout cycle will be completed in the CPU burst sequence and the data will be written to the L2 cache or to the system memory based on the L2 cache status. Data from the master is always written to the L2 cache (if L2 cache hit) and to the system memory.

Table 4-6 DMA/Master Write Cycle Summary

DMA/Master Write Cycle		Data Destination	Type of Cycle for L1 Cache	Type of Cycle for L2 Cache	Type of Cycle for DRAM
L1 Cache	L2 Cache				
Hit	Hit	DRAM, L2	Invalidate	Write Master Data	Write Master Data
HITM#	Hit	DRAM, L2	Castout, Invalidate	Write CPU Data, Write Master Data	Write Master Data
Hit	Miss	DRAM	Invalidate	No Change	Write Master Data
HITM#	Miss	DRAM	Castout, Invalidate	No Change	Write CPU Data, Write Master Data
Miss	Hit	DRAM, L2	No Change	Write Master Data	Write Master Data
Miss	Miss	DRAM	No Change	No Change	Write Master Data

HITM# = L1 Cache Modified

Figure 4-14 AT DMA Master Write (L1 Cache Line Modified)



4.3.3.11 Cacheability and Write Protection

Both system DRAM and shadow RAM are cacheable in both the primary (L1) and/or secondary (L2) cache. Of these two areas, only the shadow RAM areas (system BIOS, video BIOS and DRAM) have the capability of being write-protected. (Non-shadowed BIOS ROM areas are implicitly write-protected.) Since the possibility exists that write-protected shadow RAM can be cached, there also exists the possibility that this data might be modified inside the cache and subsequently executed. To prevent this from occurring, an explicit control mechanism must be used that prevents the unexpected from happening. There are three methods for controlling write protection in the Python Chipset. Table 4-7 summarizes these methods.

Method 1: In this method, the write protected areas are not cached in the L1 or the L2 cache. This is implemented by driving KEN# high for the first word with BRDY#, which will cause the CPU to not cache the data and not do burst cycles. Data in the L2 cache is also not updated, so all reads and writes to this area will go directly to or from the system memory. Refer to Register Index 06h for further information.

Method 2: In this method, the write protected areas can be cached in the L2 cache but not in the L1 cache. This is implemented by driving KEN# high for the first word with BRDY#, which will cause the CPU to not cache the data in the L1 cache or do a burst cycle. This data can then be stored in the L2 cache, but only subsequent read requests by the CPU are serviced (discarding all writes), thus effectively write-protecting the data in the L2 cache. Read-miss cycles are serviced by first performing a linefill burst from the DRAM into the L2 cache and then performing a normal non-cacheable (and non-burst) cycle to the CPU. In this method, writes to the system memory and to the L2 cache are write protected.

Method 3: This method is implemented by driving EADS#/WT# high during the read cycle. Data read from write protected areas are stored in both the L1 and L2 caches. Accesses from the CPU that are L2 cache read-hits are serviced in the burst mode. L2 cache read-miss cycles are serviced by first performing a linefill burst read to the L2 cache from the write protected area and then performing a normal burst cycle to the CPU. Write cycles from the CPU to these areas are write-through and are discarded by the 82C547 SYSC's cache controller. However, L1 cache writes occur internally to the CPU in this mode and are therefore not write-protected. Refer to Register Index 08h for further information.

Table 4-7 Write Protection Control Methods

	System DRAM		System BIOS		Video BIOS		Write Enabled Shadow RAM		Write Protected Shadow RAM	
Method	Read	Write	Read	Write	Read	Write	Read	Write	Read	Write
1	L1, L2	L1, L2	Single	None	Single	None	L1, L2	L1, L2	Single	None
2	L1, L2	L1, L2	L2	None	L2	None	L1, L2	L1, L2	L2	None
3	L1, L2	L1, L2	L1, L2	l1	L1, L2	L1	L1, L2	L1, L2	L1, L2	L1

Notes: L1 = accessible to Primary cache
L2 = accessible to Secondary cache
None = no cycle performed (or discard)
Int = internal cycle to CPU
WT = Write-through cycle
Single = single word (non-burst) cycle
Burst = burst cycle

4.3.3.12 SRAM Requirements

The 82C547 SYSC's cache controller uses standard off-the-shelf 3.3V SRAMs for both tag and data. The tag SRAMs may be configured as a 5.0V device through the VCC3A pin. Table 4-8 summarizes the data SRAM configurations. Table 4-9 summarizes the data and tag SRAM speed requirements.

The SRAMs are quad-word interleaved for the two bank configuration, which requires 64-bit wide SRAM. This allows systems based on the Python Chipset to perform a full 3-2-2-2 burst for reads and 4-2-2-2 burst for writes. If a single bank of SRAM is to be used, the cache controller will increase the burst wait state.

Table 4-8 Data SRAM Configurations

	Data SRAMs		Tag SRAMs				
Cache Size	Qty	Type	Qty	Tag Address Field	Qty	Tag Dirty Bit Field	Cacheable Range
64KB	8	8Kx8	1	8Kx8	1	16Kx1	16MB
128KB	16	8Kx8	1	8Kx8	1	16Kx1	32MB
256KB	8	32Kx8	1	8Kx8	1	16Kx1	64MB
512KB	16	32Kx8	2	8Kx8	1	16Kx1	128MB
1MB	8	128Kx8	1	32Kx8	1	64Kx1	128MB
2MB	16	128Kx8	1	128Kx8	1	64Kx1	128MB

Table 4-9 Data and Tag SRAM Speed Requirements

Parameter	Description	33MHz (ns)	50MHz (ns)	60MHz (ns)
Data SRAMs				
tAA	Address Access Time	35	20	15
tOE	OE# Access Time	20	12	8
tWP	Write Pulse Width	30	25	14.5
Tag SRAMs				
tAA	Address Access Time	35	20	15

4.4 DRAM Controller

The Python Chipset's DRAM controller uses a 64-bit wide DRAM data bus interface. It also uses a page mode technique for faster data access from the DRAMs.

Hidden refresh is used to increase the CPU bandwidth by not having to put the CPU on hold every 15μs to refresh the DRAM. The DRAM can be refreshed in the background while the CPU is accessing the internal cache.

Page mode is always used in the Python Chipset for CPU accesses, both for bursts and between bursts. Page mode is performed by keeping RAS active while reading or writing multiple words within a DRAM page by changing only the column address and toggling CAS with the new column address.

A posted-write to the DRAM improves the write cycle timing relative to the CPU and allows the chipset to perform an independent write burst cycle to DRAM without holding the CPU. The Python Chipset maintains a one quad-word deep data buffer for DRAM writes so that the CPU write cycle is completed without waiting for the external DRAM cycle. The lead-off cycle time is reduced to four clocks even if the cycle is a non-page-hit cycle. For a page-hit cycle, the burst write can be completed in 4-3-3-3 with posted-write enabled. The posted write buffer in the 82C546 ATC is controlled by the DLE# signal from the 82C547 SYSC. Effectively, the rising edge of DLE# will latch new data from the CPU bus to the posted write buffer.

The timing constraints to achieve optimum performance at 60MHz are met without making the system design overly critical. Timing variations that are required for different system speeds are handled by a selection of timing modes that vary the wait states used. Table 4-10 summarizes these timing modes.

The fastest possible burst read is 8-3-3-3 which means the first quad-word is received in eight clocks and the next three quad-words are received after three clocks each. For a cache-based system, it would mean the bursting to the cache and CPU for read-miss cycles or write-miss cycle. Table 4-11 and Table 4-12 summarizes the DRAM Timing Modes for read and write cycles, respectively.

Table 4-10 DRAM Programmable Control

Controlled DRAM Timing	Variation in CLK
RAS Address Hold Time	1 to 2
CAS Pulse Width for Reads	2 to 3
Case Pulse Width for Writes	2 to 3
Address setup time to CAS for Write Page-hit	1 to 2
CAS Precharge Time	1 to 2
RAS Precharge Time	3 to 6
RAS Pulse Width for Refresh	3 to 6

Table 4-11 DRAM Timing Mode - Read Cycle

CPU Speeds (MHz)	Can be Used without Cache?	Page-hit	Page-miss RAS High	Page-miss RAS Active	CPU Pipeline Reduces Leadoff Cycle by:	Burst Cycle	DRAM Speed (ns)
33 to 60	Yes	8 Cycles	11 Cycles	11+Precharge	5 Clocks	3-3-3	70

Table 4-12 DRAM Timing Mode - Write Cycle

CPU Speeds (MHz)	Can be Used without Cache?	Burst Page-hit	Page-miss Burst RAS High	Page-miss Burst RAS Active	CPU Pipeline Reduces Leadoff Cycle by:	DRAM Speed (ns)
33 to 60	Yes	4-3-3-3	4-7-3-3	4-(7+Precharge)-3-3	1 Clock	70

These modes were specifically designed for cache-based systems and for system speeds of 50MHz and up, but will also perform well in DRAM-only systems using the Pentium CPU.

The DRAM read cycle uses a CAS signal that is active for multiples of T-state boundaries rather than one-half T-state boundaries. This allows additional address decode setup time and MA bus setup time at the start of the cycle, making the fastest burst cycle 8-3-3-3.

4.4.1 DRAM Read Cycle

The DRAM read cycle begins with the DRAM controller detecting a page-hit or a page-miss cycle at the end of the second T2. Based on the status of the current open page and the active RASx#, a page-hit, a page-miss with RAS inactive, or a page-miss with RAS active cycle is executed.

Page-miss with RAS high cycle: The row address is generated from the CPU address bus. Table 4-14 gives the row/column address mux map. After RASx# goes active, the row address is changed on the next clock edge (programmable to be two CLKs) to the column address. The CASx# will be active two CLKs after the column address is generated.

Page-miss with RASx# low cycle: RAS is first precharged for the programmed number of CLKs and then driven active, after which it will be the same as a page-miss with RAS high cycle.

Page-hit cycle: The 82C547 SYSC generates the column address from the CPU address bus and the CASx# is driven active for two clocks. The data bus direction between the CPU bus and the DRAM bus is controlled in the 82C546 ATC's data buffers by the MDHDOE# signal from the 82C547 SYSC. The MDHDOE# signal can be selected to go inactive at either the beginning or end of the last T2. This is determined during the power-on reset (POR) sequence in the 82C547 SYSC. Table 4-13 gives the POR and MDHDOE# relationship. Data from the DRAM is latched by the 82C546 ATC at the end of each CAS. The latched data is valid on the CPU data bus until the next falling edge of CASx#. During this time, the next read is started, CASx# signals are precharged for one or two clocks (programmable), and the next data from the DRAM is accessed and latched. The 82C546 ATC latches the data from the DRAM and holds the data for the CPU while the DRAM controller begins the read for the next word in the burst cycle. The burst read from the DRAM is in effect pipelined into the CPU data bus by the Chipset. Refer to Figure 4-5. This scheme reduces the constraints on the board layout so that routing for the CPU data bus, MD data bus, and CASx# signal lines are less critical and performance can be maintained.

Table 4-13 POR and MDHDOE#

POR Status of XD0	Selection
High	MDHDOE# goes high at the end of the last T2
Low	MDHDOE# goes high at the beginning of the last T2

Page-hit cycle (extended): Wait states can be added if slower DRAMs are used. In this mode, data from the DRAM is latched by the 82C546 ATC at the end of each CAS cycle, similar to the default mode. The only difference between the two modes is that the CAS low time on reads is increased by one T-state. This eases up on the page mode cycle time and CAS access time parameters.

4.4.2 DRAM Write Cycle

Single level posted write cycles are employed to achieve a 4-3-3-3 burst at 60MHz. The data from the CPU is latched in the 82C546 ATC's write buffer until CAS goes active one T-state after the first T2 (on a page-hit). This provides a fast write mechanism and two wait state writes are maintained for the leadoff cycle within a page (even at 60MHz). The CAS pulse width can be extended by one more T-state to ease the timing constraints on the CAS pulse width requirement for speeds above 60MHz. Refer to Figure 4-6.

4.4.3 DRAM Parity Generation/Detection Logic

During local DRAM write cycles, the 82C546 ATC generates a parity bit for each byte of write data from the processor. Parity bits are stored into local DRAM along with each data byte. During a DRAM read, the parity bit is checked for each data byte. If the logic detects incorrect parity, the 82C547 SYSC will generate a parity error to the CPU. The parity error will invoke the NMI interrupt, provided that parity checking is enabled in configuration Index Register 08h, bit 4. Parity checking must also be enabled in the Port B Register (61h), bits 3 and 2.

4.4.4 DRAM Refresh Logic

The 82C547 SYSC supports both normal and hidden refresh. Normal refresh refers to the classical refresh implementation which places the CPU on "hold" while a refresh cycle takes place to both the local DRAM and any AT bus memory. This is the default condition at power-up. Hidden refresh is performed independently of the CPU and does not suffer from the performance restriction of losing processor bandwidth by forcing the CPU into its hold state. Hidden refresh delivers higher system performance and is recommended over normal refresh. As long as the CPU does not try to access local memory or the AT bus during a hidden refresh cycle, refresh will be transparent to the CPU. The CPU can continue to execute from its internal and secondary caches as well as execute internal instructions during hidden refresh without any loss in performance due to refresh arbitration. If a local memory or AT bus access is required during a hidden refresh cycle, wait states will be added to the CPU cycle until the resource becomes available. Hidden refresh also separates refreshing of the AT bus and local DRAM. The DRAM controller arbitrates between CPU DRAM accesses and DRAM refresh cycles, while the ATC arbitrates between CPU accesses to the AT bus, DMA, and AT refresh. The 82C546 ATC asserts the RFSH# and MRD# commands and outputs the refresh address during AT bus refresh cycles.

The 82C547 SYSC implements refresh cycles to the local DRAM using CAS-before-RAS timing. The CAS-before-RAS refresh uses less power than a RAS-only refresh which is important when dealing with large memory arrays. CAS-before-RAS refresh is used for both normal and hidden refresh to DRAM memory.

The output of internal Counter1/Timer1 (OUT1) inside the 82C206 IPC is programmed as a rate generator to produce the periodic refresh request signal which occurs every 15μs. Requests for refresh cycles are generated by two sources: Counter1/Timer1 or 16-bit ISA masters that activate refresh when they have bus ownership. These ISA masters must supply refresh cycles because the refresh controller cannot preempt the bus master to perform the necessary refresh cycles. 16-bit ISA masters that hold the bus longer than 15μs must supply refresh cycles.

4.4.5 DRAM Address Muxing

Table 4-14 shows the DRAM address (MA) muxing. Note that the column address is the same for all configurations since this is the speed path. A3 and A4 must go through an internal burst counter, for the generation of the MA address to the DRAMs. The table shows MA the line to address bit mapping for each DRAM size configuration.

Table 4-14 DRAM Row/Column MA to Address Bit Map

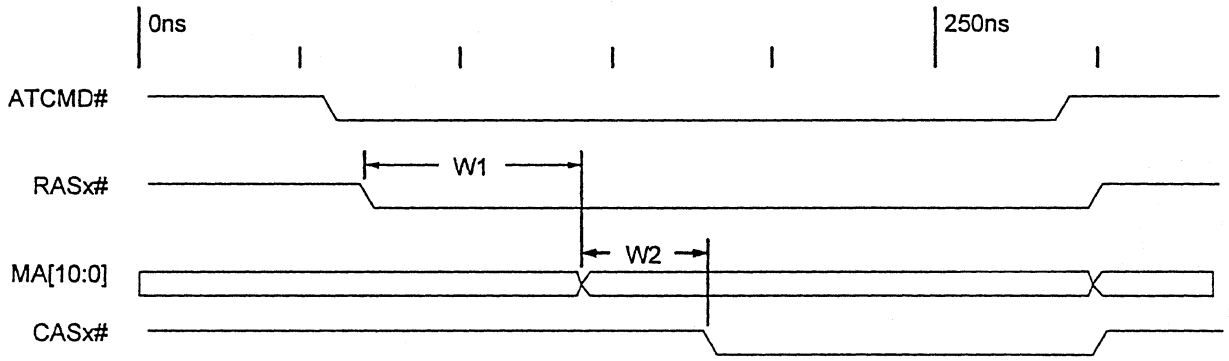
Memory Address	256KB		1MB		4MB	
	Column	Row	Column	Row	Column	Row
MA0	A3	A12	A3	A12	A3	A12
MA1	A4	A13	A4	A13	A4	A13
MA2	A5	A14	A5	A14	A5	A14
MA3	A6	A15	A6	A15	A6	A15
MA4	A7	A16	A7	A16	A7	A16
MA5	A8	A17	A8	A17	A8	A17
MA6	A9	A18	A9	A18	A9	A18
MA7	A10	A19	A10	A19	A10	A19
MA8	A11	A20	A11	A20	A11	A20
MA9			A22	A21	A22	A21
MA10					A24	A23

4.4.6 DRAM DMA/Master Cycles

For DMA and master cycles, the DRAM controller operates such that the MRD# and MWR# signals generate RASx# synchronously. The generation of the DRAM column address is then synchronized with LCLK. The synchronization can be programmed to be 0.5 to 1.5 LCLKs and 1 to 2 LCLKs. The generation of CASx# is always one LCLK after the generation of the column address. The cycles can thus be completed without adding wait states. For cases when the CPU write-back cache is enabled, wait states need to be added to the DMA/master cycles. Please refer to Figure 4-15. This is because the CPU can request a primary cache castout (always a burst write to the DRAMs) and only after the castout is completed can the requested data from the DRAM be fetched.

Note: ISA masters which ignore CHRDY may not work when the CPU's write-back is enabled.

Figure 4-15 AT Master Synchronization



ATCMD# - MEMRD# or MEMWR#
W1 - 0.5 to 1.5 and 1 to 2 LCLKs
W2 - 1 LCLK

4.5 AT Bus Interface

The AT bus state machine gains control when the 82C546 ATC's decoding logic detects a non-local memory cycle. It monitors status signals M16#, IO16#, CHRDY, and 0WS# and performs the necessary synchronization of control and status signals between the AT bus and the microprocessor. The chipset supports 8- and 16-bit memory and I/O devices located on the AT bus.

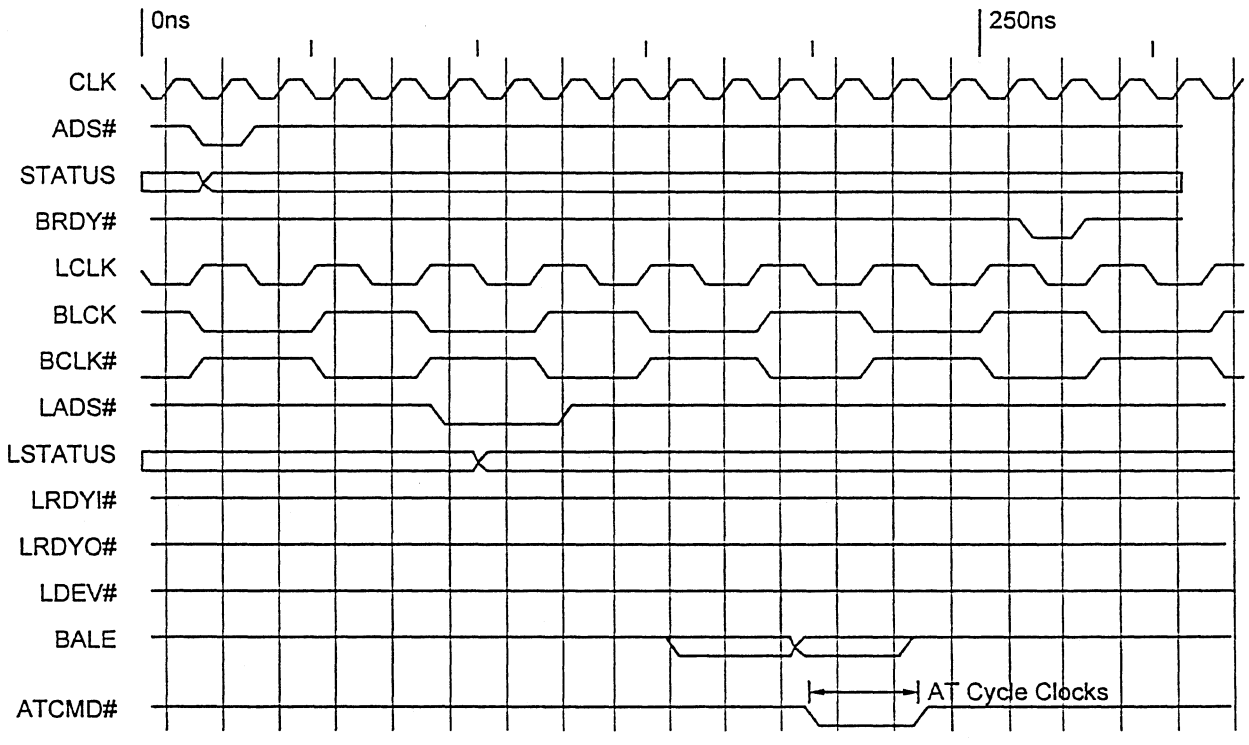
An AT bus cycle is initiated by asserting ALE in AT-TS1-state. On the trailing edge of ALE, M16# is sampled for a memory cycle to determine the bus size. It then enters the AT TC-state and provides the command signal. For an I/O cycle, IO16# is sampled after the trailing edge of ALE until the end of the command. Typically, the wait state for an AT 8/16-bit transaction is 4/1, respectively. The command cycle is extended when CHRDY is detected inactive or the cycle is terminated when the zero wait state request signal (0WS#) from the AT bus is active. Upon expiration of the wait states, the AT state machine terminates itself and passes an internal READY to the CPU state machine to output a synchronous BRDY# to the CPU. The AT bus state machine also routes data and address when an AT bus master or DMA controller accesses system memory. Refer to Figure 4-16.

The AT bus can be configured for slow or fast back-to-back I/O cycles. This is determined during the POR sequence in the 82C546 ATC. Table 4-15 gives the power-on reset and back-to-back I/O cycle relationship.

Table 4-15 POR and AT Back-to-Back I/O Cycles

POR Signal Strapping of MP2	Selection
High	Slow: Three AT Clocks inserted in Back-to-Back I/O Cycles
Low	Fast: Zero AT Clocks inserted in Back-to-Back I/O Cycles

Figure 4-16 CPU Access to the AT Bus



4.6 Bus Arbitration Logic

The 82C547 SYSC provides arbitration between the CPU, DMA controller, AT bus masters, VL bus masters, and the refresh logic. During DMA, AT bus master cycles, VL bus master cycles, and conventional refresh cycles, the 82C547 SYSC asserts HOLD to the CPU. The CPU will respond to an active HOLD signal by generating HLDA (after completing its current bus cycle) and placing most of its output and I/O pins in a high impedance state. After the CPU relinquishes the bus, the 82C547 SYSC responds by issuing RFSH# (refresh cycle) or HLDA1 (AT bus master or DMA cycle), depending on the requesting device. During hidden refresh, HOLD remains negated and the CPU continues its current program execution as long as it services internal requests or achieves cache hits (refer to the section about refresh for additional information).

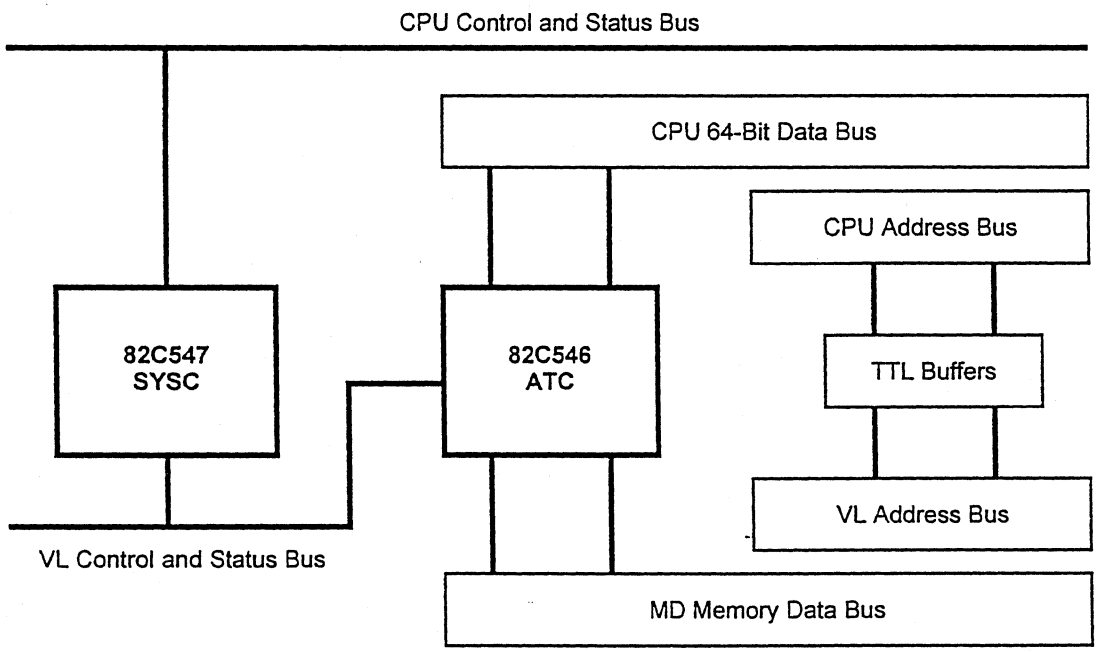
Normally, refresh cycles, DMA cycles, and master cycles are serviced on a first-in/first-out priority, but DRAM refresh requests (RFSH#) are internally latched and serviced immediately after the current DMA or master finishes its request, if the refresh request was queued behind an AT DMA or master (HRQ) request from the 82C206 IPC. The 82C547 SYSC will now request the CPU bus by asserting HOLD to the CPU. The CPU will complete the ongoing cycle and when it gives up the CPU bus, it will assert HLDA to the 82C547 SYSC. The 82C547 SYSC will grant the CPU bus to the AT DMA or master and assert HLDA1. The HRQ signal must remain active to be serviced if a refresh request comes first. DMA and bus masters share the same request pin; HRQ. To distinguish between DMA and bus master requests during an active HLDA1 period, the two signals AEN8# and AEN16# can be used to distinguish between DMA and master cycles. If AEN8# or AEN16# are active, then the cycle is an 8- or 16-bit DMA, respectively. When these signals are inactive, then an external bus master controls the system bus.

The arbitration between a refresh request and VL master is such that the VL master can be preempted by a refresh request. It can also be programmed with a first-in/first-out priority if the VL master does not support preempt.

4.7 VL Bus Interface

The VL bus is interfaced to the system as a logically and physically separate bus from the CPU bus. Refer to Figure 4-17. The VL bus is separated from the CPU bus and runs asynchronous to the CPU bus. All of the control and status signals are generated by the 82C547 SYSC and the data path is controlled by buffers in the 82C546 ATC. The 82C546 ATC also does the data bus conversion to interface the 32-bit VL bus to the 64-bit CPU bus. The Python Chipset supports VL bus speeds up to 50MHz, independent of the CPU speed. One VL master can be supported without any external glue logic.

Figure 4-17 CPU to VL Bus Interface Block Diagram



4.7.1 VL Bus Slave

The chipset assumes that an access outside the system memory area is either a VL slave cycle or an AT cycle. The 82C547 generates LADS# and VL bus status signals for all such accesses on the VL bus T1-state. The VL slave can claim such an access by asserting LDEV# at the first VL bus T2-state. For slower slave devices, the chipset can be made to sample LDEV# on the second VL bus T2-state instead of the first T2-state by a power-up strapping option. Refer to Table 4-16.

If LDEV# is active when sampled, the chipset will not execute an AT cycle, but will instead wait for the VL slave to generate LRDY#. Refer to Figure 4-18. After LRDY# is sampled active, the chipset will terminate the cycle of the current active bus master by returning BRDY#, LRDY# or CHRDY.

Table 4-16 VL Bus POR Signal Strapping

POR Signal Strapping		LDEV# Sample Point
MP4	MP3	
Low	X	LDEV# not sampled
High		LDEV# sampled at the end of the second T2
High	High	LDEV# sampled at the end of the first T2

Figure 4-18 CPU Read from VESA Slave

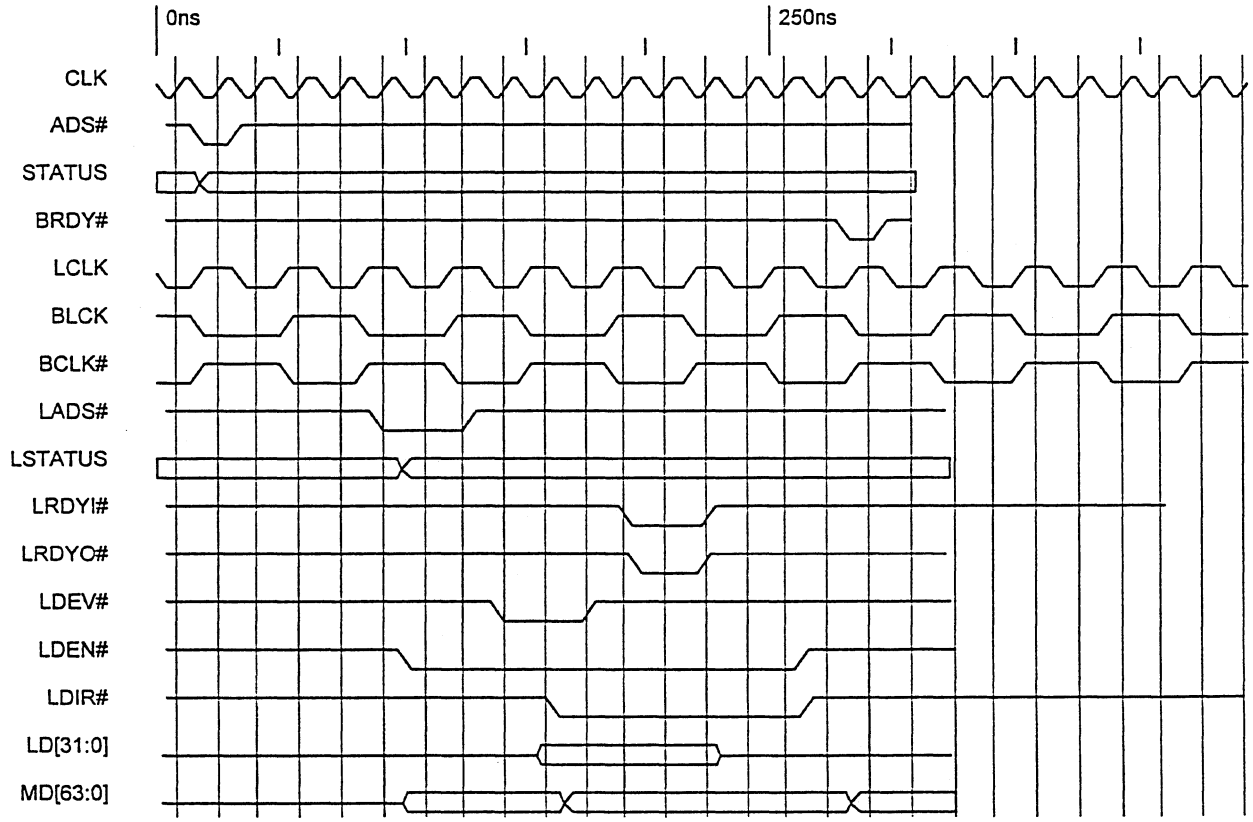
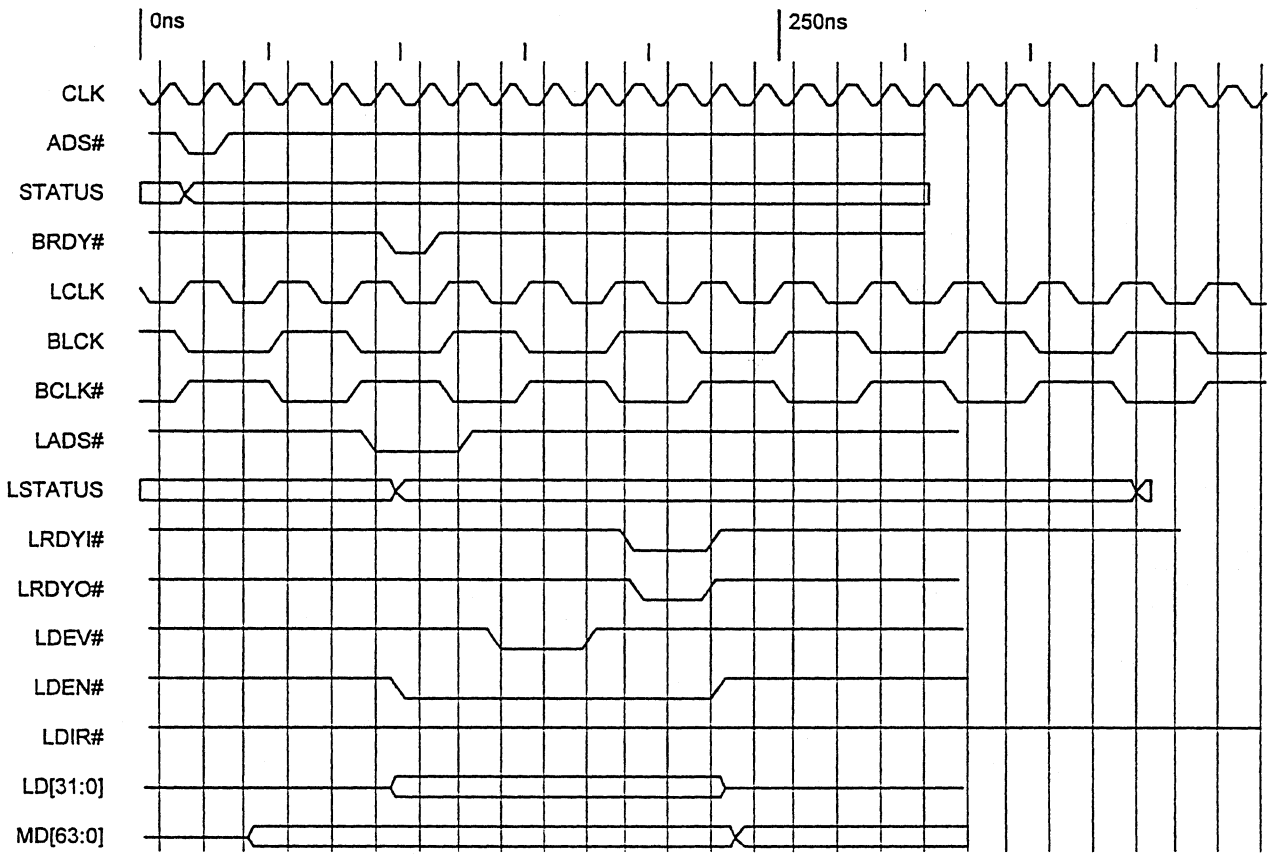


Figure 4-19 CPU Write to VESA Slave



4.7.2 VL Bus Master

The VL bus master requests the system bus by asserting LREQ#. The 82C547 SYSC's arbitration logic will return LGNT# active after the current master relinquishes the bus. The VL master will then begin a read or a write cycle by asserting LADS# and VL status signals. At the completion of the data transfer to the system memory area, VL slave or AT bus, the 82C547 SYSC will return LRDY# to the active VL master.

The Python Chipset has a programmable option to support VL bus master preempting. If a higher priority bus request (like a system refresh request) can preempt the VL master, the Python Chipset will deassert LGNT# and the VL master is expected to deassert LREQ# for at least two LCLKs after the completion of the ongoing transaction. This will allow a higher priority request access even though the system is servicing the VL master.

4.8 Data Bus Conversion/Data Path Control Logic

Data bus conversion of a 64-bit bus to a 32-bit VL or a 8/16-bit AT bus is done by the 82C546 ATC. The 82C547 SYSC converts the CPU byte enables, BE[7:0]#, to address A2 and four byte enable signals, LBE[3:0]#, for the VL bus and the 82C546 ATC. The 82C546 ATC uses the LBE[3:0]#, A2, and the other AT address information (A1, A0, SBHE#, and IO16#/M16#) to complete the 64-bit to 8/16-bit data conversion for the AT bus. The 82C546 ATC performs data bus conversion when the CPU accesses 16- or 8-bit devices through 16- or 32-bit instructions. It also handles DMA and AT master cycles that transfer data between local DRAM or cache memory and locations on the AT bus. The 82C547 SYSC provides all of the signals to control external bidirectional data buffers.

4.9 Deturbo/Slow Mode Operations

The Deturbo Mode is controlled through Configuration Register 0Fh, bit 1. If this bit is disabled (0), the SLOW# pin input will be ignored and the system will always run at full speed. If this bit is enabled, the system will operate at full speed if the SLOW# pin is asserted high and in Deturbo (slow) Mode when the SLOW# input is pulled low.

Slow mode operation is implemented by extending the refresh duration for every system DRAM refresh request (every 15µs). This will extend the CPU hold time and thus, slow down the system. If Configuration Register 0Fh, bit 1 is enabled for Deturbo Mode, the duration of the CPU hold can be controlled by the binary value in Configuration Register 0Fh, bits 2 and 3 (slowest = bits 2 and 3 = high). OSC12 is the clock source used for this operation. OSC12 is internally derived from the 14.31818MHz OSCI clock input to the 82C547 SYSC. This counter on the CPU hold duration provides a method for system speed throttle that is transparent to the rest of the system. For system designs without Deturbo, the SLOW# pin should be pulled high through a 10 Kohm resistor.

4.10 Fast GATEA20 and RESET Emulation

The 82C547 SYSC will intercept commands to Ports 60h and 64h so that it can emulate the keyboard controller, allowing the generation of the fast GATEA20 and fast INIT signals. The decode sequence is software transparent and requires no BIOS modifications to function. The fast GATEA20 generation sequence involves writing "D1h" to Port 64h, then writing data "02h" to Port 60h. The fast CPU "warm reset" function is generated when a Port 64h write cycle with data "FEh" is decoded. A write to Port 64h with data "D0h" will enable the status of GATEA20 (bit 1 of Port 60h) and the warm reset (bit 0 of Port 60h) to be readable.

4.11 Special Cycles

4.11.1 Shadow RAM

Since accesses to local DRAM are much faster than those to EPROM, the 82C547 SYSC provides shadow RAM capability. With this feature, code from slow devices like ROM and EPROM memories can be copied to local DRAM to speed up memory accesses. Accesses to the specified EPROM space are redirected to the corresponding DRAM location. Shadow RAM addresses range from C0000h-FFFFFh in 16KB granularity is provided for the address range C0000h-EFFFFh, while the 64KB range from F0000h-FFFFFh (the location of system BIOS) can be shadowed as an entire segment.

The shadow RAM control is setup in the configuration registers. First, the ROM contents must be copied into the shadow RAM area. Next, the shadow RAM enable bit is set in the configuration register. For the system BIOS area, once the bit is set, the RAM area becomes read-only. For the video and adapter BIOS area, the user can select read-only or read/write by setting the write-protect bit in the appropriate index register.

Video and system BIOS at the C0000h-C8000h and F0000h-FFFFFh area can be shadowed and cached in the L1 and L2 caches. System BIOS at F0000h-FFFFFh can also be shadowed, but can only be cached in the L2 cache.

4.11.2 System ROM BIOS Cycles

The 82C547 SYSC supports both 8- and 16-bit EPROM cycles. If the system BIOS is 16 bits wide, ROMCS# should be connected to M16# through an open collector gate, indicating to the 82C547 that a 16-bit EPROM is responding. The system BIOS resides on the XD bus. The XD to SD data buffer is normally enabled (SDEN# active) except during I/O read cycles at addresses below 100h (byte-wide I/O), INTA cycles, and 8-bit ROM BIOS cycles.

ROMCS# is generated for both the E0000h-EFFFFh and F0000h-FFFFFh segments. If a combined video/system ROM BIOS is desired, these two segments should be used.

4.11.3 System Shutdown/Halt Cycles

The Pentium CPU provides special bus cycles to indicate that certain instructions have been executed or certain conditions have occurred internally. These special cycles, such as shutdown and halt, are covered by dedicated handling logic inside the 82C547. The Python Chipset will generate INIT for a CPU shutdown cycle.

5.0 Configuration Registers

There are a total of 15 indexed configuration registers between the 82C546 ATC and 82C547 SYSC. An indexing scheme is used to access all of these registers. Port 22h is used as the Index Register and Port 24h is the Data Register. Each access to a configuration register consists of a write to Port 22h, specifying the desired register in the data byte, followed by a read or write to Port 24h with the actual register data. The Index resets after every access; so every data access (via Port 24h) must be preceded by a write to Port 22h even if the same register is being accessed consecutively.

All reserved bits are set to zero by default and must be set to zero for future purposes.

5.1 Keyboard I/O Control Registers: Ports 60h and 64h

The 82C546 ATC and 82C547 SYSC will intercept commands to Ports 60h and 64h so that it may emulate the keyboard controller, allowing the generation of the fast GATEA20 and fast CPURST signals. The decode sequence is software transparent and requires no BIOS modifications to function. The fast GATEA20 generation sequence involves writing "D1h" to Port 64h, then writing data "02h" to Port 60h. The fast CPU warm reset function is generated when a Port 64h write cycle with data "FEh" is decoded. A write to Port 64h with data "D0h" will enable the status of GATEA20 (bit 1 of Port 60h) and the system reset (bit 0 of Port 60h) to be readable.

Table 5-1 Port B Register: Index 61h

Bit(s)	Type	Default	Function
7	RO		System Parity Check
6	RO		I/O Channel Check
5	RO		Timer OUT2 Detect
4	RO		Refresh Detect
3	R/W		I/O Channel Check Enable: 0 = Enable 1 = Disable
2	R/W		Parity Check Enable: 0 = Enable 1 = Disable
1	R/W		Speaker Output Enable: 0 = Disable 1 = Enable
0	R/W		Timer 2 Gate: 0 = Disable 1 = Enable

Table 5-2 DRAM Configuration Register 1: Index 00h

Bit(s)	Type	Default	Function
7	R/W	0	Reserved
6	R/W	0	0 = Single-sided SIMM Module not installed in Bank 1 1 = Single-sided SIMM Module installed in Bank 1
5	R/W	0	0 = Single-sided SIMM Module not installed in Bank 0 1 = Single-sided SIMM Module installed in Bank 0
4:0	R/W	00000	SIMM 0 through 3 DRAM Configuration:

Bits [4:0]	SIMM0	SIMM1	SIMM2	SIMM3	Total
00000	256KB	256KB			2MB
00001	512KB	512KB			4MB
00010	1MB	1MB			8MB
00011	2MB	2MB			16MB
00100	4MB	4MB			32MB
00101	8MB	8MB			64MB
00110	256KB	256KB	256KB	256KB	4MB
00111	256KB	256KB	512KB	512KB	6MB
01000	512KB	512KB	512KB	512KB	8MB
01001	256KB	256KB	1MB	1MB	10MB
01010	512KB	512KB	1MB	1MB	12MB
01011	1MB	1MB	1MB	1MB	16MB
01100	256KB	256KB	2MB	2MB	18MB
01101	512KB	512KB	2MB	2MB	20MB
01110	1MB	1MB	2MB	2MB	24MB
01111	2MB	2MB	2MB	2MB	32MB
10000	256KB	256KB	4MB	4MB	34MB
10001	512KB	512KB	4MB	4MB	36MB
10010	1MB	1MB	4MB	4MB	40MB
10011	2MB	2MB	4MB	4MB	48MB
10100	4MB	4MB	4MB	4MB	64MB
10101	256KB	256KB	8MB	8MB	66MB
10110	512KB	512KB	8MB	8MB	68MB
10111	1MB	1MB	8MB	8MB	72MB
11000	2MB	2MB	8MB	8MB	80MB
11001	4MB	4MB	8MB	8MB	96MB
11010	8MB	8MB	8MB	8MB	128MB

Table 5-3 DRAM Control Register 1: Index 01h

Bit(s)	Type	Default	Function
7	R/W	0	Row Address Hold after RAS in CLKS: 0 = 2 CLKs 1 = 1 CLK
6	R/W	0	Address Decode Delay for Write Page-hit: 0 = Enable 1 = Disable
5:4	R/W	00	RAS Pulse Width used for Refresh in CLKs: **5 4 CLKs** 0 0 7 0 1 6 1 0 5 1 1 4
3	R/W	0	Read CAS Pulse Width in CLKs: 0 = 3 CLKs 1 = 2 CLKs
2	R/W	0	Write CAS Pulse Width in CLKs: 0 = 3 CLKs 1 = 2 CLKs
1:0	R/W	00	RAS Precharge in CLKs: **1 0 CLKs** 0 0 6 0 1 5 1 0 4 1 1 3

Table 5-4 Cache Control Register 1: Index 02h

Bit(s)	Type	Default	Function
7:6	R/W	00	Cache Size Selection: **If Index Register 0Fh bit 0 = 0** **If Index Register 0Fh bit 0 = 1** **7 6 Size** **7 6 Size** 0 0 64KB 0 0 1MB 0 1 128KB 0 1 2MB 1 0 256KB 1 1 512KB
5:4	R/W	00	Cache Write Policy: **5 4 Policy** 0 0 L2 Cache Write-through 0 1 Reserved 1 0 Reserved 1 1 L2 Cache Write-back
3:2	R/W	00	Cache Mode Select: **3 2 Mode** 0 0 Disable 0 1 Test Mode 1 (Tag Data Write-through Index Register 07h) 1 0 Test Mode 2 (Tag Data Read from Index Register 07h) 1 1 Enable L2 Cache
1	R/W	0	DRAM Post Write Enable: 0 = Disable 1 = Enable
0	R/W	0	CAS Precharge in CLKs: 0 = 2 CLKs 1 = 1 CLK

Table 5-5 Cache Control Register 2: Index 03h

Bit(s)	Type	Default	Function
7:6	R/W	00	Cache Write Burst Mode CLKs: **If Index Register 0Fh bit 0 = 0** **7 6 Size** 0 0 X-4-4-4 0 1 X-3-3-3 1 0 X-2-2-2 1 1 Reserved
5:4	R/W	00	Cache Write Leadoff Cycle Cache CLKs: **5 4 Non-Pipelined Pipelined** 0 0 5-X-X-X 4-X-X-X 0 1 4-X-X-X 3-X-X-X 1 0 3-X-X-X 3-X-X-X 1 1 4-X-X-X 4-X-X-X
3:2	R/W	00	Cache Read Burst Mode CLKs: **3 2 Mode** 0 0 X-4-4-4 0 1 X-3-3-3 1 0 X-2-2-2 1 1 Reserved
1:0	R/W	00	Cache Read Leadoff Cycle Cache CLKs: **5 4 Non-Pipelined Pipelined** 0 0 5-X-X-X 4-X-X-X 0 1 4-X-X-X 3-X-X-X 1 0 3-X-X-X 3-X-X-X 1 1 Reserved

Table 5-6 Shadow RAM Control Register 1: Index 04h

Bit(s)	Type	Default	Function
7:6	R/W	00	CC000h-CFFFFh Read/Write Control: **7 6 Function** 0 0 Read/Write AT Bus 1 0 Read from AT - Write to DRAM 1 1 Read from DRAM - Write to DRAM 0 1 Read from DRAM (write-protected)
5:4	R/W	00	C8000h-CBFFFh Read/Write Control: **5 4 Function** 0 0 Read/Write AT Bus 1 0 Read from AT - Write to DRAM 1 1 Read from DRAM - Write to DRAM 0 1 Read from DRAM (write-protected)
3:2	R/W	00	C4000h-C3FFFh Read/Write Control: **3 2 Function** 0 0 Read/Write AT Bus 1 0 Read from AT - Write to DRAM 1 1 Read from DRAM - Write to DRAM 0 1 Read from DRAM (write-protected)
1:0	R/W	00	C0000h-C3FFFh Read/Write Control: **1 0 Function** 0 0 Read/Write AT Bus 1 0 Read from AT - Write to DRAM 1 1 Read from DRAM - Write to DRAM 0 1 Read from DRAM (write-protected)

Table 5-7 Shadow RAM Control Register 2: Index 05h

Bit(s)	Type	Default	Function
7:6	R/W	00	DC000h-DFFFFh Read/Write Control: **7 6 Function** 0 0 Read/Write AT Bus 1 0 Read from AT - Write to DRAM 1 1 Read from DRAM - Write to DRAM 0 1 Read from DRAM (write-protected)
5:4	R/W	00	D8000h-DBFFFh Read/Write Control: **5 4 Function** 0 0 Read/Write AT Bus 1 0 Read from AT - Write to DRAM 1 1 Read from DRAM - Write to DRAM 0 1 Read from DRAM (write-protected)
3:2	R/W	00	D4000h-D3FFFh Read/Write Control: **3 2 Function** 0 0 Read/Write AT Bus 1 0 Read from AT - Write to DRAM 1 1 Read from DRAM - Write to DRAM 0 1 Read from DRAM (write-protected)
1:0	R/W	00	D0000h-D3FFFh Read/Write Control: **1 0 Function** 0 0 Read/Write AT Bus 1 0 Read from AT - Write to DRAM 1 1 Read from DRAM - Write to DRAM 0 1 Read from DRAM (write-protected)

Table 5-8 Shadow RAM Control Register 3: Index 06h

Bit(s)	Type	Default	Function
7	R/W	0	DRAM Hole in System Memory from 80000h-9FFFFh: 0 = No Hole in Memory 1 = Enable Hole in Memory
6	R/W	0	Wait State for VL Master: 0 = Add 1 Wait Statel 1 = No Wait State **Note:** No wait state is recommended for LCK speeds 33MHz and below.
5	R/W	0	Range C0000h-C7FFFh Cacheable: 0 = Not Cacheable 1 = Cacheable
4	R/W	0	Range F0000h-FFFFFh Cacheable: 0 = Not Cacheable 1 = Cacheable
3:2	R/W	00	F0000h-FFFFFh Read/Write Control: **3 2 Function** 0 0 Read/Write AT Bus 1 0 Read from AT - Write to DRAM 1 1 Read from DRAM - Write to DRAM 0 1 Read from DRAM (write-protected)
1:0	R/W	00	E0000h-EFFFFh Read/Write Control: **3 2 Function** 0 0 Read/Write AT Bus 1 0 Read from AT - Write to DRAM 1 1 Read from DRAM - Write to DRAM 0 1 Read from DRAM (write-protected)

Table 5-9 Tag Test Register: Index 07h

Bit(s)	Type	Default	Function
7:0	R/W	00h	Tag Test Register: If in Test Mode 1, data from this register is written to the tag. If in Test Mode 2 data from the tag is read into this register. Refer to Index Register 02h.

Table 5-10 CPU Cache Control Register 1: Index 08h

Bit(s)	Type	Default	Function
7	R/W	0	L2 Cache Single Bank Select: 0 = Double Bank (interleaved) 1 = Single Bank (non-interleaved)
6	R/W	0	Line Comparator for Bus Masters: For a master request if the subsequent read/write is within the same cache line, CPU "Inquire" cycles are not done until there is a cache line miss. 0 = Disable 1 = Enable
5	R/W	0	CPU HITM# Pin Sample Timing: 0 = Delay One Clock 1 = No Delay
4	R/W	0	Parity Check: 0 = Disabled 1 = Enabled
3	R/W	0	Hidden Refresh: 0 = Disabled 1 = Enabled
2	R/W	0	CPU Address Pipelining: 0 = Disabled 1 = Enabled
1	R/W	0	L1 Cache Write-back: 0 = Write-through Only 1 = Write-back Enabled
0	R/W	0	BIOS (F0000h-FFFFFh) Area Cacheability in L1 Cache: 0 = Not Cached in L1 Cache 1 = Cacheable in L1 Cache

Table 5-11 System Memory Function Register 1: Index 09h

Bit(s)	Type	Default	Function
7:6	R/W	00	DRAM Hole B Size: **7 6 Size** 0 0 512KB 0 1 1MB 1 0 2MB 1 1 4MB
5:4	R/W	00	DRAM Hole B Control Mode: **5 4 Mode** 0 0 Disable 0 1 Write-through for L1 and L2 Cache 1 0 Non-cacheable for L1 and L2 Cache 1 1 Enable Hole in DRAM
3:2	R/W	00	DRAM Hole A Size: **3 2 Size** 0 0 512KB 0 1 1MB 1 0 2MB 1 1 4MB
1:0	R/W	00	DRAM Hole B Control Mode: **1 0 Mode** 0 0 Disable 0 1 Write-through for L1 and L2 Cache 1 0 Non-cacheable for L1 and L2 Cache 1 1 Enable Hole in DRAM

Table 5-12 System Memory Address Decode Register 1: Index 0Ah

Bit(s)	Type	Default	Function
7:0	R/W	00h	System Memory Function "A" Starting Address A[26:19].

Table 5-13 System Memory Address Decode Register 2: Index 0Bh

Bit(s)	Type	Default	Function
7:0	R/W	00h	System Memory Function "B" Starting Address A[26:19].

Table 5-14 Extended DMA Register: Index 0Ch

Bit(s)	Type	Default	Function
7:6	R/W	00	82C547 SYSC Version Number: Read for revision number. Always write 00.
5:4	R/W	00	Reserved
3	R/W	0	Extended DMA Page Register Enable: 0 = Disabled 1 = Enabled
2:0	R/W	000	Extended DMA Page Address: Bit 2 = A26 Bit 1 = A25 Bit 0 = A24

Table 5-15 ROMCS# Register: Index 0Dh

Bit(s)	Type	Default	Function
7	R/W	0	ROMCS# for C8000h-CFFFFh: 0 = Disable 1 = Enable
6	R/W	0	ROMCS# for C0000h-C7FFFh: 0 = Disable 1 = Enable
5	R/W	0	ROMCS# for D8000h-DFFFFh: 0 = Disable 1 = Enable
4	R/W	0	ROMCS# for D0000h-D7FFFh: 0 = Disable 1 = Enable
3	R/W	0	ROMCS# for E8000h-EFFFFh: 0 = Disable 1 = Enable
2	R/W	0	ROMCS# for E0000h-E7FFFh: 0 = Disable 1 = Enable
1	R/W	0	ROMCS# for F8000h-FFFFFh: 1 = Disable 0 = Enable
0	R/W	0	ROMCS# for F0000h-F7FFFh: 1 = Disable 0 = Enable

Table 5-16 Local Master Preemption Register: Index 0Eh

Bit(s)	Type	Default	Function
7:1	R/W	0000 000	Reserved: Set to 0.
0	R/W	0	82C206 Request Delay: 0 = Normal 82C206 request timing 1 = Delay 82C206 request by two AT clocks to overcome AT clock hold time during DMA cycles

Table 5-17 Deturbo Control Register 1: Index 0Fh

Bit(s)	Type	Default	Function
7	R/W	0	Set LGNT# Synchronous to LCK: Setting LGNT# to be synchronous to LCK will result in reduced performance. This may be required for some local bus master cards which do not have synchronous LGNT# on the card. 0 = LGNT# is not synchronous to LCLK 1 = LGNT# is synchronous to LCLK
6	R/W	0	Additional AT Master Sync Time: 0 = Slow 1 = Fast Note: Slow is recommended for LCLK speeds 33MHz and above.
5	R/W	0	Access above 16MB to AT Bus: 1 = Disable 0 = Enable
4	R/W	0	Enable Parity Test Mode 0: This bit must always be set to 0. Setting this bit to 1 floats the memory parity bus of the 82C546. Always write 0. 0 = Disable 1 = Enable
3:2	R/W	00	Deturbo Value: If the Deturbo enable bits is set, the system speed throttle is controlled by these bits. For Deturbo Mode, the internal cache and hidden refresh should be disabled. 00 = 8: 1.19MHz Clock Delay (Minimum) 01 = 10: 1.19MHz Clock Delay 10 = 12: 1.19MHz Clock Delay 11 = 16: 1.19MHz Clock Delay (Maximum)
1	R/W	0	Deturbo Counter Enable Control: 1 = Enable Deturbo Counter and SLOW# 0 = Disable Deturbo Counter and SLOW#
0	R/W	0	Cache Size Selection: 0 = Below 1MB 1 = Above 1MB

Table 5-18 Cache Write-hit Control Register: Index 10h

Bit(s)	Type	Default	Function
7:2	R/W	000 000	Reserved: Set to 0.
1	R/W	0	74AHCT126 Present Select: 0 = 74AHCT126 installed (for CPU clock over 50MHz) 1 = No 74AHCT126 installed (for CPU clock 50MHz or less)
0	R/W	0	Reserved: Set to 0.

Table 5-19 Master Cycle Control Register: Index 11h

Bit(s)	Type	Default	Function
7:0	R/W	0000 0000	Reserved: Set to 0.

Table 5-20 PS/2 Reset Control: Port 92h

Bit(s)	Type	Default	Function
7:2	R/W	000000	Reserved
1	R/W	0	A20M# Register: 0 = A20M# Active 1 =A20M# Inactive
0	R/W	0	Fast Reset (automatically clears back to 0): 1 = INIT sent to the Pentium processor

6.0 Maximum Ratings

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1 Absolute Maximum Ratings

Symbol	Parameter	5.0 Volt		3.3 Volt		Unit
		Min	Max	Min	Max	
VCC	Supply Voltage		+6.5		TBD	V
VI	Input Voltage	-0.5	+5.5	-0.5	TBD	V
VO	Output Voltage	-0.5	+5.5	-0.5	TBD	V
TOP	Operating Temperature	-25	+70	-25	+70	°C
TSTG	Storage Temperature	-40	+125	-40	+125	°C

6.2 DC Characteristics: 5.0 Volt (VCC = 5.0V ±5%, TA = -25°C to +70°C)

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input Low Voltage	-0.5	+0.8	V	
VIH	Input High Voltage	+2.0	+5.5	V	
VOL	Output Low Voltage		+0.4	V	IOL = 4.0mA
VOH	Output High Voltage	+2.4		V	IOH = -1.6mA
IIL	Input Leakage Current		+10.0	µA	VIN = VCC
IOZ	Tristate Leakage Current		+10.0	µA	
CIN	Input Capacitance		+10.0	pF	
COUT	Output Capacitance		+10.0	pF	
ICC	Power Supply Current		TBD	mA	

6.3 DC Characteristics: 3.3 Volt (VCC = 3.3V ±5%, TA = -25°C to +70°C)

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input Low Voltage	-0.5	+0.8	V	
VIH	Input High Voltage	+2.0	TBD	V	
VOL	Output Low Voltage		+0.4	V	IOL = 4.0mA
VOH	Output High Voltage	+2.4		V	IOH = -1.6mA
IIL	Input Leakage Current		+10.0	µA	VIN = VCC
IOZ	Tristate Leakage Current		+10.0	µA	
CIN	Input Capacitance		+10.0	pF	
COUT	Output Capacitance		+10.0 -	pF	
ICC	Power Supply Current		TBD	mA	

6.4 82C546 AC Characteristics (60MHz - Preliminary)

Symbol	Parameter	Min	Max	Unit	Condition
t204	BCLK to BALE Active/Inactive	3	15	ns	
t205	BCLK to MRD#, MWE# Delay	3	15	ns	
t206	BCLK to IORD#, IOWR# Delay	3	15	ns	
t208	CHRDY Setup to BCLK		10	ns	
t208	LBE[3:0]# to XA[1:0] Delay from LCLK		25	ns	

Symbol	Parameter	Min	Max	Unit	Condition
t209	LBE[3:0]# to SBHE# Delay from LCLK		25	ns	
t210	M16#, IO16# Setup to BCLK	5	25	ns	
t211	M16#, IO16# Hold from BCLK	5		ns	
t212	0WS# Setup to BCLK Low	20		ns	
t213	0WS# Hold from BCLK High	5		ns	
t225	CHCK# Setup	5		ns	

Symbol	Parameter	Min	Max	Unit	Condition
t400	MD[63:0] Valid Delay Max	2	10	ns	
t401	D[63:0] Valid Delay Max	2	10	ns	
t402	DLE# Low to MD[63:0] Bus Valid	5	15	ns	
t403	DLE# Low to MP[7:0] New Parity Valid		15	ns	
t404	HDMDOE# Low to MP[7:0] Valid		13	ns	
t410	D[63:0] Data Setup to DLE# High	5		ns	
t411	D[63:0] Data Hold after DLE# High	3		ns	
t412	MD[63:0] Data Setup to DLE# High	5		ns	
t413	MD[63:0] Data Hold after DLE# High	6		ns	
t414	MP[7:0] Data Hold after DLE# High	6		ns	
t420	HDMDOE# High to D[63:0] High-Z		15	ns	
t421	HDMDOE# High to MD[63:0] High-Z		15	ns	

Symbol	Parameter	Min	Max	Unit	Condition
t450	LDEN# Delay from LCLK	4	13	ns	
t451	LDIR# Delay from LCLK	4	13	ns	

Notes: BCLK = AT Bus Buffered Clock
BALE = Buffered ALE

6.5 82C547 AC Characteristics (60MHz - Preliminary)

Symbol	Parameter	Min	Max	Unit	Condition
t10	ECA4, OCA4 Delay from CLK	3	12	ns	
t11	82C547 ECA4, OCA4 Propagation Delay		15	ns	
t12	CDOE# Cache OE Delay from CLK High	3	12	ns	
t13	CAWE# Delay from CLK	3	12	ns	
t14	HACALE Delay from CLK	2	8	ns	
t15	BESL# Delay from CLK	3	10	ns	
t20	TAG[7:0] Data Read Setup to BRDY# Low	7		ns	
t22	DIRTY Data Read Setup to CLK	7		ns	
t23	TAGWE# Delay from CLK	3	10	ns	
t24	TAG[7:0] Data Delay from CLK	3	15	ns	
t50	82C547 CLK to RAS[3:0]# Delay	4	13	ns	70pF Load
t51	82C547 CLK to CAS[3:0]# Delay	3	10	ns	
t52	82C547 CLK to DWE# Delay	4	15	ns	
t53	82C547 CLK to MA[10:0] Delay	3	13	ns	
t54	82C547 A[26:3] to MA[10:0 Delay on Page-hit	3	17	ns	
t55	HDMDOE# Propagation Delay from CLK	4	13	ns	
t56	MDHDOE# Propagation Delay from CLK	4	13	ns	
t57	82C547 CLK to DLE# Delay	4	13	ns	

Symbol	Parameter	Min	Max	Unit	Condition
t100	CLK Delay from CPUCLK	2		ns	
t101	ECLK Setup to CPUCLK	2	5	ns	
t106	ADS# Setup to CLK	5		ns	
t107	ADS# Hold from CLK	2		ns	
t106a	M/IO#, D/C, W/R#, CACHE# Setup to CLK	5		ns	
t107a	M/IO#, D/C, W/R#, CACHE# Hold from CLK	2		ns	
t106b	82C547 A[26:3] Setup to CLK	5		ns	
t107b	82C547 A[26:3] Hold to CLK	2		ns	
t106c	DRAM# Setup to End of first T2	9		ns	
t107c	DRAM# Hold from CLK	2		ns	
t109	HLDA, HITM# Setup to CLK	5		ns	70pF Load
t110	HLDA, HITM# Hold from CLK	2		ns	
t114	A[26:3] Delay from CLK	3	7	ns	
t116	EADS#/WT# Delay from CLK	5	10	ns	
t118	KEN#/LMEM#, NA# Delay from CLK	5	10	ns	

82C547 AC Characteristics (60MHz - Preliminary) (Cont.)

Symbol	Parameter	Min	Max	Unit	Condition
t120	BRDY# Delay from CLK	5	12	ns	
t122	BOFF#, AHOLD Delay from CLK max	5	15	ns	
t124	HOLD Delay from CLK	3	15	ns	
t126	A20M#, INTA# Delay from CLK	3	12	ns	
t128	FLUSH#, INIT Delay from CLK	3	12	ns	
t136	RESET Delay from CLK	3	10	ns	

Symbol	Parameter	Min	Max	Unit	Condition
t226	ROMCS# Delay		25	ns	

Symbol	Parameter	Min	Max	Unit	Condition
t306	LADS# Setup to LCLK	5		ns	
t307	LADS# Hold from LCLK	3		ns	
t306a	LM/IO#, LD/C#, LW/R# Setup to LCLK	5		ns	
t307a	LM/IO#, LD/C#, LW/R# Hold to LCLK	3		ns	
t308	LRDY# Setup to LCLK	5		ns	
t309	LRDY# Hold from LCLK	3		ns	
t316	LADS# Delay from LCLK	3	11	ns	
t318	LM/IO#, LD/C#, LW/R# Delay from LCLK	4	13	ns	
t320	LRDY# Delay from LCLK	3	12	ns	
t321	LBE[3:0]# Delay from LCKK	4	13	ns	

Figure 6-1 Setup Timing Waveform

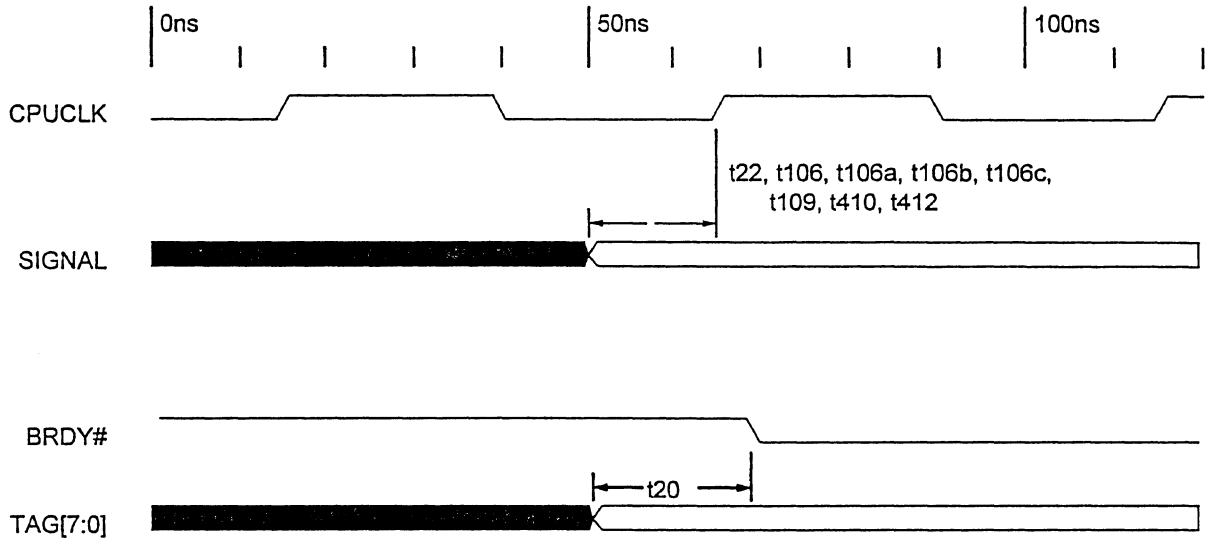


Figure 6-2 Hold Timing Waveform

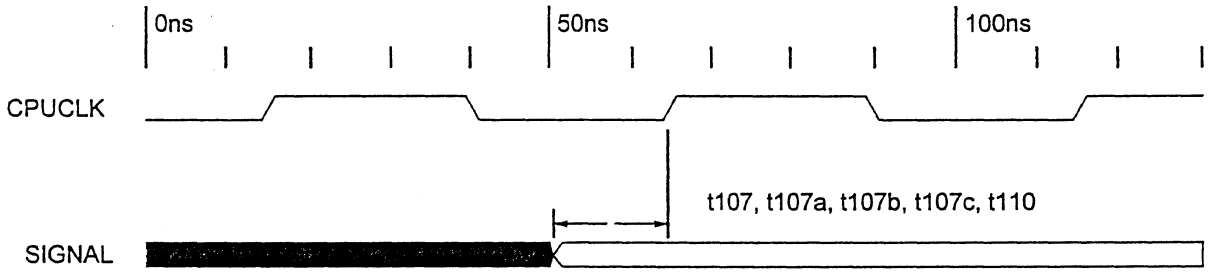


Figure 6-3 Output Delay Timing Waveform

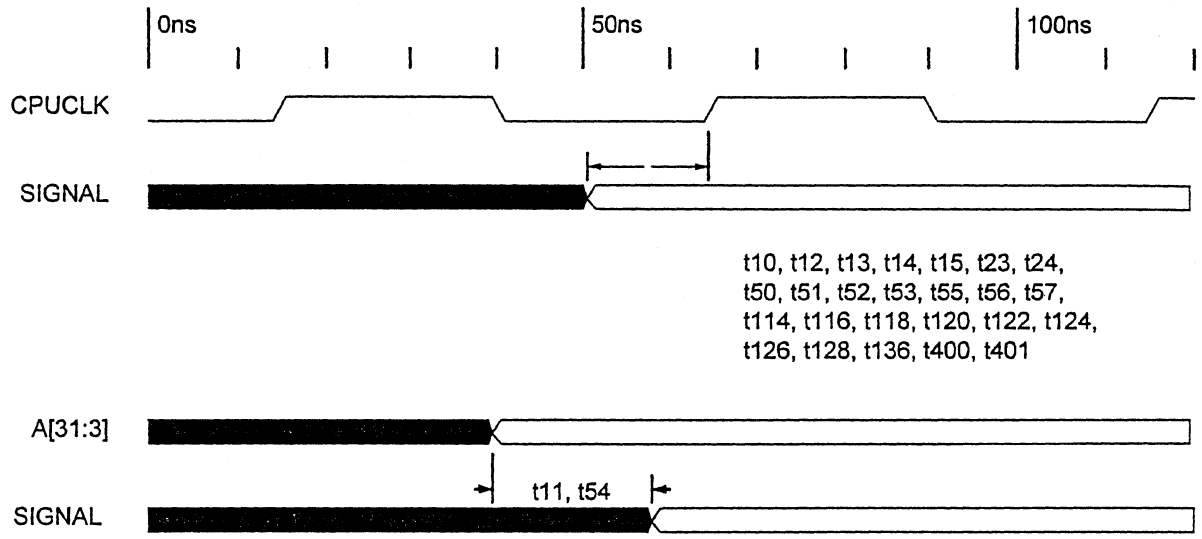
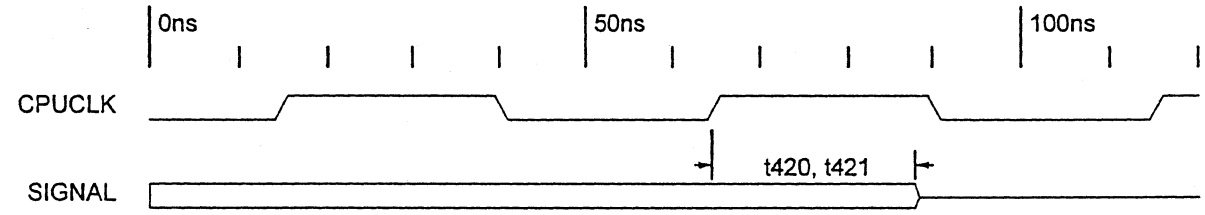
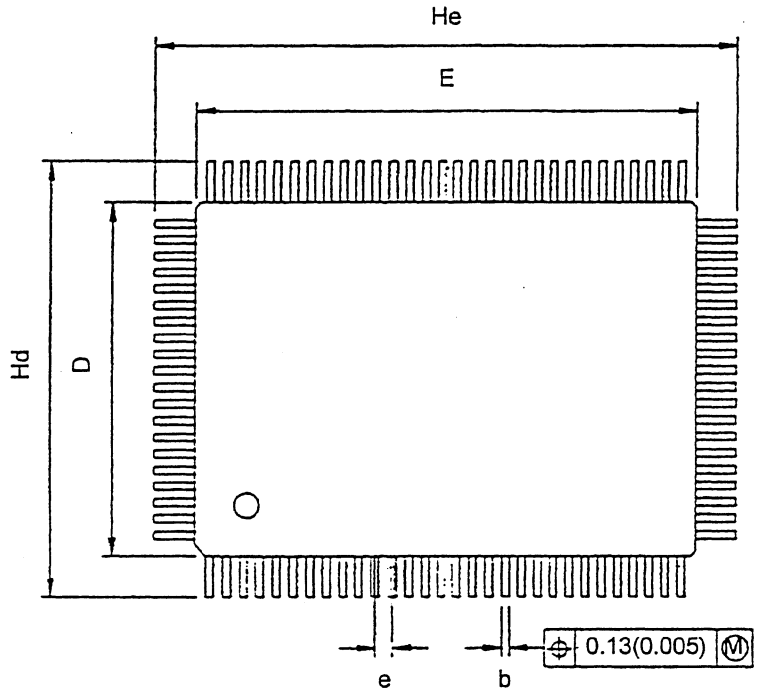


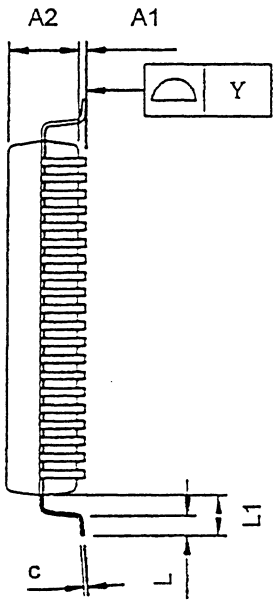
Figure 6-4 Float Delay Timing Waveform

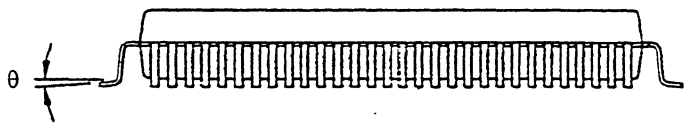


7.0 Mechanical Package Outlines

Figure 7-1 100-Pin Plastic Quad Flat Pack (PQFP)

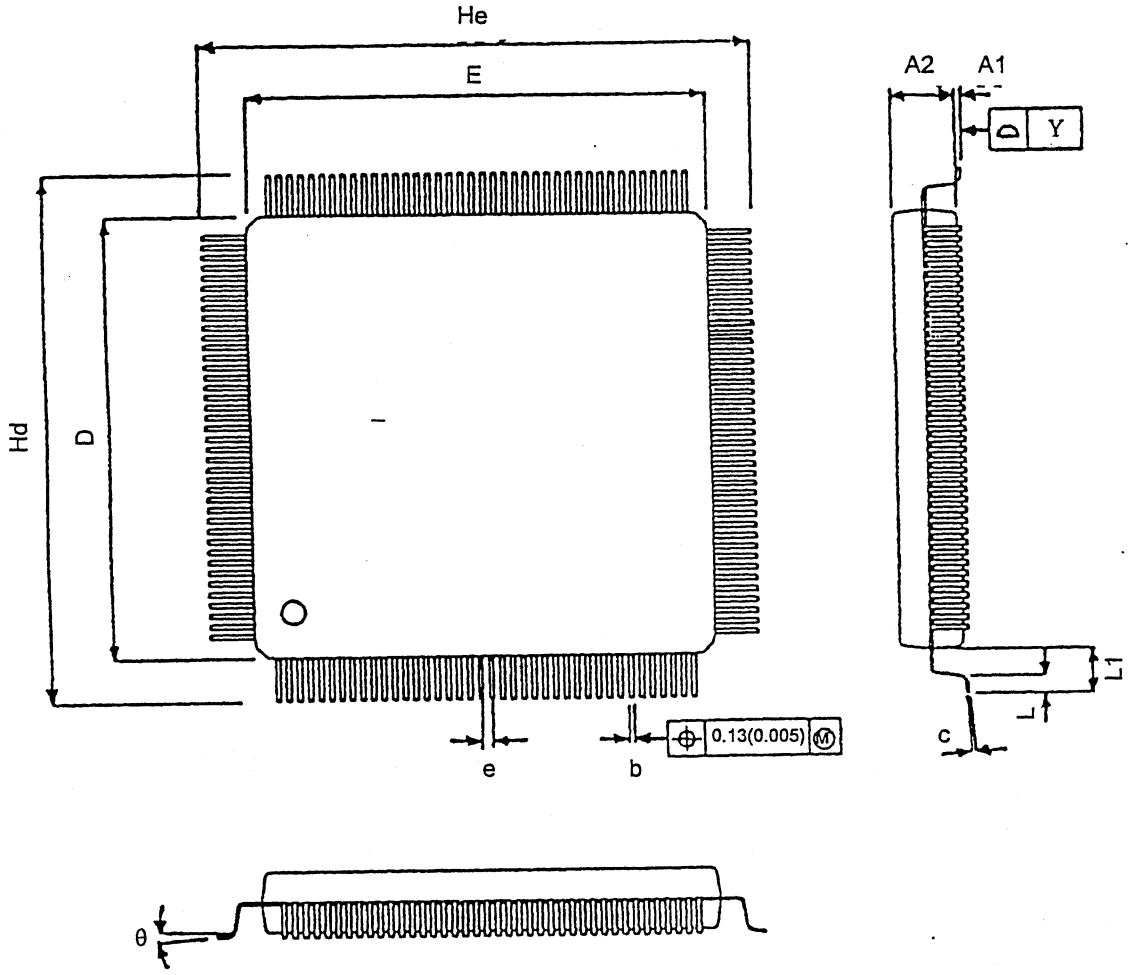






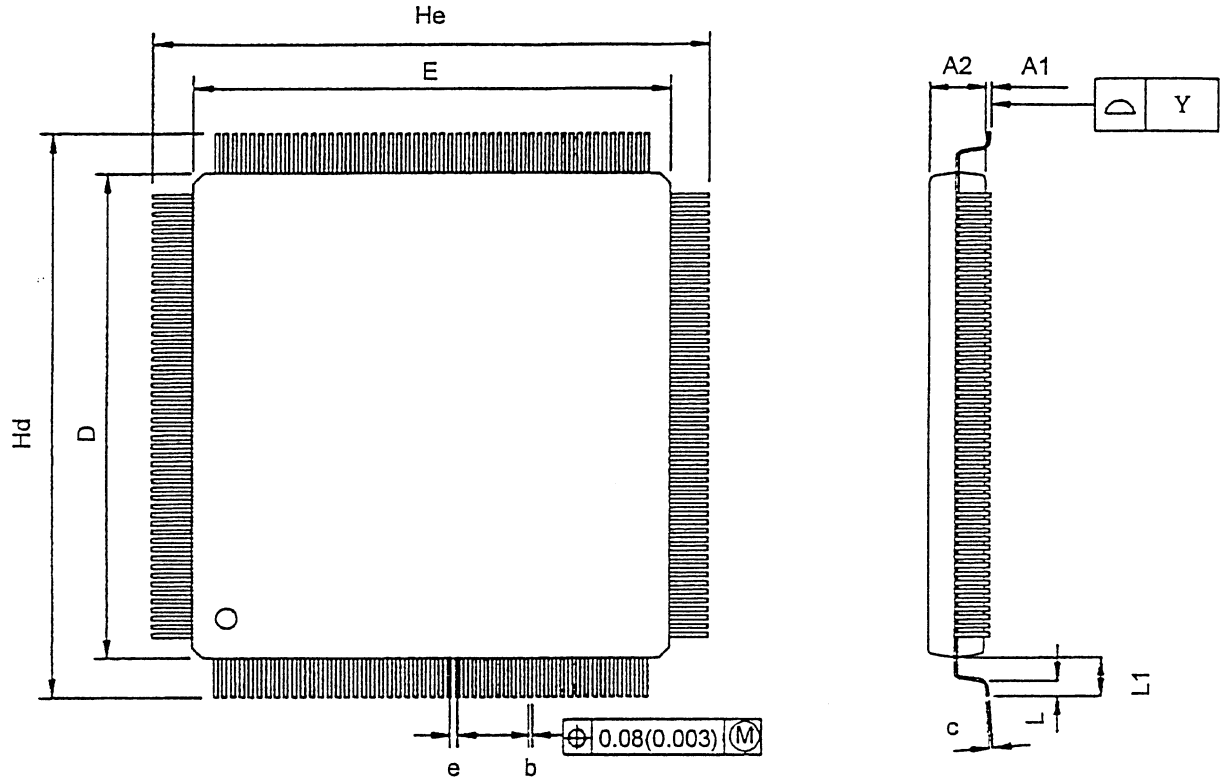
Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A1	0.25	0.35	0.45	0.010	0.014	0.018
A2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e		0.65			0.026	
Hd	17.00	17.20	17.40	0.669	0.677	0.685
He	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L1		1.60			0.063	
Y			0.08			0.003
θ °	0		10	0		10

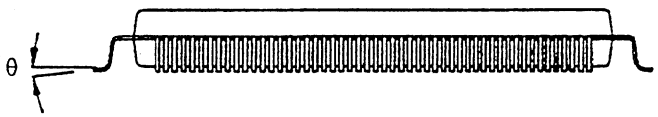
Figure 7-2 160-Pin Plastic Quad Flat Pack (PQFP)



Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A1	0.05	0.25	0.50	0.002	0.010	0.020
A2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.65			0.026	
Hd	31.65	31.90	32.15	1.246	1.256	1.266
He	31.65	31.90	32.15	1.246	1.256	1.266
L	0.65	0.80	0.95	0.025	0.031	0.037
L1		1.95			0.077	
Y			0.08			0.003
θ	0		10	0		10

Figure 7-3 208-Pin Plastic Quad Flat Pack (PQFP)





Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A1	0.05	0.25	0.50	0.002	0.010	0.020
A2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.50			0.020	
Hd	30.35	30.60	30.85	1.195	1.205	1.215
He	30.35	30.60	30.85	1.195	1.205	1.215
L	0.35	0.50	0.65	0.014	0.020	0.026
L1		1.30			0.051	
Y			0.08			0.003
θ	0		10	0		10

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