DATA SHEET

SAA7785

ThunderBird Avenger™ PCI Audio Accelerator

Preliminary specification

1999 Nov 12

Philips
Semiconductors

PHILIPS

ThunderBird Avenger™ PCI Audio Accelerator

SAA7785

GENERAL DESCRIPTION

The SAA7785 ThunderBird Avenger™ is a high-performance PCI audio accelerator offering the ultimate home theater, gaming and music solution. Armed with QSound's advanced QMSS™, ThunderBird Avenger™ transforms ordinary stereo games, movies and music to 5.1 speaker output. An integrated S/PDIF OUT connects to consumer audio equipment and S/PDIF IN support provides digital connection from a CD player or other digital audio equipment. The ThunderBird Avenger™ supports redirection of up to 5.1 streams from PCI to USB or IEEE 1394 devices. Full hardware acceleration of DirectSound™, 3D audio, music synthesis and gameport functions provides increased graphic framerates and industry leading low CPU consumption. Utilizing a specialized DSP controller and combining with a AC97 codec creates a high quality, high performance, low cost audio subsystem.

FEATURES

- 2, 4, or 5.1 speaker and headphone 3D algorithms
- QSound3DInteractive™ interactive positional 3D
- QSound Multi-Speaker System™ stereo to quad or stereo to 5.1 processing
- QSound Environmental Modeling™ (I3D Level 2.0, EAX™ 1.0/2.0 compatible)
- QXpander™ and stereo-to-3D remapping
- Integrated S/PDIF OUT and optional S/PDIF IN
- AC3 5.1 or stereo playback through S/PDIF output
- Processing up to 512 simultaneous inputs including 256 DirectSound streams and up to 96 concurrent CD quality 3D streams
- Redirection up to 5.1 streams from PCI to USB or IEEE 1394 devices via 14 Channel Virtual Write Master
- Superior hardware acceleration for minimum CPU consumption
- Broadest API compatibility including DirectSound3D™, EAX™, and A3D™
- 64 hardware wavetable polyphony
- Professional soft-synth with 256 voice polyphony and XG support
- Second generation ActiMedia programmable DSP architecture
- Global reverb for external digital and analog input sources
- Enhanced MIDI reverb and chorus (per track and global)
- Independent I^2S input and output ports
- Comprehensive Real Mode DOS and DOS windows support
- Dual gameport accelerator with leagacy and digital joystick modes
- PC/PCI, DDMA, and LAM™ PCI DMA support
- Supports quad and dual AC97 CODECS
- 3.3 v operation with 5 v tolerant I/O
- Windows(R) 95 , Windows(R) 98, and Windows(R) 2000 (WDM) drivers

APPLICATIONS

- Complete audio subsystem when combined with AC97 CODEC
- PC sound cards and motherboards
- Video games and other PCI bus-based multimedia applications

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7785	TQFP128	Thin quad flat pack; 128 leads (lead length 1.00 mm); body 14 x 14 x 1.00 mm	25-90040
SAA7785	TQFP100	Thin quad flat pack; 100 leads (lead length 1.00 mm); body 14 x 14 x 1.00 mm	25-90042

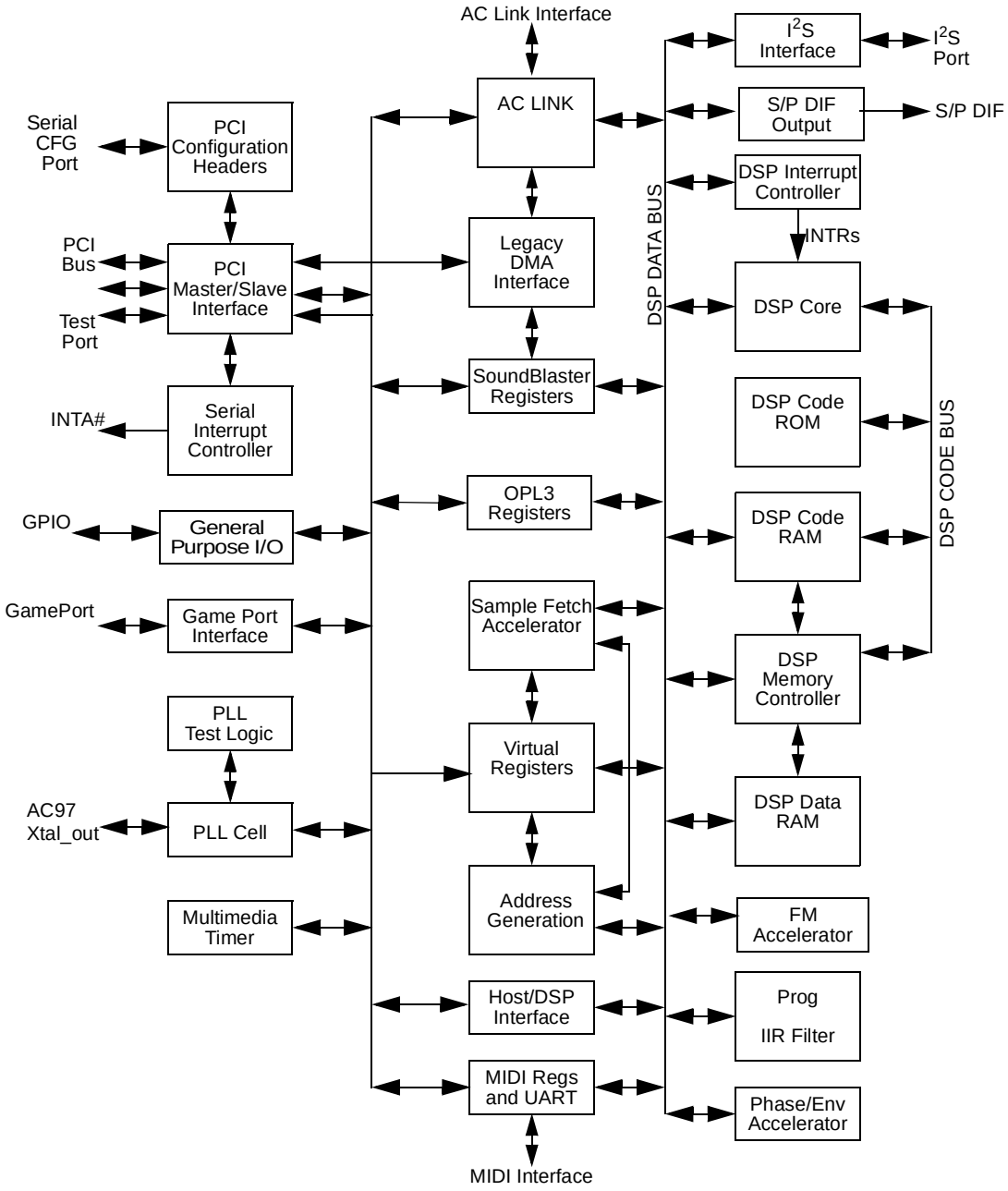
QUICK REFERENCE DATA

Condition	Symbol	Maximum Ratings
Ambient Operating Temperature	T_A	0°C to +70°C
Ambient Storage Temperature	T_S	-65°C to +150°C
Non-Operating Core and Ring Supply Voltage	VDD, VDDIC	-0.5V to 4.6V *
Operating Core Supply Voltage	VDDIC	-0.5V to 3.63V *
Operating Ring Supply Voltage	VDD	3.0V to 3.63V *
5V Tolerant Supply (5.0V nominal supply)	NWELL	-0.5V to 5.5V *
NWELL to VDD Differential	NWELL-VDD	0 ≤ (NWELL-VDD) < 4.0V
3V Tolerant I/O DC Input Voltage	V_{I3}	-0.5V to VDD+0.5V (≤ 4.6V max)+
3V Tolerant I/O DC Output Voltage	V_{O3}	-0.5V to VDD+0.5V (≤ 4.6V max)+
5V Tolerant I/O DC Input Voltage	V_{I5}	-0.5V to 5.5V (≤ 6.0V max)+
5V Tolerant I/O DC Output Voltage	V_{O5}	-0.5V to VDD+0.5V (≤ 4.6V max)+
DC Input Current (at V_I < 0V or V_I > VDD)	I_I	± 20mA
DC Output Current (at V_O < 0V or V_O > VDD)	I_O	± 20mA
Power Dissipation	P_D	500mW

*Refer to Section 3.1 to ensure proper power supply sequencing as well as voltage ranges.

+Items in parenthesis are non-operating conditions.

FIGURE 1 BLOCK DIAGRAM



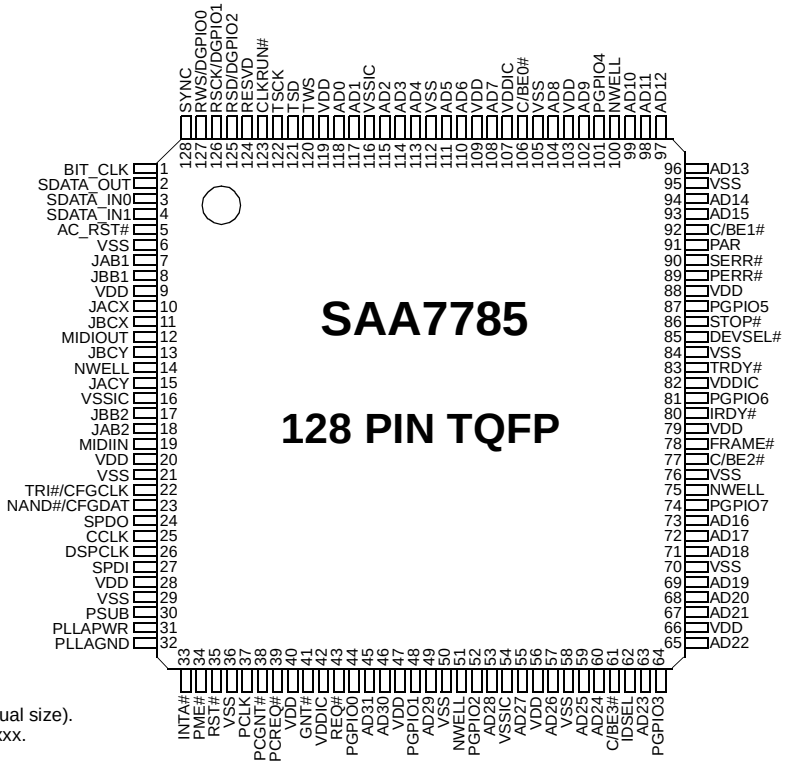
PINNING

TABLE 1 Signal and Pin Names for 128 pin SAA7785 ThunderBird Avenger™

PIN #	PIN NAME						
1	BIT_CLK	33	GNT#	65	AD22	97	AD12
2	SDATA_OUT	34	PME#	66	VDD	98	AD11
3	SDATA_IN0	35	RST#	67	AD21	99	AD10
4	SDATA_IN1	36	VSS	68	AD20	100	NWELL1
5	AC_RST#	37	PCLK	69	AD19	101	PGPIO4
6	VSS	38	PCGNT#	70	VSS	102	AD9
7	JAB1	39	PCREQ#	71	AD18	103	VDD
8	JBB1	40	VDD	72	AD17	104	AD8
9	VDD	41	GNT#	73	AD16	105	VSS
10	JACX	42	VDDIC	74	PGPIO7	106	C/BE0
11	JBCX	43	REQ#	75	NWELL3	107	VDDIC
12	MIDIOUT	44	PGPIO0	76	VSS	108	AD7
13	JBCY	45	AD13	77	C/BE2#	109	VDD
14	NWELL2	46	AD30	78	FRAME#	110	AD6
15	JACY	47	VDD	79	VDD	111	AD5
16	VSSIC	48	PGPIO1	80	IRDY#	112	VSS
17	JBB2	49	AD29	81	PGPIO6	113	AD4
18	TRI#/CFGCLK	50	VSS	82	VDDIC	114	AD3
19	MIDIIN	51	NWELL0	83	TRDY#	115	AD2
20	VDD	52	PGPIO2	84	VSS	116	VSSIC
21	VSS	53	AD28	85	DEVSEL#	117	AD1
22	TRI#/CFGCLK	54	VSSIC	86	STOP#	118	AD0
23	NAND#/CFGDAT	55	AD27	87	PGPIO5	119	VDD
24	SPDO	56	VDD	88	VDD	120	TWS
25	CCLK	57	AD26	89	PERR#	121	TSD
26	DSPCLK	58	VSS	90	SERR#	122	TSCK
27	SPDI	59	AD25	91	PAR	123	CLKRUN
28	VDD	60	AD24	92	C/BE1	124	RESVDS
29	VSS	61	C/BE3#	93	AD15	125	RSD/GPIO2
30	PSUB	62	IDSEL	94	AD14	126	RSCK/GPIO1
31	PLLAPWR	63	AD23	95	VSS	127	RWS/GPIO0
32	PLLAGND	64	PGPIO3	96	AD13	128	SYNC

FIGURE 2 PIN CONFIGURATION

SAA7785 ThunderBird Avenger™ PINS ON 128 PIN TQFP PACKAGE DIAGRAM (TOP VIEW).



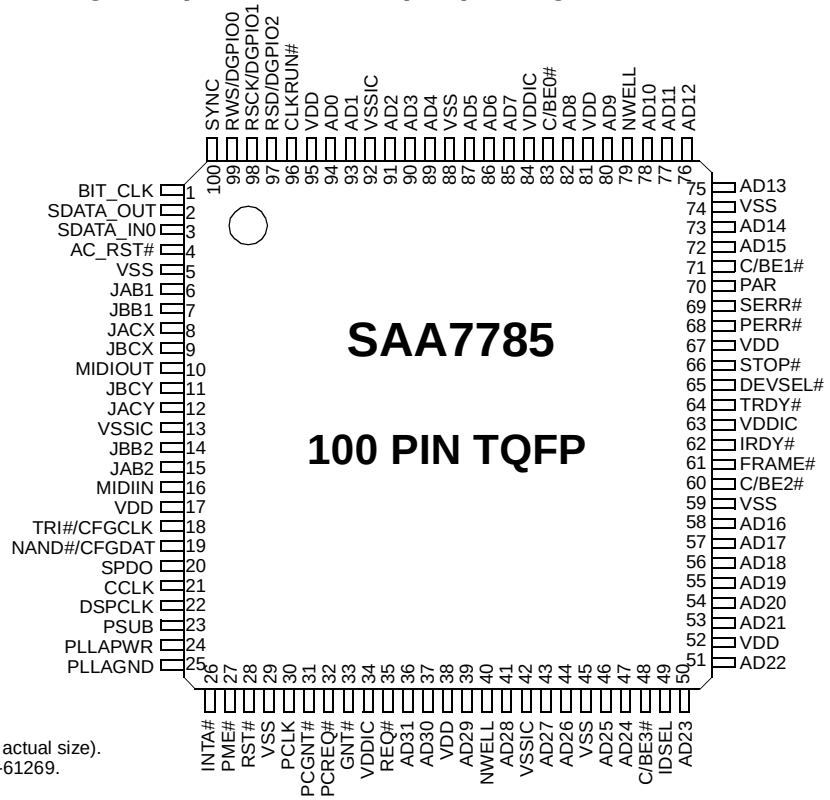
Notes:
1. Package body size is 14 mm.
2. Scale is approx 1” = 5.08 mm (5X actual size).
3. Use package bond form nuber 23-xxxxx.

PINNING

TABLE 2 PIN DEFINITIONS FOR THE 100 Pin SAA7785 ThunderBird Avenger™

PIN #	PIN NAME						
1	BIT_CLK	30	PCLK	59	VSS	87	AD5
2	SDATA_OUT	31	PCGNT#	60	C/BE2#	88	VSS
3	SDATA_IN	32	PCREQ#	61	FRAME#	89	AD4
4	AC_RST#	33	GNT#	62	IRDY#	90	AD3
5	VSS	34	VDDIC	63	VDDIC	91	AD2
6	JAB1	35	REQ#	64	TRDY#	92	VSSIC
7	JBB1	36	AD31	65	DEVSEL#	93	AD1
8	JACX	37	AD30	66	STOP#	94	AD0
9	JBCX	38	VDD	67	VDD	95	VDD
10	MIDIOUT	39	AD29	68	PERR#	96	CLKRUN#
11	JBCY	40	NWELL_40	69	SERR#	97	RSD/GPIO2
12	JACY	41	AD28	70	PAR	98	RSCK/GPIO1
13	VSSIC	42	VSSIC	71	C/BE1#	99	RWS/GPIO0
14	JBB2	43	AD27	72	AD15	100	SYNC
15	JAB2	44	AD26	73	AD14		
16	MIDIIN	45	VSS	74	VSS		
17	VDD	46	AD25	75	AD13		
18	TRI#/CFGCLK	47	AD24	76	AD12		
19	NAND#/CFGDAT	48	C/BE3#	77	AD11		
20	SPDO	49	IDSEL	78	AD10		
21	CCLK	50	AD23	79	NWELL1		
22	DSPCLK	51	AD22	80	AD9		
23	PSUB	52	VDD	81	VDD		
24	PLLAPWR	53	AD21	82	AD8		
25	PLLAGND	54	AD20	83	C/BE0#		
26	INTA#	55	AD19	84	VDDIC		
27	PME#	56	AD18	85	AD7		
28	RST#	57	AD17	86	AD6		
29	VSS	58	AD16				

SAA7785 ThunderBird Avenger™ pinout for 100 pin package



Notes:
1. Package body size is 14 mm.
2. Scale is approx 1” = 5.08 mm (5X actual size).
3. Use package bond form nuber 23-61269.

FUNCTIONAL OVERVIEW

QSound 3D Audio Algorithms

QSound Labs most advanced algorithms for 3D virtualization, multichannel processing, audio mixing and wavetable synthesis result in unsurpassed 3D audio. QSound's Q3D™ is the only solution developed natively for speakers and therefore requires no crosstalk cancellation. The result is a wide "sweetspot", strong positional perception and insensitivity to head movement and position. Listeners can enjoy a true 3D experience with only two speakers connected to their PC.

QSound Multi-Speaker System™ (QMSS™) uses a proprietary stereo-to-quad or 5.1 remapping algorithm to transform ordinary stereo into more immersive quad and 5.1 outputs. Not simply mirroring the front speaker output to the rear speakers, QMSS™ creates 4 and 5.1 individual channels. The result is DirectSound games become more realistic with action all around the listener; music CD, MP3 and MIDI playback become more immersive; and stereo and Dolby ProLogic film clips become theatre-like in presentation without needing a specific decoder.

QSound3DInteractive™ utilizes the ActiMedia™ DSP to interactively position DirectSound streams in 3D space around the listener. Four different 3D engines, based on HRTF and patented QSound technology, render sound over headphones, 2, 4 or 5.1 speakers. Q3DI™ uses the industry standard DirectSound3D™ API and is compatible with DirectSound, EAX™, and A3D1.0™ applications.

QSound Environmental Modeling™ (QEM™) adds further realism by adding reverb, occulsion and obstruction as additional positional ques. With QEM enabled, each DirectSound3D sound source receives reverb simulating acoustic reflections based on the regions reverb present and the sources' current position relative to the listener. In addition obstruction and occlusion filters are used to simulate the acoustical effects of barriers and openings in a games virtual 3D environment such as walls, doorways and pillars, and is compliant with I3D Level 2.0.

S/PDIF OUT/IN

The SAA7785 ThunderBird Avenger™ provides an integrated S/PDIF OUT port enabling users to output AC3 data from a DVD directly to an AC3 decoder. The S/PDIF stereo output capability allows users to connect to a variety of consumer audio equipment, such as a stereo receiver, minidisk, or digital speakers. S/PDIF IN support through the I^2S port enables digital connection from a CD player or other audio equipment that utilizes the S/PDIF format.

Superior Concurrency

The SAA7785 ThunderBird Avenger™ combines its 64 hardware input buffers with software (256 MIDI channels and 192 DirectSound™ inputs) for a total of 512 simultaneous streams. The ThunderBird Avenger™ can process 64 combined audio and wavetable voices in hardware plus an additional 192 audio streams using QSound's efficient MMX host engine. In addition, Avenger offers game developers up to 96 simultaneous 3D streams. For greater concurrency and higher music polyphony a professional quality 256 voice soft-synth is available. This can be used for all music synthesis reserving all 256 streams for other audio sources, making the ThunderBird Avenger™ an excellent solution for gaming applications.

Hardware Acceleration

The SSA7785 ThunderBird Avenger™ is a true hardware audio accelerator. CPU consumption is minimized by processing sample rate conversion, panning, mixing, 3D virtualization, filtering, music synthesis, multichannel conversion, and gameport functions in the hardware DSP. This frees up the host CPU to perform other tasks, boosting graphic frame rates and raising system benchmarks.

320 Voice CD Quality Wavetable Synthesis

ThunderBird Avenger™ includes two wavetable synthesis engines. When hardware mode is enabled, the ActiMedia™ DSP can produce up to 64 wavetable 44Khz, 16 bit voices. This mode minimizes CPU consumption and is ideal for games with MIDI music tracks. In addition, a professional quality soft-synth can produce up to 256 voices including special effects. The soft-synth is configurable and can be optimized for highest quality with pure music applications or for minimum CPU consumption in gaming applications. Combining both hardware and software synthesizers allows for 320

total simultaneous voices.

ActiMedia™ DSP Architecture

ActiMedia™ DSP architecture combines the strengths of programmable and fixed function DSP architectures. Programmability enables custom features, field upgrades, and simple application development, while an array of gate-efficient fixed function DSP processors (accelerators) operate in parallel to provide an excellent price/performance ratio. Unlike fixed-point DSPs that must use a single resolution for all audio processing, each accelerator is designed with the optimum resolution for its function. This provides audio integrity without the cost of high resolution or floating point programmable DSP implementation.

Digital Model Dual Game Port

The software polling used by analog game ports can consume up to 10% of the host CPU. ThunderBird PCI products utilize a digital operation mode that can eliminate software polling and accelerate the game port function resulting in significantly improved system performance. Joystick buttons can be polled or interrupt driven to further enhance performance. A default analog mode assures compatibility with DOS and other non-DirectInput™ applications.

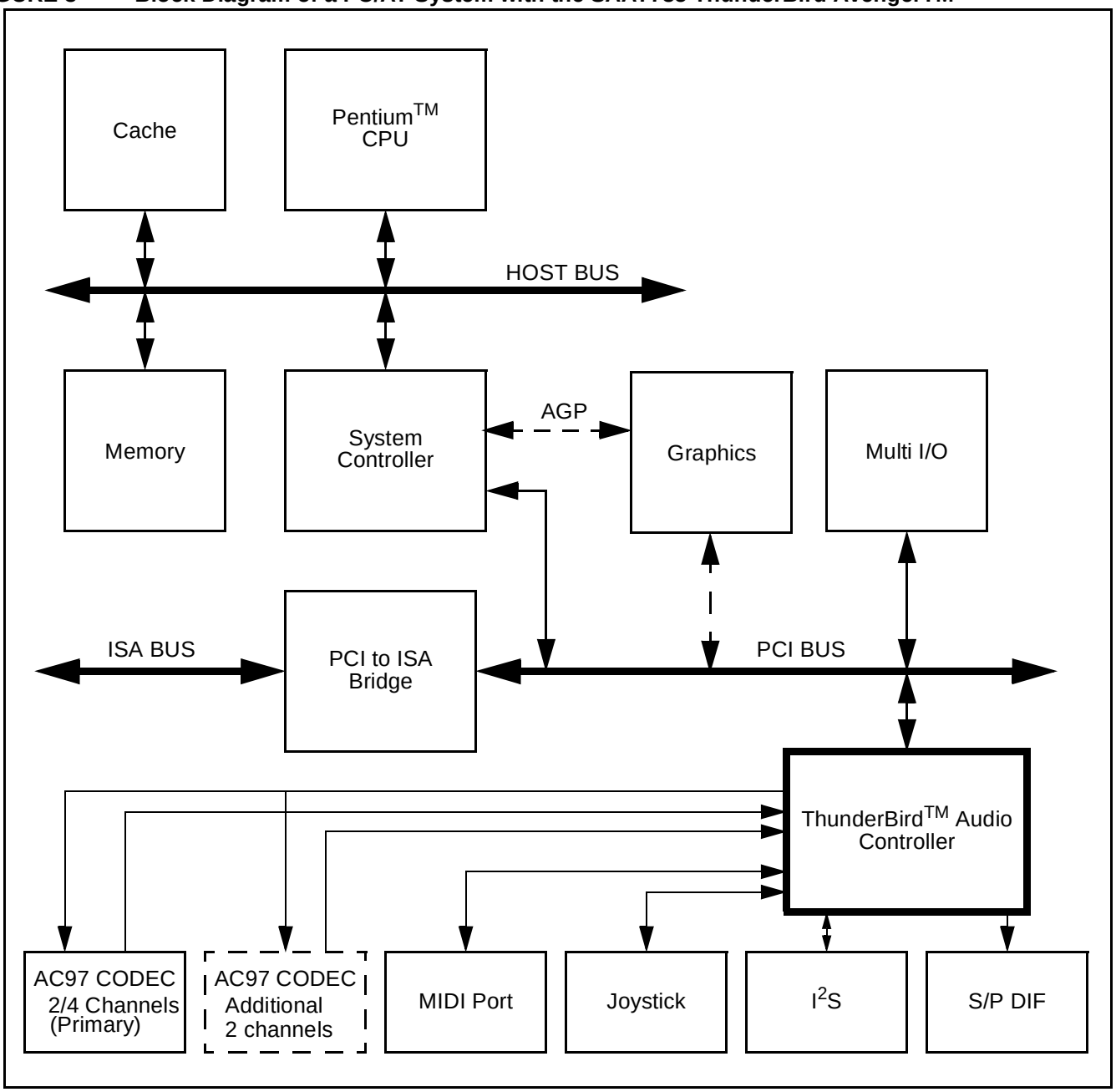
Comprehensive Legacy Audio Support

SoundBlaster Pro compatibility in both Real Mode DOS and DOS windows is achieved through hardware SoundBlaster and OPL3 (FM) emulation registers. Legacy DMA over the PCI bus is supported on all major platforms utilizing PC/PCI, DDMA, or Philips' proprietary Legacy Accommodation Mode™ (LAM™). DOS music synthesis includes stereo MIDI playback and quad/5.1 MIDI playback as well as FM emulation.

Architectural Overview

The SAA7785 ThunderBird Avenger™ is a multi-functional device that provides sound processing producing Sound-Blaster-compatible emulation, DirectSound acceleration, 3D sound, spatialization, special effects, and 64-voice wavetable synthesis through the use of a Pine Digital Signal Processor (DSP) as the primary engine. Included within the ThunderBird Q3DIII are interfaces for an AC97 codec, I^2S I/O, MIDI port, standard analog joysticks, and an S/P DIF Consumer Output port.

FIGURE 3 Block Diagram of a PC/AT System with the SAA7785 ThunderBird AvengerTM



The SAA7785 ThunderBird Avenger™ chip is designed to operate on any PCI system with the proper software support. Software support is required for non-DOS applications, such as Windows(tm) drivers. Non Pentium(tm) based system can also be supported with the additional software.

Systems that provide DDMA or have the ISA bridge on the primary PCI bus are able to perform SoundBlaster emulation enabling the operation of legacy DOS based games. The SAA7785 ThunderBird Avenger™ chip provides two 8237 style DMA channels to perform legacy DMA cycles on selected systems. The same two 8237 channels provide Distributed DMA support as well. PC/PCI is also supported to provide legacy DMA support on chipsets that support said protocol. For systems that support neither DDMA nor PC/PCI, there is a software solution implemented as a TSR.

DirectSound acceleration, both for 2D and 3D audio along with wavetable sample fetching, is accomplished using the SAA7785 ThunderBird Avenger™ chip PCI 2.1 bus master. This bus master provides the means for the SAA7785 ThunderBird Avenger™ chip to accelerate DirectSound audio streams as well as fetch wavetable sample for the 64 voice wavetable synthesis and effects algorithms. Wavetable sample fetching is always retrieved from system memory saving the cost of an external wavetable ROM. Downloadable sample sets, with software, are also supported using the bus master hardware.

Additionally, the SAA7785 ThunderBird Avenger™ chip follows the AC97 Architecture to provide high quality audio by the use of one or more separate codecs. Serial DACs, as well as AC97 CODECs can be selected to providing audio into the analog world for low cost playback. Multi-channel AC97 CODECs can be used to provide up to 8 channels of audio output.

A programmable DSP core is also provided to run the audio algorithms for wavetable synthesis, FM synthesis, special effects such as reverb and chorus, along with sample rate conversion and data management. The imbedded DSP core and its peripherals are managed solely by the DSP and requires no intervention from the host. The host can DSP can pass messages to and from each domain to provide a host software interface into the DSP domain.

PCI Interface, Configuration, and Interrupt Serializer

The SAA7785 ThunderBird Avenger™ chip PCI interface is composed of master and slave state machines, an address/data/byte enable datapath, a bus arbiter for the two on chip masters, control logic for the master and slave internal busses, an interrupt serializer, and the standard PCI configuration register header.

The standard PCI configuration header is also supported. Since the SAA7785 ThunderBird Avenger™ is a multi-function device, there are three PCI configuration spaces allocated for each function. The three functions are the audio device, the joystick and the 16650 UART. The purpose of the multiple configuration headers is to ensure PCI compliance and enable the operating system to select the correct software driver for each individual device. The Serial CFG Port is used to shift in subvendor specific data for each of the PCI configuration headers. The Serial CFG port is an industry standard I^2C™ format. The configuration headers are included in the PCI interface to reduce inter-block routing. All other PCI configuration space registers are included in the blocks that utilize these registers.

Clocks and the PLL Subsystem

Clocks for operation of the SAA7785 ThunderBird Avenger™ are derived from two sources; an external crystal and bit clock from the AC97 CODEC. The SAA7785 ThunderBird Avenger™ PLL Subsystem derives its reference from the external crystal.

The SAA7785 ThunderBird Avenger™ substem consists of a fixed layout PLL cell and a digital interface to the 8 bit PS bus. The PLL is designed to drive the clocks for the DSP subsystem. The implementation calls for the PLL to be utilized with complete programmable register interface to enable the tuning of the frequencies as necessary.

Multimedia Timer

The SAA7785 ThunderBird Avenger™ chip supplies a 20-bit, .84 uS resolution timer for game synchronization. The

timer data can be accessed as an I/O device. This timer can be used by game developers to keep track of time elapsed to synchronize the video to the audio stream. The timer can be polled or interrupt driven and is selectable by the user application.

DMA

DMA is for the Sound Blaster registers, the DSP Mastering Device (DMD), and the S/P DIF output. To cover as many systems as possible, the DMA interface supports three modes for legacy support: Mobile PC/PCI DMA Arbitration (PC/PCI), Distributed DMA (DDMA) and Legacy Accommodation Mode (LAM).

Legacy Accommodation Mode allows the SAA7785 ThunderBird Avenger™, in an architecturally compatible system, to snoop and snarf selected DMA cycles on the PCI bus that were intended to the ISA Bridge. If a chip set supports Distributed DMA, the SAA7785 ThunderBird Avenger™ will use this method since it is more efficient than LAM. Additionally, PC/PCI can be utilized as well if neither DDMA nor LAM are supported on the selected chip set.

AC Link

The SAA7785 ThunderBird Avenger™ chip provides support for the AC97 (V2.1) specification by supplying an AC Link interface to communicate with industry standard AC97 CODECs. Up to two CODECs can be used for a total of 8 possible outputs (4 stereo channels).

Sound Blaster Registers

The other device that requires DMA is the SoundBlaster registers. DMA is used to transfer SoundBlaster digital audio files from the host to a codec for playback in addition to providing a mailbox for other commands. In order for the DSP to emulate the Sound Blaster sound effects, a legacy register set must be implemented to capture these commands. These sixteen, 16-bit registers are used primarily to emulate SoundBlaster Pro register set as well as the SoundBlaster Pro mixer registers. These registers are used as a mailbox to the DSP data bus to deliver data to the SoundBlaster Emulation code. The SAA7785 ThunderBird Avenger™ chip supports DMA to the Sound Blaster that legacy code requires. All data transmitted over the SoundBlaster Registers is processed by the DSP to emulate the Sound Blaster Pro hardware.

OPL3 Registers and the FM Accelerators

The OPL3 register interface is a subset of the complete SoundBlaster register set. The OPL3 registers are separate to point out that the FM legacy is supported at the register level. The OPL3 registers simply pass FM synthesis commands to the SoundBlaster Emulation code and receive status from the same code.

Virtual Registers

The Virtual Registers interfaces the PCI bus and two substantial wavetable synthesis accelerators: the Sample Fetch and Address Generation accelerators. The Virtual Registers is responsible for setting up the PCI interface for master cycles data fetches and retrieving those fetches into a sample buffer. The Virtual Registers get commands from the Address Generation accelerator and turns them into PCI master requests. Once the data has been retrieved, the Virtual Register then instructs the Sample Fetch accelerator to process a block of data. Once the processing is complete, the Sample Fetch Accelerator notifies the Virtual Registers that all is clear and that new data can be processed.

Address Generation Accelerator

The Address Generation accelerator is a preprocessing unit for the sample fetching mechanism inside the Virtual Registers. The Address Generator will get a set of parameters from the DSP code on a per voice basis for either Direct-Sound processing or wavetable synthesis. Once these voice parameters are set, the hardware is instructed to translate

the addresses and fetch the audio samples from system memory. The Address Generator is also capable of looping without intervention from the DSP code. The DSP kills voices by instructing the Address Generator to stop fetching data. Once the samples are fetched, they are stored in the Virtual Register's input sample buffer for processing by the Sample Fetch Accelerator.

Sample Fetch Accelerator

The Sample Fetch accelerator is used to process audio samples fetched by the Virtual Registers and deliver them to the DSP code for further processing. This processing can include pitch shifting or sample rate conversion. The degree of pitch shifting is under direction of DSP code indicating the Sample Fetch accelerator is programmable. The input samples are taken from the Virtual Register's input sample buffer and stored in DSP memory space.

MIDI Registers and UART

An MPU401 compatible UART is supplied to enable external MIDI devices to use the SAA7785 ThunderBird Avenger™ chip synthesizers as well as its external device's own synthesizer. The MIDI register interface is used to pass the MIDI command stream from the host to the DSP firmware for parsing into synthesizer commands. The MPU401 UART always operates in "dumb" mode. Both the PCI and DSP can access the MIDI UART directly. Data is presented from/to the MPU401 Registers in a mailbox fashion to the MPU401 UART.

General Purpose Input/Output

There are seven general purpose I/O pins that are controlled by the PCI bus (128 pin version). No GPIOs are available in the 100 pin package.

PINE DSP Core

The Pine DSP core is a programmable 16-bit integer DSP with separate code and data busses (Harvard architecture). Main features of the DSP core include 2K x 16 data RAM, 64K word code and data space, 16 x 16 bit two's complement parallel multiplier with 32-bit product, single cycle multiply/accumulate instructions, 36-bit ALU, two 36-bit accumulators, six-general purpose 16-bit pointer registers, option for up to eight user-defined 16-bit registers, zero overhead looping, repeat and block-repeat instructions with one nesting level, shifting capability, automatic saturation mode on overflow while reading content of accumulators, divide and normalize step support.

As noted on Figure 2, the DSP subsystem is supported by two dedicated Pine internal busses called the DSP code bus and the DSP data bus. All DSP peripherals are connected to the DSP data bus while the code bus is used for just that, DSP code ROM and RAM. Both the DSP code and data busses are 16-bit for the address and data lines on each bus. DSP code also enables the DSP core to act as a PCI bus master making it a powerful and flexible audio processing unit.

DSP Interrupt Controller

The DSP Interrupt Controller is a programmable, priority encoded device that encodes two interrupt signals to the Pine core. The DSP Interrupt Controller resides on the DSP data bus and is programmed by DSP code. Both sets of interrupt vectors feature an enable and status bit for each interrupt based device.

DSP Memory Controller

The DSP memory controller provides controls and decodes for the regular DSP data and code RAMs as well as the code ROMs. The Memory Controller also includes a patch mechanism to allow ROM code to be updated or fixed using a trapping device.

SERIAL PORT INTERFACES

OVERVIEW

The SAA7785 chip will contain an S/PDIF Consumer Grade transmit port and an I^2S transmit/receive pair. These serial ports are designed to exchange digital audio data but can be used for any type of data transfer assuming the bandwidth is adequate. Currently, these ports are connected to the DSP data bus.

The Inter-IC Sound Bus, or I^2S Port, is a simple interface used to transfer digital data from one source to another. The interface is based on a continuous serial clock that determines the data rate along with the word select line and the data lines. An I^2S port can be a master or a slave device. A master device drives the serial clock and word select lines while a slave device receives the clocking signals. The SAA7785 I^2S ports are independently programmable to be either a master or a slave and for 32.0, 44.1 and 48.0KHz stereo data transfer.

Also included is a Sony/Philips Digital Interface Format, or S/PDIF, serial port. This interface is generally used to transmit raw audio data but is also used to transfer AC-3 encoded data as well using DMA. The S/PDIF format is a synchronous interface with the clock encoded on the data stream. The S/PDIF ports support 32.0, 44.1 and 48.0KHz stereo data transfer up to 24 bits. The S/PDIF interface is IEC958 Consumer Grade compliant.

FIGURE 4 I²S SERIAL PORTS BLOCK DIAGRAM

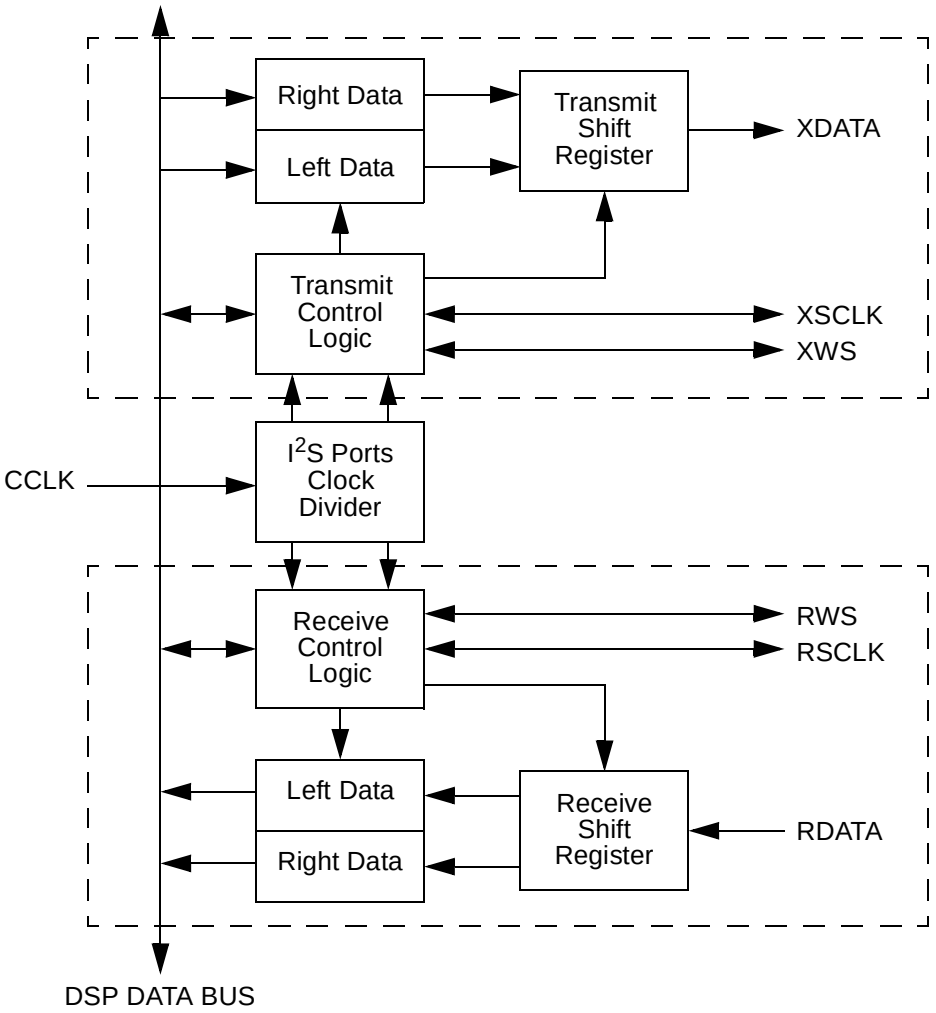
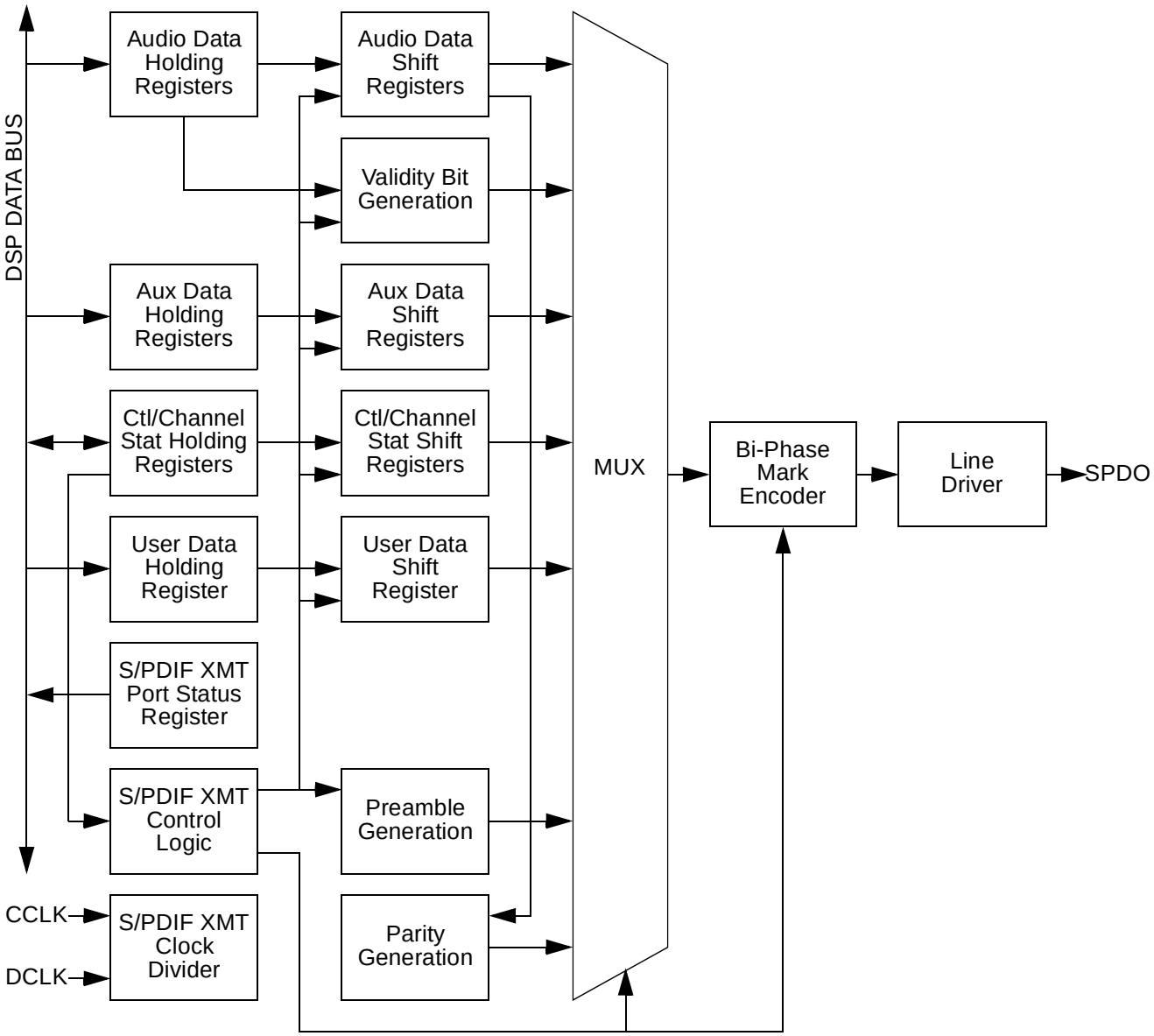


FIGURE 5 S/PDIF TRANSMIT PORT BLOCK DIAGRAM



VIRTUAL WRITE MASTER

Audio streams may be directed back to host memory from the DSP domain. The VWM has a data buffer capable of storing enough audio data to burst into the host memory. The VWM is a simplified version of DMA and has more stringent requirements on which and how many pages need to be allocated.

Using the VWM, the system programmer can redirect audio streams processed by the SAA7785 ThunderBird Avenger™ device and use them in any other audio device that resides in the system. The VWM is more efficient than the DMA and should be the device of choice when redirecting audio streams back to the host. The device supports audio sample rates from 8 to 48 KHz.

Game Port

The SAA7785 ThunderBird Avenger™ Game Port interface is designed to emulate the PC-AT based legacy joystick operation as well as support of a digital joystick mode. The legacy or analog, type of operation is designed to support all legacy software that uses the original joystick address and the method for resolving the joystick axes positions. The Digital Mode is designed to reduce the joystick overhead by resolving the joystick position directly and to support applications that use DirectInput.

The legacy joystick used a one shot multi-vibrator on each of the four joystick potentiometers. These one shots were set up to deliver a pulse that was proportional to the resistor value of the joystick potentiometers. Software would them poll the one shots to see if they had been set to the original value. The time it took for each axes to return to the original value was resolved into a position by the legacy software. The SAA7785 ThunderBird Avenger™ emulates the 558 based one shot circuit to support legacy games that use the PC-AT joystick. The joystick button values were routed directly to the system bus where only a decode was required to read the value of the button. Software would poll the buttons as well. All button and joystick axes data is returned in a single byte wide register.

Game Port Legacy I/O Register

This register is the legacy mode register for the 558 based joystick. When in “analog” mode, this register is aliased to respond to addresses at base + (0-7) . Reads from this register will poll the status of the joystick buttons and are used to resolve the position. Writes to this register will discharge the external capacitors to emulate the 558 one shots. Software can then poll the joystick register bit to resolve each of the joystick axes positions by timing. The joystick button register bits have meaning in both the digital and analog modes. The axes bits are only valid for analog mode.

TABLE 3 Game Port 558-Based Register - GAMEPORT (RO)

I/O GMBASE	D7	D6	D5	D4	D3	D2	D1	D0
Offset 1h	JOYB_2	JOYB_1	JOYA_2	JOYA_1	JOYB_Y	JOYB_X	JOYA_Y	JOYA_X
POR Value	1	1	1	1	0	0	0	0

Bit	Name	R/W	Function
7	JOYB_2	RO	Joystick B button 2 status. The joystick button status bits are cleared when the respective joystick button is pressed.
6	JOYB_1	RO	Joystick B button 1 status.
5	JOYA_2	RO	Joystick A button 2 status.
4	JOYA_1	RO	Joystick A button 1 status.
3	JOYB_Y	RO	Joystick B y-coordinate. Can also be referred to as position 3.
2	JOYB_X	RO	Joystick B x-coordinate. Can also be referred to as position 2.
1	JOYA_Y	RO	Joystick A y-coordinate. Can also be referred to as position 1.
0	JOYA_X	RO	Joystick A x-coordinate. Can also be referred to as position 0.

SAA7785 SIGNAL DEFINITIONS

PCI LOCAL BUS INTERFACE SIGNALS

AD[31:0] **PCI Address/Data**

AD[31:0] contains a physical byte address during the first clock of a PCI transaction, and data during subsequent clocks.

When the SAA7785 is a PCI master, AD[31:0] are outputs during the address phase of a transaction. They are either inputs or outputs during the data phase, depending on the type of PCI cycle in process.

When the SAA7785 is a PCI slave, AD[31:0] are inputs during the address phase. They are either inputs or outputs during the data phase, depending on the type of PCI cycle in process.

C/BE#[3:0] **PCI Bus Command and Byte Enables**

C/BE#[3:0] defines the bus command during the first clock of a PCI transaction, and the byte enables during subsequent clocks.

C/BE#[3:0] are outputs when the SAA7785 is a PCI bus master and inputs when it is a PCI bus slave.

DEVSEL# **PCI Bus Device Select**

When the SAA7785 is a PCI bus master the SAA7785 uses DEVSEL# to determine whether a master abort should occur if DEVSEL# is not sampled active by clock 5 of the transaction, or to determine whether a cycle is to be aborted or retried when a target-initiated termination occurs.

When the SAA7785 is a PCI bus slave, DEVSEL# is an output which the SAA7785 drives LOW during the second PCLK after FRAME# assertion to the end of a transaction if the SAA7785 is selected.

FRAME# **PCI Bus Cycle Frame**

When the SAA7785 is a PCI master, FRAME# is an output which indicates the beginning of a SAA7785-initiated bus transaction. While FRAME# is asserted data transfers continue. When FRAME# is deasserted the transaction is in the final data phase.

When the SAA7785 is a PCI slave, FRAME# is an input that initiates an I/O, memory or configuration register access if the SAA7785 is selected for the transaction. The SAA7785 latches the C/BE#[3:0] and AD[31:0] signals on the PCLK edge on which it first samples FRAME# active.

IRDY# **PCI Bus Initiator Ready**

When the SAA7785 is a PCI master, IRDY# is an output which indicates the SAA7785's ability to complete the data phase of the current transaction. It is always asserted from the PCLK cycle after FRAME# is asserted to the last clock of the transaction.

When the SAA7785 is a PCI slave, IRDY# is an input which causes the SAA7785 to hold-off completion of a read or write cycle until sampled active.

STOP# **PCI Bus Stop (Target Initiated Termination)**

When the SAA7785 is a PCI master, STOP# is an input which causes the SAA7785 to complete, abort or retry the transfer, depending on the state of TRDY# and DEVSEL#.

When the SAA7785 is a PCI slave, it drives STOP# as active (LOW) to terminate or retry a transaction.

TRDY# **PCI Bus Target Ready**

When the SAA7785 is a PCI master, TRDY# is an input which indicates the target agent's ability to complete the data phase of the transaction. After initiation of a PCI bus transaction, the SAA7785 inserts wait cycles until TRDY# is sampled active.

When the SAA7785 is a PCI slave, it drives TRDY# active to indicate that the SAA7785 has sampled the data from AD[31:0] during a write phase, or presented valid data on AD[31:0] during a read phase.

PAR **PCI Bus Parity**

When the SAA7785 is a PCI master, it drives PAR to reflect the correct value for even parity on the AD[31:0] and C/BE#[3:0] buses one clock after the address phase and after each write data phases.

When the SAA7785 is a PCI slave, it drives PAR to reflect the correct value for even parity on the AD[31:0] and C/BE#[3:0] buses one clock after completion of each read data phase.

PCREQ# **PC/PCI DMA Request**

This signal requests DMA series from an external chipset that supports PC/PCI protocols. The SAA7785 chip asserts PCGNT# according to the desired DMA channel required by either the SoundBlaster or AC97 interfaces. The requested channel is encoded serially on the PCGNT# pin.

The SAA7785 will become the bus owner when it receives an asserted PCGNT# signal. This handshaking is synchronous to PCLK.

PCGNT# **PC/PCI DMA Grant**

An asserted PCGNT# pin indicates that the external PC/PCI master arbiter has granted DMA services to the encoded DMA channel to the requesting DMA agent on the SAA7785 chip.

REQ# **PCI Bus Request**

This signal controls the PCI bus arbitration between the SAA7785 chip and the PCI master arbiter. When REQ# is asserted, the SAA7785 indicates a desire to become the PCI bus owner. The SAA7785 will become the bus owner when it receives an asserted grant signals (GNT# is LOW). This handshaking is synchronous to PCLK.

REQ# is three-stated while RST# is active.

GNT# **PCI Bus Grant**

An asserted GNT# pin indicates that the PCI master arbiter has granted bus ownership to the SAA7785 chip.

INTA# **PCI Bus Interrupt A**

The interrupt output is a PCI compatible active low level sensitive interrupt. It is only used if the SAA7785 is used in a non Common Architecture system. Otherwise it is tri-stated. It is driven low when any of the internal interrupts are asserted.

PERR# **PCI Bus Parity Error**

This signal indicates a data parity error for any cycle type other than a Special Cycle command. PERR# is made active two clocks after the completion of the data phase which caused the parity error. This error signal may result in the generation of a non-maskable interrupt (NMI) or other high priority interrupt sent to the CPU.

SERR# **PCI Bus System Error**

This signal indicates an address parity error, data parity errors on Special Cycle commands or any other catastrophic system error. SERR# is an open-drain bidirectional pin which is driven low for a single PCLK cycle by the agent reporting the error. This error may result in the generation of a non-maskable interrupt (NMI) or other high priority interrupt sent to the CPU.

IDSEL **Initialization Device Select**

IDSEL is used as a chip select during configuration register read and write operations. One system board address line from AD[31:11] is used as IDSEL to select the SAA7785 configuration space in the SAA7785 chip when used on the PCI bus.

CLKRUN# **PCI Bus Clock Run Request**

The SAA7785 uses CLKRUN# according to the Mobile PCI protocol to start the PCI clock or keep the clock running whenever an internal PCI device requires it.

PCLK **PCI Bus Clock Input**

PCLK is the PCI bus clock input. It is used to synchronize all PCI bus operations and typically runs at 33MHz.

RST# **PCI Bus Reset**

An active low version of the system reset, this signal causes the PCI interface to return to the idle states in all state machines and asynchronously three-states all PCI bus signals. All registers will be reset to their default values as well. The CODEC interface line should be all driven inactive along with the external memory interface. This reset will assert the DSP reset.

PME# **PCI Bus Power Management Event**

Reserved.

PCI GENERAL PURPOSE I/O

PGPIO[7:0] **PCI General Purpose Input/Outputs**

These eight pins are used as controls or data to devices external to the SAA7785 chip. Each are independently controlled.

TEST INTERFACE/SERIAL CONFIGURATION PORT

NAND#/CFG-DAT **NAND Tree Test Enable/Serial Configuration Data**

When this pin is pulled low and RST# is pulsed asserted, all output and I/O pins of the SAA7785 will be forced into a three-state condition. Pulsed assertion of the RST# signal will release the SAA7785 from this test mode.

If this pin is pulled high during PCI reset, then it is used to shift in PCI configuration data for the Subsystem ID and the Subsystem Vendor ID in each of the PCI configuration headers present in the SAA7785 chip. The Serial Configuration Port is a standard I^2C interface. This line should never be pulled low.

TRI#/CFGCLK **Tri-State Test Enable/Serial Configuration Clock**

When this pin is pulled low and RST# is pulsed asserted, the SAA7785 will enter the parametric NAND tree test mode. The details of the NAND tree test mode are described later in this document.

If this pin is pulled high during PCI reset, then this pin will supply the serial 400 KHz clock, derived from OSC, to an external serial EEPROM. CFGCLK is used to synchronize the serial configuration data.

GAME PORT INTERFACE

JACX **Joystick A X Axis**

This pin functions as an input for the joystick A X-position axis.

JACY **Joystick A Y Axis**

This pin functions as an input for the joystick A Y-position axis.

JBCX **Joystick B X Axis**

This pin functions as an input for the joystick B X-position axis.

JBCY **Joystick B Y Axis**

This pin functions as an input for the joystick B Y-position axis.

JAB2 **Joystick A Button 2 Interface**

This pin functions as an input for the joystick A button 2.

JAB1 **Joystick A Button 1 Interface**

This pin functions as an input for the joystick A button 1.

JBB2 **Joystick B Button 2 Interface**

This pin functions as an input for the joystick B button 2.

JBB1 **Joystick B Button 1 Interface**

This pin functions as an input for the joystick B button 1.

MIDI INTERFACE

MIDIIN **MIDI Serial Data Input**

This signal is part of the standard 2 wire MIDI interface. This input receives MIDI data at a rate of 31.25Kbaud. Optical isolation is required.

MIDIOUT **MIDI Serial Data Output**

This signal is part of the standard 2 wire MIDI interface. This output transmits MIDI data at a rate of 31.25Kbaud. Optical isolation is required.

AC'97 CODEC INTERFACE

SYNC **AC'97 Codec Synchronization/Frame Output**

This signal is used to frame the tag packet from the AC link designer from the SAA7785 chip.

BIT_CLK **AC'97 Data Bit Clock**

This signal is used to clock synchronous data on the AC link interface.

SDATA_OUT **AC'97 Serial Data Out**

This is the time division multiplexed serial output data stream from the SAA7785 controller.

SDATA_IN0 **AC'97 Serial Data In Port 0**

This is the time division multiplexed serial input data stream from the primary external AC'97 codec.

SDATA_IN1 **AC'97 Serial Data In Port 1**

This is the time division multiplexed serial input data stream from the secondary external AC'97 codec.

AC_RST_N# **AC'97 Master Reset**

The external AC'97 codec has a master reset line which is has a separate control. The codec status must report a ready before any audio or modem data is transmitted to the codec.

DSP SERIAL PORTS/GENERAL PURPOSE I/O

SPDO **Sony/Philips Digital Interface Format Output Port**

Consumer format S/PDIF Output Port. The output characteristic of this pad approximates the RS422 interface.

SPDI **Sony/Philips Digital Interface Format Input Port**

Reserved.

RWS **Inter-IC Sound Bus Receive Port Word Select Clock/DSP General Purpose I/O 0**

When the I^2S is configured as a master, this pin will output a word clock at the frequency selected by the user. When configured as a slave, the receive port will synchronize the left or right channel data to this signal.

RSCK **Inter-IC Sound Bus Receive Port Bit Clock/DSP General Purpose I/O 1**

When the I^2S is configured as a master, this pin will output a bit clock. When configured as a slave, the receive port will shift in data from the RSD data stream using RSCK as an input.

RSD **Inter-IC Sound Bus Receive Port Data/DSP General Purpose I/O 2**

This pin is the input data stream for the I^2S receive port.

TWS **Inter-IC Sound Bus Transmit Port Word Select Clock**

When the I^2S is configured as a master, this pin will output a word clock at the frequency selected by the user. When configured as a slave, the receive port will synchronize the left or right channel data to this signal.

TSCK **Inter-IC Sound Bus Transmit Port Bit Clock**

When the I^2S is configured as a master, this pin will output a bit clock. When configured as a slave, the transmit port will shift out data from the TSD data stream using TSCK as an input.

TSD **Inter-IC Sound Bus Transmit Port Data**

This pin is the output data stream for the I^2S transmit port.

PLL/DSPCLK SUBSYSTEM INTERFACE

CCLK **CODEC Clock Input**

This pin is the raw 24.576MHz clock from the AC'97 crystal. The CCLK clock is used to provide a fixed time base for many functions within the SAA7785 device.

DSPCLK **DSP Clock Input**

This pin can be used as the clock input for the SAA7785 for the DSP subsystem in place of the PLL driving the clock. DSPCLK is also used to drive the DSP subsystem for controllability during testing.

PSUB **PLL Substrate**

This pin supplies the bias for the guard ring on the PLL core. Connect this to a clean analog supply ground.

PLLAPWR **PLL Analog Power**

Analog power supply for the PLL. Be sure the analog supply is isolated from the 3 volt digital supply.

PLLAGND **PLL Analog Ground**

Analog ground for the PLL. This power supply is sensitive to noise and should be handled carefully.

POWER AND GROUND PINS

VDDIC **Core Power**

3 volt power supply for the core of the chip.

VSSIC **Core Ground**

Ground reference for the core of the chip.

VSS **Ring Ground**

Ground reference for the pad interfaces of the chip.

VDD **Ring Power**

3 volt supply for the pad interfaces of the chip.

NWELL **External N-Well Bias**

Tie these pins to 5v for proper 5 volt tolerant operation. The 5v supply must be powered up before the 3v supply. Likewise, the 3v supply must be powered down before the 5v supply. **PLEASE READ THE CAUTIONS IN Section 4.1, POWER SUPPLY OPERATING REQUIREMENTS ***** MUST READ *****

DSP EXTERNAL MEMORY INTERFACE

MA[14:0] **External Memory Address**

Address lines for the external SRAM devices. The external memory interface can be used for DSP code space if the EXT_SRAM_EN (in HDCFG, bit 5) is set. Otherwise, the DSP will use internal ROM as the code source.

MD[15:0] **External Memory Data Bus**

Word wide data bus for the external SRAM. Use 6ns memory for maximum DSP performance.

MCS# **External Memory Chip Select**

Chip select line for the external SRAM devices.

MWE# **External Memory Read/Write Control**

Selects the external SRAM for reading or writing.

SAA7785 ThunderBird Avenger™ Functional Block Descriptions

Register Table Document Description and Example

The next table gives an example of how registers are documented in this specification.

TABLE 4 Example Register - REGEX (RW/RO)

SPACE	D15	D14	D13	D12	D11	D10	D9	D8
Offset nnh	R	R	R	R	R	R	R	R
POR Value	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	EXDATA[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
15:8	R	RO	Reserved. These bits always return zeros.
7:0	EXDATA	RW	Example data. The example data for all to see.

In the above table example, the EXAMPLE REGISTER text would be a descriptive title for the register that we wish to detail. Following the register description would be a register mnemonic used in register summary tables and the like. In this example the mnemonic is REGEX. Following the mnemonic is the read/write access allowed into this register. If the entire register is readable and writable, then the RW key is assigned. If some bits are read/write while others are read only, then the key will indicate this fact. In the example, this register has both read/write and read only bits. The register memory map location is marked in the table cell marked SPACE. SPACE could be substituted with PCI CFG n (for PCI configuration register space for function n), IOBASE (for an I/O space register with an IOBASE specified in a configuration register), DSP DATA (for DSP data memory mapped registers), MEM MSTR (indicating a PCI master in memory space), and DSP CODE (indicating a DSP code memory mapped register. Just below the SPACE marker is the offset from the base address specified in the SPACE field. The rest of the table should be obvious.

SAA7785 ThunderBird Avenger™ PCI Interface

Overview

The SSA7785 ThunderBird Avenger™ chip PCI interface is designed to interface the external PCI bus interface to all of the selected devices in the SSA7785 ThunderBird Avenger™ chip. The PCI interface composed of master and slave state machines, an address/data/byte enable datapath, a bus arbiter for the two on chip masters, control logic for the master and slave internal busses, and standard PCI configuration register headers. The Interrupt Serializer will be discussed in a later chapter. This section of the specification will describe the PCI interface in more detail along with design considerations for both the slave, master, and datapath. The configuration header will be discussed in the SSA7785 ThunderBird Avenger™ PCI Configuration Registers section of this specification.

The discussion will begin with the PCI master and target systems. The PCI bus master has the capability to burst double words to/from the two internal bus masters, the Distributed DMA and the Virtual Registers. The full address range is supported for these master devices. Since there are two masters, an arbiter is required to determine priority between the two devices. Details on the arbiter can be found in the PCI master section.

The PCI datapath block contains the multiplexors and registers to steer the data to and from the PCI interfaces. The data is de-multiplexed from the external PCI interface to the internal master and slave busses. Control logic from the master and slave devices control the datapath.

The SSA7785 ThunderBird Avenger™ is considered a multi-function device since the operating system may wish to load different drivers for certain functions. These functions are the audio subsystem, the joystick and the 16650 UART. Each of these major functions must have a separate PCI configuration space. The standard PCI configuration header for these three functions are supported in the PCI interface.

The SSA7785 ThunderBird Avenger™ PCI interface responds to and initiates PCI cycles with positive decoding according to the PCI 2.1 specification. The interface asserts DEVSEL# after the first clock following FRAME# making it a medium responder. For specific LAM cycles, the SSA7785 ThunderBird Avenger™ will be a fast responder. SSA7785 ThunderBird Avenger™ indicates which cycles the PCI interface responds to or initiates.

TABLE 5 PCI Bus Command Definitions and SSA7785 ThunderBird Avenger™ Responses

c/be#[3:0]	Command Type	SSA7785 ThunderBird Avenger™ Response to Cycle
0000	Interrupt Acknowledge	This cycle is not claimed.
0001	Special Cycle	This cycle is not claimed.
0010	I/O Read	All I/O Read cycles directed to the SSA7785 ThunderBird Avenger™ are claimed by the target interface.
0011	I/O Write	All I/O Write cycles directed to the SSA7785 ThunderBird Avenger™ are claimed by the target interface.
0100	Reserved	This cycle is not claimed.
0101	Reserved	This cycle is not claimed.
0110	Memory Read	This cycle is not claimed.
0111	Memory Write	This cycle is not claimed.
1000	Reserved	This cycle is not claimed.
1001	Reserved	This cycle is not claimed.
1010	Configuration Read	All Configuration Read cycles are claimed by the target interface provided IDSEL is sampled asserted during the address/cmd phase.
1011	Configuration Write	All Configuration Write cycles are claimed by the target interface provided IDSEL is sampled asserted during the address/cmd phase.
1100	Memory Read Multiple	This cycle is not claimed.
1101	Dual Address Cycle	The SSA7785 ThunderBird Avenger™ supports 32-bit addresses only.
1110	Memory Read Line	This cycle is not claimed.
1111	Memory Write and Invalidate	This cycle is not claimed.

The SSA7785 ThunderBird Avenger™ will respond to byte, word, tri-byte or double word access for configuration read and configuration write cycles provided PCI addressing rules are followed. Byte and word width accesses allowed for I/O cycles depend largely on the target I/O device. In general, 24-bit and 32-bit accesses are not allowed to I/O devices and will result in a target abort. The SSA7785 ThunderBird Avenger™ performs double word accesses when initiating

master cycles. Note that the SSA7785 ThunderBird Avenger™ cannot initiate a master cycle to itself. SSA7785 ThunderBird Avenger™ summarizes the access rules for configuration and I/O cycles.

TABLE 6 BIT Width Device Access Rules

Device	Cycle Types	Data Width	Comments
PCI Configuration Registers	Config Read Config Write	Any	Follow PCI addressing rules, otherwise assert a target abort. Note that configuration registers, no matter where they are, are accessed by configuration cycles only. Note that the PLL will only allow 8 bit configuration accesses, the Virtual Registers TBLBASE registers are 32 bit access only, and the VRCFG is 16 bit access only.
Game Port	I/O Read I/O Write	8	Any other access will result in a target abort.
AC'97 Codec	I/O Read I/O Write	16	For PIO type accesses, only 16 bit I/O cycles are allowed, other wise a target abort will result.
DMA Interface	I/O R/W	Any	
Sound Blaster Registers	I/O Read I/O Write	8	Any other access will result in a target abort.
Virtual Registers	Mem Read	Any	Follow PCI addressing rules.
Host/DSP Interface	I/O Read I/O Write	8,16	Usually, only 16 bit accesses will be used to download and access the DSP. Byte wide are also allowed for DSP configuration accesses. Word accesses must be on word boundaries.
MPU401 Registers	I/O Read I/O Write	8	Any other access will result in a target abort.
16650 UART	I/O Read I/O Write	8	Any other access will result in a target abort.

The PCI interface consists of three major blocks, the PCI master interface, the PCI slave interface and the PCI datapath. The PCI master interface contains the master state machine, the master control logic, and the PM bus arbiter. The PCI slave interface contains the target state machine, the target control logic and configuration register headers. The PCI datapath is the de-multiplexing logic for the address, data and byte enable data paths for the PS and PM busses. The PM and PS busses are described in detail in the SSA7785 ThunderBird Avenger™ Internal Busses section. Partitioning of these PCI blocks are done in this manner to reduce block inter-connectivity and to provide an interface between the three major sections of the PCI interface.

PCI Master Interface

The SSA7785 ThunderBird Avenger™ PCI master interface performs the memory read and write cycles initiated by the DMA or Virtual Registers blocks. The major components of the PCI master interface are the master state machine, the PM bus arbiter and the master control logic. Each of the functional blocks will be discussed in detail.

PCI Master State Machine

This block will performs the handshaking between the PCI interface and the PM internal bus. The PCI master will perform bursting in a linear incrementing type fashion. The PCI master state machine may also wish to provide a target lockout signal. This signal prevents the PCI target interface from responding to any master signals.

PC/PCI Legacy Support

The PCI block supports the PC/PCI sideband signals for legacy support of the soundblaster. The PC/PCI can be enabled by a configuration register bit and one channel selected. The PCI slave block will provide the serial encoded request signal (PCREQ#) in response to a request from the soundblaster and decode the serial encoded PCGNT# line. The PCI slave will then claim I/O writes to address 0000h or 0004h with the PCGNT# line asserted as writes to the SoundBlaster and pass the data to the SoundBlaster.

PCI Target State Machine

The PCI target state machine controls all SSA7785 ThunderBird Avenger™ target responses on the PCI bus in addition to handling the PS internal bus.

PCI Target Control Logic

The target control logic handles the address decoding for the ps_NNNcs# signals, bus command decoding for the ps_XXXrd# and ps_XXXwr# signals, determination of target abort conditions, and data path/pad control logic from the target interface. Also included in this logic are the controls for the PCI datapath and I/O pads. These controls are sent to the datapath logic where they are combined with the master controls and then sent to the datapath and pad devices. The control logic also includes an interface to the PCI configuration headers.

Serial Configuration Port

The Subsystem Vendor ID and Subsystem ID for each of the configuration headers presents a special case. These three 32 bit registers must be programmed by the Subsystem Vendor. It is impractical to hard wire the Subsystem ID registers since each Subsystem Vendor will have a unique ID. Therefore an external serial EEROM device is used to download the proper values into the ID registers after reset and before begin read by the BIOS or other configuration software. The PCI interface should force a retry if any of the subsystem registers have not completed a loading. The Serial Configuration Port is a standard two pin I^2C interface. The ThunderBird Q3DIII will supply the 400 KHz clock to the external serial EEPROM on the CFGCLK pin. The serial data stream will arrive on the CFGDAT input pin. Please refer to a 24LC00 128 bit I^2C Bus Serial EEPROM data sheet for interface protocols and timings.

Serial Configuration Port Programming

The SSA7785 ThunderBird Avenger™ uses an inexpensive external EEPROM, programmed before installation, to download the Subsystem Vendor ID and Subsystem ID registers for each function for a total of 96 bits (six 16 bit registers). The recommended device, a Microchip 24LC01B 1K Bit (128 Byte) Serial EEPROM, can be programmed using a conventional DATA I/O programmer.

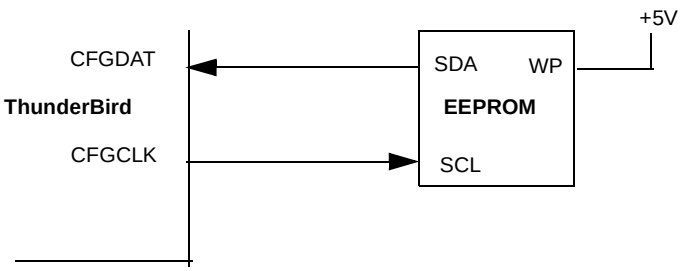


FIGURE 6

In each of the three SSA7785 ThunderBird Avenger™ functions PCI configuration space there is a Subsystem Vendor ID register at an offset of 2Ch and a Subsystem ID register at an offset of 2Eh. Each register is 16 bits in length and is write-only by the serial EEPROM and read-only from the PCI interface. The data from the EEPROM is loaded into the registers immediately after PCI reset. If no EEPROM is detected, the default values are loaded and shown in SSA7785 ThunderBird Avenger™ and reflect the default values for the System ID and Vendor ID for that function.

TABLE 7 Subsystem Register Default Values

Function	Device Type	Offset	Register Name	Default Value
0	Audio Subsystem	2Ch	Subsystem Vendor ID	1004h
0	Audio Subsystem	2Eh	Subsystem ID	0304h
1	Joystick	2Ch	Subsystem Vendor ID	1004h
1	Joystick	2Eh	Subsystem ID	0305h
2	16650 UART	2Ch	Subsystem Vendor ID	1004h
2	16650 UART	2Eh	Subsystem ID	0306h

The EEPROM contains bits 000h through 3FFh. Only bits 000h through 05Fh are utilized to program the Subsystem ID and Subsystem Vendor ID registers. The bit assignments between the EEPROM and the configuration registers are shown in SSA7785 ThunderBird Avenger™.

TABLE 8 EEPROM BIT Assignments to Subsystem Registers

Function 0 - Audio Subsystem				Function 1 - Joystick				Function 2 - 16650 Modem UART			
Subsystem Vendor ID - Offset 2Ch		Subsystem ID - Offset 2Eh		Subsystem Vendor ID - Offset 2Ch		Subsystem ID - Offset 2Eh		Subsystem Vendor ID - Offset 2Ch		Subsystem ID - Offset 2Eh	
EEPROM Bit #	Reg Bit #	EEPROM Bit #	Reg Bit #	EEPROM Bit #	Reg Bit #	EEPROM Bit #	Reg Bit #	EEPROM Bit #	Reg Bit #	EEPROM Bit #	Reg Bit #
000h	15	010h	15	020h	15	030h	15	040h	15	050h	15
001h	14	011h	14	021h	14	031h	14	041h	14	051h	14
002h	13	012h	13	022h	13	032h	13	042h	13	052h	13
003h	12	013h	12	023h	12	033h	12	043h	12	053h	12
004h	11	014h	11	024h	11	034h	11	044h	11	054h	11
005h	10	015h	10	025h	10	035h	10	045h	10	055h	10
006h	9	016h	9	026h	9	036h	9	046h	9	056h	9
007h	8	017h	8	027h	8	037h	8	047h	8	057h	8
008h	7	018h	7	028h	7	038h	7	048h	7	058h	7
009h	6	019h	6	029h	6	039h	6	049h	6	059h	6
00Ah	5	01Ah	5	02Ah	5	03Ah	5	04Ah	5	05Ah	5
00Bh	4	01Bh	4	02Bh	4	03Bh	4	04Bh	4	05Bh	4
00Ch	3	01Ch	3	02Ch	3	03Ch	3	04Ch	3	05Ch	3
00Dh	2	01Dh	2	02Dh	2	03Dh	2	04Dh	2	05Dh	2
00Eh	1	01Eh	1	02Eh	1	03Eh	1	04Eh	1	05Eh	1

Function 0 - Audio Subsystem				Function 1 - Joystick				Function 2 - 16650 Modem UART			
Subsystem Vendor ID - Offset 2Ch		Subsystem ID - Offset 2Eh		Subsystem Vendor ID - Offset 2Ch		Subsystem ID - Offset 2Eh		Subsystem Vendor ID - Offset 2Ch		Subsystem ID - Offset 2Eh	
EEPROM Bit #	Reg Bit #	EEPROM Bit #	Reg Bit #	EEPROM Bit #	Reg Bit #	EEPROM Bit #	Reg Bit #	EEPROM Bit #	Reg Bit #	EEPROM Bit #	Reg Bit #
00Fh	0	01Fh	0	02Fh	0	03Fh	0	04Fh	0	05Fh	0

These bits correspond to Function 0, Subsystem ID (offset 2Eh) bits 2, 1, and 0, respectively. The Vendor should choose and ID that corresponds to the peripherals present and program the EEPROM accordingly.

PCI Datapath

The PCI datapath provides the flip flops to convert the external PCI interface address, data, command and byte enables busses to the internal PM and PS busses.

PCI Configuration Register

Since the SSA7785 ThunderBird Avenger™ is a multi-function device, there are three configuration headers. They are defined as the audio configuration header as function 0, the joystick configuration header as function 1, and the UART configuration header defined as function 2. Each configuration space is divided up into two groups, the registers that stay with the PCI interface and the registers that do not. This section will describe the PCI configuration registers that bunk with the PCI interface. These registers include the PCI standard configuration header registers and the base address registers for various blocks in the SSA7785 ThunderBird Avenger™ chip.

To be more specific, the registers in the offset config space from 00h - 3Fh are the predefined PCI configuration header. All three PCI configuration header registers will reside with the PCI interface. The remainder of the registers are function specific and can be found in the block section itself.

The following sections will detail each of the configuration header spaces for each of the SSA7785 ThunderBird Avenger™ functions: audio, joystick and UART.

PCI Configuration Space 0

The following table is a summary of all the PCI configuration space registers. The registers that are block-mates with the PCI interface (offset 00h - 44h) will be detailed following SSA7785 ThunderBird Avenger™. The remainder of the registers will be detailed with the blocks they control.

TABLE 9 PCI Configuration Space 0 Register Map

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Master Latency Timer	Cache Line Size	0Ch
SONGBASE				10h
SBBASE				14h
MDBASE				18h
ALBASE				1Ch
Reserved				20-2Bh

SUBSYSTEM ID		SUBSYSTEM VENDOR ID		2Ch
Reserved				30-3Bh
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
DMABBASE		DMAABASE		40h
Reserved				44-57h
Reserved	Reserved	Reserved	MSCCFG	58h
Reserved	Reserved	Reserved	ACLCFG0	5Ch
Reserved	Reserved	VRCFG		60h
Reserved	Reserved	Reserved	TIMRCFG0	64h
Reserved	Reserved	HDCFG		68h
Reserved				6Ch
Reserved	Reserved	DMACFG		70h
Reserved				74-77h
Reserved	Reserved	Reserved	DPLLCTL0	78h
Reserved	Reserved	Reserved	DPLLCTL1	7Ch
Reserved	Reserved	Reserved	DPLLCTL2	80h
Reserved				84-87h
Reserved	Reserved	Reserved	TESTCTL0	88h
Reserved				8C-8Fhh
TBLBASE0				90h
TBLBASE1				94h
TBLBASE2				98h
TBLBASE3				9Ch
Reserved	Reserved	Reserved	IRQCTL0	A0h
Reserved	Reserved	Reserved	IRQCTL1	A4h
Reserved	Reserved	Reserved	IRQCTL2	A8h
Reserved	Reserved	Reserved	IRQCTL3	ACh
Reserved	Reserved	Reserved	IRQCTL4	B0h
Reserved	Reserved	Reserved	IRQCTL5	B4h
Reserved	Reserved	Reserved	IRQCTL6	B8h
Reserved	Reserved	Reserved	IRQCTL7	BCh
Reserved	Reserved	Reserved	COMARCH0	C0h
Reserved				C4-EFh
DMAACCNT		DMAACADR		F0h
DMABCCNT		DMABCADR		F4h
DMAMASK	DMACMD	DMAAMODE	Reserved	F8h
Reserved	Reserved	DMABMODE	Reserved	FCh

TABLE 10 Vendor ID Register - VENDOR_ID (RO)

PCI CFG 0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Offset 00h	VENDOR_ID[15:8]							
POR Value	0	0	0	1	0	0	0	0

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	VENDOR_ID[7:0]							
POR Value	0	0	0	0	0	1	0	0

Bit	**Name**	**R/W**	**Function**
15:0	VENDOR_ID	RO	The PCI Vendor ID for Philips Semiconductors (VLSI) is 1004h.

TABLE 11 Device ID Register - DEVICE_ID (RO)

PCI CFG 0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Offset 02h	DEVICE_ID[15:8]							
POR Value	0	0	0	0	0	0	1	1
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	DEVICE_ID[7:0]							
POR Value	0	0	0	0	0	1	0	0

Bit	**Name**	**R/W**	**Function**
15:0	DEVICE_ID	RO	The Device ID for the SSA7785 ThunderBird Avenger™, function 0 is 0304h.

TABLE 12 Command Register - COMMAND (RO/RW)

PCI CFG 0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Offset 04h	R	R	R	R	R	R	FBACK_ ENB	SERR_R ESP
POR Value	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	STEP- PING	PERR_ RESP	SNOOP_ ENB	MEM_ INV_EN	SPEC_ CNTL	MAST_ CNTL	MEM_ CNTL	IO_ CNTL
POR Value	0	0	0	0	0	0	0	0

Bit	**Name**	**R/W**	**Function**
15:10	R	RO	Reserved. These bits always return zero.

Bit	Name	R/W	Function
9	FBACK_ENB	RO	Fast Back-to-Back Enable: the SSA7785 ThunderBird Avenger™, function 0 does not support fast back to back master cycles therefore this bit always returns a zero.
8	SERR_RESP	RW	System Error Response: When set to 1, the SSA7785 ThunderBird Avenger™, function 0 responds to detected PCI bus address parity errors by asserting SERR#. When 0, the SSA7785 ThunderBird Avenger™ ignores these errors.
7	STEPPING	RO	Address / Data Stepping: Always returns 0.
6	PERR_RESP	RW	Parity Error Response: When set to 1, the SSA7785 ThunderBird Avenger™, function 0 responds to detected PCI bus data parity errors by asserting PERR#. When 0, the SSA7785 ThunderBird Avenger™ ignores PCI bus data parity errors.
5	SNOOP_ENB	RO	VGA Snoop Enable. The SSA7785 ThunderBird Avenger™, function 0 does not support VGA snoop enable, therefore this bit always returns a zero.
4	MEM_INV_EN	RO	Memory Write and Invalidate Enable: Always returns 0.
3	SPEC_CNTL	RO	Special Cycle Control: Controls the devices ability to respond to Special Cycle Operations. A value of 0 causes the SSA7785 ThunderBird Avenger™, function 0 to ignore all Special Cycles.
2	MAST_CNTL	RW	Master Control: Controls the devices ability to act as a master on the PCI bus. A value of 0 disables the ability of the SSA7785 ThunderBird Avenger™, function 0, to act as a primary PCI master. A value of 1 enables the ThunderBird Q3DIII, function 0 to become a PCI bus master.
1	MEM_CNTL	RO	Memory Response Control: The SSA7785 ThunderBird Avenger™, function 0 does not support target memory cycles therefore this bit always returns a zero.
0	IO_CNTL	RW	I/O Response Control: Controls the SSA7785 ThunderBird Avenger™, function 0's response to I/O space. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O space accesses.

TABLE 13 Status Register - Status (RO/RW)

PCI CFG 0	D15	D14	D13	D12	D11	D10	D9	D8
Offset 06h	R_PERR	S_SERR	SM_ ABORT	RT_ ABORT	ST_ ABORT	DEVSEL_TMG		S_PERR
POR Value	0	0	0	0	0	0	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
	F_ BK2BK	UDF	MHz66	R	R	R	R	R
POR Value	1	0	0	0	0	0	0	0

Bit	Name	R/W	Function
15	R_PERR	RC	Received Parity Error: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 0 has detected a PCI bus parity error at least once since this bit was last reset.
14	S_SERR	RC	Signalled System Error: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 0 has reported a system error on the SERR# signal at least once since this bit was last reset.
13	SM_ABORT	RC	Signalled Master Abort: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 0 (acting as a master) had to initiate a master abort at least once since this bit was last reset.
12	RT_ABORT	RC	Received Target Abort: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 0 (acting as a master) has received a target abort at least once since this bit was last reset.
11	ST_ABORT	RC	Signalled Target Abort: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 0 has signalled a target abort at least once since this bit was last reset.
10:9	DEVSEL_TMG	RO	DEVSEL Timing: This field indicates the timing of the DEVSEL output (when a PCI master is accessing a SSA7785 ThunderBird Avenger™, function 0 resource). It always returns 01 (Bin). 00 = Fast 01 = Medium (Default Timing) 10 = Slow
8	S_PERR	RC	Signalled Parity Error: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 0 was a bus master for a cycle in which PERR# was activated. This bit cannot be set if the PERR_RESP bit in the command register is not enabled.
7	F_BK2BK	RO	Always returns 1 to indicate support of fast back to back cycles when the SSA7785 ThunderBird Avenger™, function 0 is the target.
6	UDF	RO	User Definable Features. Always returns 0.
5	MHz66	RO	66 MHzMHz Capable. Always returns 0.
4:0	R	RO	Reserved. These bits always return zero.

Note: An RC indicates that this bit can be reset to 0 by writing a 1. Writing a zero leaves this bit unchanged.

TABLE 14 Revision ID Register - REVISION (RO)

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 08h	REVISION_ID[7:0]							
POR Value	0	0	0	1	1	0	0	1

Bit	Name	R/W	Function
7:0	REVISION_ID	RO	The current revision ID for the SSA7785 ThunderBird Avenger™, function 0, the audio subsystem.

TABLE 15 Class Code Register - CLASS (RO)

PCI CFG 0	D23	D22	D21	D20	D19	D18	D17	D16
Offset 09h	BASE_CLASS[7:0]							
POR Value	0	0	0	0	0	1	0	0
	D15	D14	D13	D12	D11	D10	D9	D8
	SUB_CLASS[7:0]							
POR Value	0	0	0	0	0	0	0	1
	D7	D6	D5	D4	D3	D2	D1	D0
	PGM_IFACE[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
23:16	BASE_CLASS	RO	The base class of 04h describes a PCI multimedia device.
15:8	SUB_CLASS	RO	The sub class of 01h describes a PCI audio multimedia device.
7:0	PGM_IFACE	RO	Device generic function identification.

TABLE 16 CACHELINE Size Register - CACHELINE (RO)

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Ch	CACHELINE[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	CACHELINE	RO	Reserved for cache line size indicator.

TABLE 17 Master Latency Timer Register - LATIME (RW)

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Dh	LATIME[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	LATIME	RW	The primary bus latency timer specifies the number of primary clocks that the primary master may consume. The timer is reloaded at each assertion of FRAME# by the primary master. If the primary master loses its bus grant, then it must relinquish the bus after the timer expires.

TABLE 18 Header Type Register - HEADER (RO)

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Eh	MULTI_FN	HEADER[6:0]						
POR Value	1	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7	MULTI_FN	RO	A 1 indicates that the SSA7785 ThunderBird Avenger™ is a multi-function device. The three PCI configuration headers are accessed by the configuration cycle address bits 10-8. The function definitions are as follows: 0 = Audio Subsystem 1 = Joystick 2 = 16650 UART
6:0	HEADER	RO	Header Type. A 00h indicates this device is a not a PCI-to-PCI bridge.

TABLE 19 BIST Register - BIST (RO)

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Fh	BIST	START	R	R	CODE[3:0]			
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7	BIST	RO	BIST capable. BIST is not supported in the SSA7785 ThunderBird Avenger™, function 0 at this revision. It may be desired to include a BIST test for the DSP at a later time.

Bit	Name	R/W	Function
6	START	RO	If BIST capable, this bit will start the BIST. Writing a 1 will start the test and the BIST should write this bit to a zero when complete. Software should fail the device if the BIST is not complete after 2 seconds.
5:4	R	RO	Reserved. These bits always return zero.
3:0	CODE	RO	Completion Code. A value of zero means the device has passed its test. Non-zero values means the device has failed using device specific failure codes.

SSA7785 ThunderBird Avenger™ CFG Space 0 Non-Legacy Base Address Registers

The Thunderbird Base Address Register (SONGBASE) is used to I/O map all of the non-legacy I/O devices in the SSA7785 ThunderBird Avenger™ chip. The SONGBASE register maps the two DMA channels, the AC Link registers, the Host/DSP interface, the Serial Port interfaces, and the Multimedia Timer. The offset index for each of the devices are shown below: SSA7785 ThunderBird Avenger™ Non-Legacy I/O Device Map

Device Name	Byte 3	Byte 2	Byte 1	Byte 0	Offset
Multimedia Timer	TMCOUNT2	TMCOUNT1	TMCOUNT0	TMSTAT	00h
	Reserved	Reserved	Reserved	Reserved	04h
	Reserved	Reserved	Reserved	Reserved	08h
	Reserved	Reserved	Reserved	Reserved	0Ch
Serial Ports	Reserved		Reserved		10h
	Reserved		Reserved		14h
	Reserved		Reserved		18h
	Reserved		Reserved		1Ch
Host/DSP Interface	HDPCTL		HDDATA		20h
	HDDLA		HDPSTT		24h
	Reserved		HDDLD		28h
	Reserved		Reserved		2Ch
AC Link Interface	ACDATA		ACADDR		30h
	ACSTAT		ACCTRL		34h
	ACPCML				38h
	ACPCMR				3Ch
Serial IRQ	Reserved	Reserved	Reserved	IRQCTL	40h
Thunderbird Reserved	Reserved				44-7Fh

TABLE 20 ThunderBird Base Address Register - Songbase (RW/RO)

PCI CFG 0	D31	D30	D29	D28	D27	D26	D25	D24
Offset 10h	SONGBASE[31:24]							
POR Value	0	0	0	0	0	0	0	0

	D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
	SONGBASE[23:16]							
POR Value	0	0	0	0	0	0	0	0
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
	SONGBASE[15:8]							
POR Value	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SONG BASE[7]	R	R	R	R	R	R	IO
POR Value	0	0	0	0	0	0	0	1

Bit	Name	R/W	Function
31:7	SONGBASE	RW	Thunderbird non-legacy device base address register. This register supplies the I/O base address for the non-legacy I/O devices within the SSA7785 ThunderBird Avenger™ chip.
6:1	R	RO	Reserved. These bits are reserved a must always return a zero for plug and play.
0	IO	RO	I/O flag. This read only bit indicates that this is an I/O range.

SSA7785 ThunderBird Avenger™ CFG Space 0 Legacy Base Address Registers

The SSA7785 ThunderBird Avenger™ contains three legacy I/O base registers in configuration space 0. These legacy devices are the Sound Blaster register, the AdLib registers and the MIDI interface registers. They are described in detail in the next three tables.

TABLE 21 Sound Blaster Base Address- SBBASE (RW/RO)

PCI CFG 0	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**
Offset 14h	SBBASE[31:24]							
POR Value	0	0	0	0	0	0	0	0
	D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
	SBBASE[23:16]							
POR Value	0	0	0	0	0	0	0	0

	D15	D14	D13	D12	D11	D10	D9	D8
	SBBASE[15:8]							
POR Value	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SBBASE[7:4]				R	R	R	IO
POR Value	0	0	0	0	0	0	0	1

Bit	Name	R/W	Function
31:4	SBBASE	RW	Sound Blaster programmable base address. The address should be on a 16 byte boundary. For reference, the Sound Blaster legacy base addresses are 220h and 240h. Note that accesses from the AdLib base address are mapped into a subset of the SoundBlaster registers.
3:1	R	RO	Reserved. These bits are reserved and always return zeros for plug and play.
0	IO	RO	I/O flag. This read only bit indicates that this is an I/O range.

TABLE 22 MIDI Base Address- MDBASE (RW/RO)

PCI CFG 0	D31	D30	D29	D28	D27	D26	D25	D24
Offset 18h	MDBASE[31:24]							
POR Value	0	0	0	0	0	0	0	0
	D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
	MDBASE[23:16]							
POR Value	0	0	0	0	0	0	0	0
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
	MDBASE[15:8]							
POR Value	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	MDBASE[7:2]						R	IO
POR Value	0	0	0	0	0	0	0	1

Bit	Name	R/W	Function
31:2	MDBASE	RW	MIDI port programmable base address. The address should be on a double word boundary. For reference the MIDI port legacy base addresses are 220h, 230h, 240h, 250h, 300h, 320h, 330h, 332h, 334h, 336h, 340h, and 360h.
1	R	RO	Reserved. This bit is reserved a must always return a zero for plug and play.
0	IO	RO	I/O flag. This read only bit indicates that this is an I/O range.

TABLE 23 ADLIB Base Address Register - ALBASE (RW/RO)

PCI CFG 0	D31	D30	D29	D28	D27	D26	D25	D24
Offset 1Ch	ALBASE[31:24]							
POR Value	0	0	0	0	0	0	0	0
	D23	D22	D21	D20	D19	D18	D17	D16
	ALBASE[23:16]							
POR Value	0	0	0	0	0	0	0	0
	D15	D14	D13	D12	D11	D10	D9	D8
	ALBASE[15:8]							
POR Value	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	ALBASE[7:3]					R	R	IO
POR Value	0	0	0	0	0	0	0	1

Bit	Name	R/W	Function
31:3	ALBASE	RW	AdLib registers programmable base address. The address should be on a quad word (64 bit) boundary. For reference, the AdLib legacy base address is at 388h and maps into a subset of the Sound Blaster registers.
2:1	R	RO	Reserved. These bits are reserved and always return zeros for plug and play.
0	IO	RO	I/O flag. This read only bit indicates that this is an I/O range.

TABLE 24 Subsystem Vendor ID - SUBVENID (RO)

PCI CFG 0	D15	D14	D13	D12	D11	D10	D9	D8
Offset 2Ch	SUBVEN_ID[15:8]							

POR Value	0	0	0	1	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SUBVEN_ID[7:0]							
POR Value	0	0	0	0	0	1	0	0

Bit	Name	R/W	Function
15:0	SUBVEN_ID	RO	Subsystem Vendor ID. The Subsystem Vendor ID register allows the manufacturer to uniquely identify their board since more than one board OEM may use the SSA7785 ThunderBird Avenger™ chip. The Subsystem Vendor ID register is loaded by an external EEPROM via the Serial Configuration Port after reset and before any access to the PCI configuration header. The PCI target logic should force a retry if the Subsystem Vendor ID register has not completed loading. The Subsystem Vendor ID is read only to the PCI interface. If no external EEPROM is present, then the default Subsystem Vendor ID is 1004h, that of Philips Semiconductors (VLSI).

TABLE 25 Subsystem ID - SUBSYSID (RO)

PCI CFG 0	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Offset 2Eh	SUBSYS_ID[15:8]							
POR Value	0	0	0	0	0	0	1	1
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SUBSYS_ID[7:0]							
POR Value	0	0	0	0	0	1	0	0

Bit	Name	R/W	Function
15:0	SUBSYS_ID	RO	Subsystem ID. The Subsystem ID register allows the manufacturer to uniquely identify their board since more than one board OEM may use the SSA7785 ThunderBird Avenger™ chip. The Subsystem ID register is loaded by an external EEPROM via the Serial Configuration Port after reset and before any access to the PCI configuration header. The PCI target logic should force a retry if the Subsystem ID register has not completed loading. The Subsystem ID is read only to the PCI interface. If no external EEPROM is present, then the default Subsystem ID is 0304h, identical to the SSA7785 ThunderBird Avenger™ function 0 Device ID.

TABLE 26 Interrupt Line Register - INTLINE (RW)

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Ch	INTLINE[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	INTLINE	RW	Interrupt Line. The Interrupt Line register is an eight bit register used to communicate interrupt line routing information. The value in this register tells which input of the system interrupt controller(s) the SSA7785 ThunderBird Avenger™ Device's interrupt pin is connected to. If serial interrupts are enabled (COMARCH0 Register IRQSER=1) then the INT_LINE register will be read only and will have the value of all 1's. If Serial Interrupts are disabled (IRQSER=0) then the INT_LINE register will be readable/writable.

TABLE 27 Interrupt Pin Register - INTPIN (RO)

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Dh	INTPIN[7:0]							
POR Value	0	0	0	0	0	0	0	1

Bit	Name	R/W	Function
7:0	INTPIN	RO	Interrupt Pin. The interrupt pin register tells which interrupt the SSA7785 ThunderBird Avenger™ device uses. If serial interrupts are enabled (COMARCH0 Register IRQSER=1) then the INT_PIN register will have the read only value of all 0's implying that the SSA7785 ThunderBird Avenger™ device does not use any of the PCI Interrupt pins. If Serial Interrupts are disabled (IRQSER=0) then the INT_PIN register will have the read only value of 01h implying that the SSA7785 ThunderBird Avenger™ device uses INT A interrupt pin.

TABLE 28 MIN_GNT Register - MINGNT (RO)

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Eh	MINGNT[7:0]							
POR Value	0	0	0	0	1	0	0	1

Bit	Name	R/W	Function
7:0	MINGNT	RO	Minimum grant specifies how long of a burst period the device needs assuming a clock speed of 33MHz. Since the SSA7785 ThunderBird Avenger™, function 0, will burst a maximum of 64 double words, therefore requiring about 75 33MHz clocks or 2.25 microseconds. The time units specified are in 0.25 microsecond increments.

TABLE 29 MAX_LAT Register - MAXLAT (RO)

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Fh	MAXLAT[7:0]							
POR Value	0	0	1	0	1	0	0	0

Bit	Name	R/W	Function
7:0	MAXLAT	RO	Maximum latency specifies how often a device needs to gain access to the PCI bus. The SSA7785 ThunderBird Avenger™, function 0, should only request the bus a a maximum of every 10 microseconds. The MAXLAT value is computed using the same parameters as the MINGNT.

SSA7785 ThunderBird Avenger™ CFG Space 0 DMA Base Registers

This section will describe the PCI configuration registers that provide functions such as base address remapping and the like. These registers reside within the PCI interface.

TABLE 30 DMA Channel A Base Address Register - DMAABASE (RW)

PCI CFG 0	D15	D14	D13	D12	D11	D10	D9	D8
Offset 40h	DMAABASE[15:8]							
POR Value	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	DMAA BASE[7]	R	DMAABASE[5:4]		R	XFRSIZ[1:0]		DDMAA EN
POR Value	0	0	0	0	0	1	0	0

Bit	Name	R/W	Function
15:7	DMAABASE	RW	DMA channel A programmable base address, bits 15:7.
6	R	RO	Reserved. This bit must always be zero.

Bit	Name	R/W	Function
5:4	DMAABASE	RW	DMA channel A programmable base address, bits 5:4. These bits select a channel number for this channel. In LAM DMAABASE[5:4] select the channel number that this DMA represents, it should be different than DMAB-BASE[5:4].
3	R	RO	Reserved. This bit must always be zero.
2:1	XFRSIZ	RW	DMA transfer size. 00 = reserved 10 = double word 11 = reserved 01 = reserved
0	DDMAAEN	RW	DDMA channel A enable. This DDMA channel is enabled when this bit is set to a one.

TABLE 31 DMA Channel B Base Address Register - DMABBASE (RW)

PCI CFG 0	D31	D30	D29	D28	D27	D26	D25	D24
Offset 42h	DMABBASE[15:8]							
POR Value	0	0	0	0	0	0	0	0
	D23	D22	D21	D20	D19	D18	D17	D16
	DMAB BASE[7]	R	DMABBASE[5:4]		R	R	R	DDMAB EN
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
15:7	DMABBASE	RW	DMA channel B programmable base address. Normally this base is set the same as DMA channel A except for DMABBASE[5:4] which select the channel number. This is a requirement of some PC chipsets, future chipsets may eliminate this requirement. In LAM DMABBASE[5:4] select the channel number that this DMA represents, it should be different than DMAABASE[5:4].
6	R	RO	Reserved. This bit must always be zero.
5:4	DMABBASE	RW	DMA channel B programmable base address, bits 5:4. These bits select a channel number for this channel. In LAM DMABBASE[5:4] select the channel number that this DMA represents, it should be different than DMAA-BASE[5:4].
3:1	R	RO	Reserved. These bits must always be zeros.
0	DDMABEN	RW	DMA channel B enable. This DDMA channel is enabled when this bit is set to a one.

TABLE 32 Miscellaneous Configuration Register - MSCCFG (RO/RW)

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 58h	ASYMCLK[1:0]		RDY_EN	CFGCLK	BHEN	PCCH[1:0]		PCPCI_EN
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:6	ASYMCLK	RW	Asymmetrical Clock Select. These bits program the duty cycle for the input for the two phase DSP clock generator.
5	RDY_EN	RW	Music registers ready enable. When set, the music registers will cause the PCI interface to retry when either of the music registers (music0 or music1) are full.
4	CFGCLK	RW	Serial Configuration Port Clock Select. This bit selects the clock output to the Configuration Serial Port. 0 = Ouput a 400 KHz clock. Incoming data will be synchronized to this clock. 1 = Output the PCI clock.
3	BHEN	RW	Bus Hog Fix Enable.
2:1	PCCH	RW	These two bits are the encoded channel number that the soundblaster will be on in the PC/PCI mode and are valid only when the PC/PCI mode is enabled.
0	PCPCI_EN	RW	PC/PCI mode enable bit. This bit, when set = 1, will enable the PC/PCI side-band signals for the Soundblaster legacy mode.

PCI Configuration Space 1

The following table is a summary of all the PCI configuration space registers. The registers that are block-mates with the PCI interface (offset 00h - 3Ch) will be detailed following SSA7785 ThunderBird Avenger™. The remainder of the registers will be detailed with the blocks they control. This register space is for the joystick.

TABLE 33 PCI Configuration Space 1 Register Map

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Master Latency Timer	Cache Line Size	0Ch
GMBASE				10h
Reserved				14-2B
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30-3Bh
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Reserved				40-6Bh

Reserved	Reserved	Reserved	GAMECFG0	6Ch
Reserved				70-FFh

TABLE 34 Vendor ID Register - VENDOR_ID (RO)

PCI CFG 1	D15	D14	D13	D12	D11	D10	D9	D8
Offset 00h	VENDOR_ID[15:8]							
POR Value	0	0	0	1	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	VENDOR_ID[7:0]							
POR Value	0	0	0	0	0	1	0	0

Bit	Name	R/W	Function
15:0	VENDOR_ID	RO	The PCI Vendor ID for Philips Semiconductors (VLSI) is 1004h.

TABLE 35 Device ID Register - DEVICE_ID (RO)

PCI CFG 1	D15	D14	D13	D12	D11	D10	D9	D8
Offset 02h	DEVICE_ID[15:8]							
POR Value	0	0	0	0	0	0	1	1
	D7	D6	D5	D4	D3	D2	D1	D0
	DEVICE_ID[7:0]							
POR Value	0	0	0	0	0	1	0	1

Bit	Name	R/W	Function
15:0	DEVICE_ID	RO	The Device ID for the SSA7785 ThunderBird Avenger™, function 1 is 0305h.

TABLE 36 Command Register - COMMAND (RO/RW)

PCI CFG 1	D15	D14	D13	D12	D11	D10	D9	D8
Offset 04h	R	R	R	R	R	R	FBACK_ENB	SERR_RESP
POR Value	0	0	0	0	0	0	0	0

	D7	D6	D5	D4	D3	D2	D1	D0
	STEP-PING	PERR_ RESP	SNOOP_ ENB	MEM_ INV_EN	SPEC_ CNTL	MAST_ CNTL	MEM_ CNTL	IO_ CNTL
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
15:10	R	RO	Reserved. These bits always return zero.
9	FBACK_ENB	RO	Fast Back-to-Back Enable: the SSA7785 ThunderBird Avenger™, function 1 does not support fast back to back master cycles therefore this bit always returns a zero.
8	SERR_RESP	RW	System Error Response: When set to 1, the SSA7785 ThunderBird Avenger™, function 1 responds to detected PCI bus address parity errors by asserting SERR#. When 0, the SSA7785 ThunderBird Avenger™ ignores these errors.
7	STEPPING	RO	Address / Data Stepping: Always returns 0.
6	PERR_RESP	RW	Parity Error Response: When set to 1, the SSA7785 ThunderBird Avenger™, function 1 responds to detected PCI bus data parity errors by asserting PERR#. When 0, the SSA7785 ThunderBird Avenger™ ignores PCI bus data parity errors.
5	SNOOP_ENB	RO	VGA Snoop Enable. The SSA7785 ThunderBird Avenger™, function 1 does not support VGA snoop enable, therefor this bit always returns a zero.
4	MEM_INV_EN	RO	Memory Write and Invalidate Enable: Always returns 0.
3	SPEC_CNTL	RO	Special Cycle Control: Controls the devices ability to respond to Special Cycle Operations. A value of 0 causes the SSA7785 ThunderBird Avenger™, function 1 to ignore all Special Cycles.
2	MAST_CNTL	RO	Master Control: The SSA7785 ThunderBird Avenger™, function 1 does not have any master functions.
1	MEM_CNTL	RO	Memory Response Control: The SSA7785 ThunderBird Avenger™, function 1 does not support target memory cycles therefore this bit always returns a zero.
0	IO_CNTL	RW	I/O Response Control: Controls the SSA7785 ThunderBird Avenger™, function 1's response to I/O space. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O space accesses.

TABLE 37 Status Register - STATUS (RO/RW)

PCI CFG 1	D15	D14	D13	D12	D11	D10	D9	D8
Offset 06h	R_PERR	S_SERR	SM_ ABORT	RT_ ABORT	ST_ ABORT	DEVSEL_TMG		S_PERR
POR Value	0	0	0	0	0	0	1	0

	D7	D6	D5	D4	D3	D2	D1	D0
	F_ BK2BK	UDF	MHz66	R	R	R	R	R
POR Value	1	0	0	0	0	0	0	0

Bit	Name	R/W	Function
15	R_PERR	RC	Received Parity Error: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 1 has detected a PCI bus parity error at least once since this bit was last reset.
14	S_SERR	RC	Signalled System Error: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 1 has reported a system error on the SERR# signal at least once since this bit was last reset.
13	SM_ABORT	RO	Signalled Master Abort: The SSA7785 ThunderBird Avenger™, function 1, does not act as a master.
12	RT_ABORT	RO	Received Target Abort: The SSA7785 ThunderBird Avenger™, function 1 does not act as a master.
11	ST_ABORT	RC	Signalled Target Abort: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 1 has signalled a target abort at least once since this bit was last reset.
10:9	DEVSEL_TMG	RO	DEVSEL Timing: This field indicates the timing of the DEVSEL output (when a PCI master is accessing a SSA7785 ThunderBird Avenger™, function 1 resource). It always returns 01 (Bin). 00 = Fast 01 = Medium (Default Timing) 10 = Slow
8	S_PERR	RO	Signalled Parity Error: The SSA7785 ThunderBird Avenger™, function 1, does not act as a bus master.
7	F_BK2BK	RO	Always returns 1 to indicate support of fast back to back cycles when the SSA7785 ThunderBird Avenger™, function 1 is the target.
6	UDF	RO	User Definable Features. Always returns 0.
5	MHz66	RO	66 MHz Capable. Always returns 0.
4:0	R	RO	Reserved. These bits always return zero.

Note: An RC indicates that this bit can be reset to 0 by writing a 1. Writing a zero leaves this bit unchanged.

TABLE 38 Revision ID Register - REVISION (RO)

PCI CFG 1	D7	D6	D5	D4	D3	D2	D1	D0
Offset 08h	REVISION_ID[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	REVISION_ID	RO	The current revision ID for the SSA7785 ThunderBird Avenger™ joystick.

TABLE 39 Class Code Register - CLASS (RO)

PCI CFG 1	D23	D22	D21	D20	D19	D18	D17	D16
Offset 09h	BASE_CLASS[7:0]							
POR Value	0	0	0	0	1	0	0	1
	D15	D14	D13	D12	D11	D10	D9	D8
	SUB_CLASS[7:0]							
POR Value	1	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	PGM_IFACE[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
23:16	BASE_CLASS	RO	The base class of 09h describes an input device.
15:8	SUB_CLASS	RO	The sub class of 80h describes a “other” input controller.
7:0	PGM_IFACE	RO	Device generic function identification.

TABLE 40 CACHELINE Size Register - CACHELINE (RO)

PCI CFG 1	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Ch	CACHELINE[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	CACHELINE	RO	Reserved for cache line size indicator.

TABLE 41 Master Latency Timer Register - LATIME (RW)

PCI CFG 1	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Dh	LATIME[7:0]							

PCI CFG 1	D7	D6	D5	D4	D3	D2	D1	D0
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	LATIME	RO	The primary bus latency timer specifies the number of primary clocks that the primary master may consume. It is set to zero since the joystick is a target only.

TABLE 42 Header Type Register - HEADER (RO)

PCI CFG 1	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Eh	MULTI_FN	HEADER[6:0]						
POR Value	1	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7	MULTI_FN	RO	For the SSA7785 ThunderBird Avenger™, function 1, this bit has no meaning.
6:0	HEADER	RO	Header Type. A 00h indicates this device is not a PCI-to-PCI bridge.

TABLE 43 BIST Register - BIST (RO)

PCI CFG 1	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Fh	BIST	START	R	R	CODE[3:0]			
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7	BIST	RO	BIST capable. BIST is not supported in the SSA7785 ThunderBird Avenger™, function 1 at this revision.
6	START	RO	If BIST capable, this bit will start the BIST. Writing a 1 will start the test and the BIST should write this bit to a zero when complete. Software should fail the device if the BIST is not complete after 2 seconds.
5:4	R	RO	Reserved. These bits always return zero.
3:0	CODE	RO	Completion Code. A value of zero means the device has passed its test. Non-zero values means the device has failed using device specific failure codes.

SSA7785 ThunderBird Avenger™ CFG Space 1 Legacy Base Address Registers

The SSA7785 ThunderBird Avenger™, contains one legacy I/O base registers in configuration space 1. The joystick is the sole legacy I/O base address register and is documented here.

TABLE 44 Game Port(JOYSTICK) Base Address - GMBASE (RW/RO)

PCI CFG 1	D31	D30	D29	D28	D27	D26	D25	D24
Offset 10h	GMBASE[31:24]							
POR Value	0	0	0	0	0	0	0	0
	D23	D22	D21	D20	D19	D18	D17	D16
	GMBASE[23:16]							
POR Value	0	0	0	0	0	0	0	0
	D15	D14	D13	D12	D11	D10	D9	D8
	GMBASE[15:8]							
POR Value	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	GMBASE[7:3]					R	R	IO
POR Value	0	0	0	0	0	0	0	1

Bit	Name	R/W	Function
31:3	GMBASE	RW	Game port programmable base address. The address should be on a 8 byte boundary. For reference, the game port legacy base address is 201h.
2:1	R	RO	Reserved. These bits are reserved and always return zeros for plug and play.
0	IO	RO	I/O flag. This read only bit indicates that this is an I/O range.

TABLE 45 Subsystem Vendor ID - SUBVENID (RO)

PCI CFG 1	D15	D14	D13	D12	D11	D10	D9	D8
Offset 2Ch	SUBVEN_ID[15:8]							
POR Value	0	0	0	1	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	SUBVEN_ID[7:0]							
POR Value	0	0	0	0	0	1	0	0

Bit	Name	R/W	Function
15:0	SUBVEN_ID	RO	Subsystem Vendor ID. The Subsystem Vendor ID register allows the manufacturer to uniquely identify their board since more than one board OEM may use the SSA7785 ThunderBird Avenger™ chip. The Subsystem Vendor ID register is loaded by an external EEPROM via the Serial Configuration Port after reset and before any access to the PCI configuration header. The PCI target logic should force a retry if the Subsystem Vendor ID register has not completed loading. The Subsystem Vendor ID is read only to the PCI interface. If no external EEPROM is present, then the default Subsystem Vendor ID is 1004h, that of Philips Semiconductors (VLSI).

TABLE 46 Subsystem ID - SUBSYSID (RO)

PCI CFG 1	D15	D14	D13	D12	D11	D10	D9	D8
Offset 2Eh	SUBSYS_ID[15:8]							
POR Value	0	0	0	0	0	0	1	1
	D7	D6	D5	D4	D3	D2	D1	D0
	SUBSYS_ID[7:0]							
POR Value	0	0	0	0	0	1	0	1

Bit	Name	R/W	Function
15:0	SUBSYS_ID	RO	Subsystem ID. The Subsystem ID register allows the manufacturer to uniquely identify their board since more than one board OEM may use the SSA7785 ThunderBird Avenger™ chip. The Subsystem ID register is loaded by an external EEPROM via the Serial Configuration Port after reset and before any access to the PCI configuration header. The PCI target logic should force a retry if the Subsystem ID register has not completed loading. The Subsystem ID is read only to the PCI interface. If no external EEPROM is present, then the default Subsystem ID is 0305h, identical to the SSA7785 ThunderBird Avenger™ function 1 Device ID.

TABLE 47 Interrupt Line Register - INTLINE (RO)

PCI CFG 1	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Ch	INTLINE[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	INTLINE	RO	Interrupt Line. The Interrupt Line register is an eight bit register used to communicate interrupt line routing information. The value in this register tells which input of the system interrupt controller(s) the SSA7785 ThunderBird Avenger™ Device's interrupt pin is connected to. It is set to 00h to use function 0's interrupt line. There is no legacy interrupt support for function 1.

TABLE 48 Interrupt Pin Register - INTPIN (RO)

PCI CFG 1	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Dh	INTPIN[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	INTPIN	RO	Interrupt Pin. The interrupt pin register tells which interrupt the SSA7785 ThunderBird Avenger™ device uses. The read only value of 00h implies that the SSA7785 ThunderBird Avenger™ device shares the INT A interrupt pin with function 0. There is no legacy interrupt support for function 1.

TABLE 49 MIN_GNT Register - MINGNT (RO)

PCI CFG 1	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Eh	MINGNT[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	MINGNT	RO	Minimum grant specifies how long of a burst period the device needs assuming a clock speed of 33MHz. Since the SSA7785 ThunderBird Avenger™, function 1, is a target only, this register is read only and set to zero.

TABLE 50 MAX_LAT Register - MAXLAT (RO)

PCI CFG 1	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Fh	MAXLAT[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	MAXLAT	RO	Maximum latency specifies how often a device needs to gain access to the PCI bus. The SSA7785 ThunderBird Avenger™, function 1, is a target only, this register is read only and set to zero.

PCI Configuration Space 2

The following table is a summary of all the PCI configuration space registers. The registers that are block-mates with the PCI interface (offset 00h - 3Ch) will be detailed following SSA7785 ThunderBird Avenger™. The remainder of the registers will be detailed with the blocks they control. This register space is for the 16650 UART.

TABLE 51 PCI Configuration Space 2 Register Map

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Master Latency Timer	Cache Line Size	0Ch
UARTBASE				10-13h
Reserved				14-2B
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30-3Bh
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Reserved	Reserved	Reserved	UARTCFG0	40h
Reserved	Reserved	Reserved	SFCR	44h
Reserved				48-FFh

TABLE 52 Vendor ID Register - VENDOR_ID (RO)

PCI CFG 2	D15	D14	D13	D12	D11	D10	D9	D8
Offset 00h	VENDOR_ID[15:8]							
POR Value	0	0	0	1	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	VENDOR_ID[7:0]							
POR Value	0	0	0	0	0	1	0	0

Bit	Name	R/W	Function
15:0	VENDOR_ID	RO	The PCI Vendor ID for Philips Semiconductors (VLSI) is 1004h.

TABLE 53 Device ID Register - DEVICE_ID (RO)

PCI CFG 2	D15	D14	D13	D12	D11	D10	D9	D8
Offset 02h	DEVICE_ID[15:8]							
POR Value	0	0	0	0	0	0	1	1
	D7	D6	D5	D4	D3	D2	D1	D0
	DEVICE_ID[7:0]							
POR Value	0	0	0	0	0	1	1	0

Bit	Name	R/W	Function
15:0	DEVICE_ID	RO	The Device ID for the SSA7785 ThunderBird Avenger™, function 2 is 0306h.

TABLE 54 Command Register - COMMAND (RO/RW)

PCI CFG 2	D15	D14	D13	D12	D11	D10	D9	D8
Offset 04h	R	R	R	R	R	R	FBACK_ ENB	SERR_R ESP
POR Value	0	0	0	0	0	0	0	0
	D7	D6	D5	D4	D3	D2	D1	D0
	STEP- PING	PERR_ RESP	SNOOP_ ENB	MEM_ INV_EN	SPEC_ CNTL	MAST_ CNTL	MEM_ CNTL	IO_ CNTL
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
15:10	R	RO	Reserved. These bits always return zero.
9	FBACK_ENB	RO	Fast Back-to-Back Enable: the SSA7785 ThunderBird Avenger™, function 2 does not support fast back to back master cycles therefore this bit always returns a zero.
8	SERR_RESP	RW	System Error Response: When set to 1, the SSA7785 ThunderBird Avenger™, function 2 responds to detected PCI bus address parity errors by asserting SERR#. When 0, the SSA7785 ThunderBird Avenger™ ignores these errors.
7	STEPPING	RO	Address / Data Stepping: Always returns 0.
6	PERR_RESP	RW	Parity Error Response: When set to 1, the SSA7785 ThunderBird Avenger™, function 2 responds to detected PCI bus data parity errors by asserting PERR#. When 0, the SSA7785 ThunderBird Avenger™ ignores PCI bus data parity errors.

Bit	Name	R/W	Function
5	SNOOP_ENB	RO	VGA Snoop Enable. The SSA7785 ThunderBird Avenger™, function 2 does not support VGA snoop enable, therefor this bit always returns a zero.
4	MEM_INV_EN	RO	Memory Write and Invalidate Enable: Always returns 0.
3	SPEC_CNTL	RO	Special Cycle Control: Controls the devices ability to respond to Special Cycle Operations. A value of 0 causes the SSA7785 ThunderBird Avenger™, function 2 to ignore all Special Cycles.
2	MAST_CNTL	RO	Master Control: The SSA7785 ThunderBird Avenger™, function 2 does not have any master functions.
1	MEM_CNTL	RO	Memory Response Control: The SSA7785 ThunderBird Avenger™, function 2 does not support target memory cycles therefore this bit always returns a zero.
0	IO_CNTL	RW	I/O Response Control: Controls the SSA7785 ThunderBird Avenger™, function 2's response to I/O space. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O space accesses.

TABLE 55 Status Register - STATUS (RO/RW)

PCI CFG 2	D15	D14	D13	D12	D11	D10	D9	D8
Offset 06h	R_PERR	S_SERR	SM_ ABORT	RT_ ABORT	ST_ ABORT	DEVSEL_TMG		S_PERR
POR Value	0	0	0	0	0	0	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
	F_ BK2BK	UDF	MHz66	R	R	R	R	R
POR Value	1	0	0	0	0	0	0	0

Bit	Name	R/W	Function
15	R_PERR	RC	Received Parity Error: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 2 has detected a PCI bus parity error at least once since this bit was last reset.
14	S_SERR	RC	Signalled System Error: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 2 has reported a system error on the SERR# signal at least once since this bit was last reset.
13	SM_ABORT	RO	Signalled Master Abort: The SSA7785 ThunderBird Avenger™, function 2, does not act as a master.
12	RT_ABORT	RO	Received Target Abort: The SSA7785 ThunderBird Avenger™, function 2 does not act as a master.

Bit	Name	R/W	Function
11	ST_ABORT	RC	Signalled Target Abort: When set to 1, this bit indicates that the SSA7785 ThunderBird Avenger™, function 2 has signalled a target abort at least once since this bit was last reset.
10:9	DEVSEL_TMG	RO	DEVSEL Timing: This field indicates the timing of the DEVSEL output (when a PCI master is accessing a SSA7785 ThunderBird Avenger™ resource). It always returns 01 (Bin). 00 = Fast 01 = Medium (Default Timing) 10 = Slow
8	S_PERR	RO	Signalled Parity Error: The SSA7785 ThunderBird Avenger™, function 2, does not act as a bus master.
7	F_BK2BK	RO	Always returns 1 to indicate support of fast back to back cycles when the SSA7785 ThunderBird Avenger™, function 2 is the target.
6	UDF	RO	User Definable Features. Always returns 0.
5	MHz66	RO	66 MHz Capable. Always returns 0.
4:0	R	RO	Reserved. These bits always return zero.

Note: An RC indicates that this bit can be reset to 0 by writing a 1. Writing a zero leaves this bit unchanged.

TABLE 56 Revision ID Register - REVISION (RO)

PCI CFG 2	D7	D6	D5	D4	D3	D2	D1	D0
Offset 08h	REVISION_ID[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	REVISION_ID	RO	The current revision ID for the SSA7785 ThunderBird Avenger™, function 2 joystick..

TABLE 57 Class Code Register - CLASS (RO)

PCI CFG 2	D23	D22	D21	D20	D19	D18	D17	D16
Offset 09h	BASE_CLASS[7:0]							
POR Value	0	0	0	0	0	1	1	1
	D15	D14	D13	D12	D11	D10	D9	D8
	SUB_CLASS[7:0]							
POR Value	0	0	0	0	0	0	0	0

PCI CFG 2	D23	D22	D21	D20	D19	D18	D17	D16
	D7	D6	D5	D4	D3	D2	D1	D0
	PGM_IFACE[7:0]							
POR Value	0	0	0	0	0	0	1	0

Bit	Name	R/W	Function
23:16	BASE_CLASS	RO	The base class of 07h describes simple communication devices.
15:8	SUB_CLASS	RO	The sub class of 00h describes serial controllers.
7:0	PGM_IFACE	RO	The interface of 02h details a 16550 compatible serial controller.

TABLE 58 CACHELINE Size Register - CACHELINE (RO)

PCI CFG 2	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Ch	CACHELINE[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	CACHELINE	RO	Reserved for cache line size indicator.

TABLE 59 Master Latency Timer Register - LATIME (RW)

PCI CFG 2	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Dh	LATIME[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	LATIME	RO	The primary bus latency timer specifies the number of primary clocks that the primary master may consume. It is set to zero since the 16650 UART is a target only.

TABLE 60 Header Type Register - HEADER (RO)

PCI CFG 2	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Eh	MULTI_FN	HEADER[6:0]						
POR Value	1	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7	MULTI_FN	RO	For the SSA7785 ThunderBird Avenger™, function 2, this bit has no meaning.
6:0	HEADER	RO	Header Type. A 00h indicates this device is not a PCI-to-PCI bridge.

TABLE 61 BIST Register - BIST (RO)

PCI CFG 2	D7	D6	D5	D4	D3	D2	D1	D0
Offset 0Fh	BIST	START	R	R	CODE[3:0]			
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7	BIST	RO	BIST capable. BIST is not supported in the SSA7785 ThunderBird Avenger™, function 2 at this revision.
6	START	RO	If BIST capable, this bit will start the BIST. Writing a 1 will start the test and the BIST should write this bit to a zero when complete. Software should fail the device if the BIST is not complete after 2 seconds.
5:4	R	RO	Reserved. These bits always return zero.
3:0	CODE	RO	Completion Code. A value of zero means the device has passed its test. Non-zero values means the device has failed using device specific failure codes.

SSA7785 ThunderBird Avenger™ CFG Space 1 Legacy Base Address Registers

The SSA7785 ThunderBird Avenger™, contains one legacy I/O base registers in configuration space 1. The joystick is the sole legacy I/O base address register and is documented here.

TABLE 62 16650 UART Base Address - UARTBASE (RW/RO)

PCI CFG 2	D31	D30	D29	D28	D27	D26	D25	D24
Offset 10h	UARTBASE[31:24]							
POR Value	0	0	0	0	0	0	0	0
	D23	D22	D21	D20	D19	D18	D17	D16
	UARTBASE[23:16]							
POR Value	0	0	0	0	0	0	0	0
	D15	D14	D13	D12	D11	D10	D9	D8

	UARTBASE[15:8]							
POR Value	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	UARTBASE[7:3]					R	R	IO
POR Value	0	0	0	0	0	0	0	1

Bit	Name	R/W	Function
31:3	UART-BASE	RW	16650 UART base address. The address should be on a 8 byte boundary. For reference, 550 compatible UART legacy base addresses are 3E8h, 338h, 2E8h, 220h, 238h, 2E0h, 228h, 3F8h, and 2F8h.
2:1	R	RO	Reserved. These bits are reserved and always return zeros for plug and play.
0	IO	RO	I/O flag. This read only bit indicates that this is an I/O range.

TABLE 63 Subsystem Vendor ID - SUBVENID (RO)

PCI CFG 2	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Offset 2Ch	SUBVEN_ID[15:8]							
POR Value	0	0	0	1	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SUBVEN_ID[7:0]							
POR Value	0	0	0	0	0	1	0	0

Bit	Name	R/W	Function
15:0	SUBVEN_ID	RO	Subsystem Vendor ID. The Subsystem Vendor ID register allows the manufacturer to uniquely identify their board since more than one board OEM may use the SSA7785 ThunderBird Avenger™ chip. The Subsystem Vendor ID register is loaded by an external EEPROM via the Serial Configuration Port after reset and before any access to the PCI configuration header. The PCI target logic should force a retry if the Subsystem Vendor ID register has not completed loading. The Subsystem Vendor ID is read only to the PCI interface. If no external EEPROM is present, then the default Subsystem Vendor ID is 1004h, that of Philips Semiconductors (VLSI).

TABLE 64 Subsystem ID - SUBSYSID (RO)

PCI CFG 2	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**

Offset 2Eh	SUBSYS_ID[15:8]							
POR Value	0	0	0	0	0	0	1	1
	D7	D6	D5	D4	D3	D2	D1	D0
	SUBSYS_ID[7:0]							
POR Value	0	0	0	0	0	1	1	0

Bit	Name	R/W	Function
15:0	SUBSYS_ID	RO	Subsystem ID. The Subsystem ID register allows the manufacturer to uniquely identify their board since more than one board OEM may use the SSA7785 ThunderBird Avenger™ chip. The Subsystem ID register is loaded by an external EEPROM via the Serial Configuration Port after reset and before any access to the PCI configuration header. The PCI target logic should force a retry if the Subsystem ID register has not completed loading. The Subsystem ID is read only to the PCI interface. If no external EEPROM is present, then the default Subsystem ID is 0306h, identical to the SSA7785 ThunderBird Avenger™ function 2 Device ID.

TABLE 65 Interrupt Line Register - INTLINE (RO)

PCI CFG 2	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Ch	INTLINE[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	INTLINE	RO	Interrupt Line. The Interrupt Line register is an eight bit register used to communicate interrupt line routing information. The value in this register tells which input of the system interrupt controller(s) the SSA7785 ThunderBird Avenger™ Device's interrupt pin is connected to. It is set to 00h to use function 0's interrupt line. There is no legacy interrupt support for function 2.

TABLE 66 Interrupt Pin Register - INTPIN (RO)

PCI CFG 2	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Dh	INTPIN[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	INTPIN	RO	Interrupt Pin. The interrupt pin register tells which interrupt the SSA7785 ThunderBird Avenger™ device uses. The read only value of 00h implies that the SSA7785 ThunderBird Avenger™ device shares the INT A interrupt pin with function 0. There is no legacy interrupt support for function 2.

TABLE 67 MIN_GNT Register - MINGNT (RO)

PCI CFG 2	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Eh	MINGNT[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	MINGNT	RO	Minimum grant specifies how long of a burst period the device needs assuming a clock speed of 33MHz. Since the SSA7785 ThunderBird Avenger™, function 2, is a target only, this register is read only and set to zero.

TABLE 68 MAX_LAT Register - MAXLAT (RO)

PCI CFG 2	D7	D6	D5	D4	D3	D2	D1	D0
Offset 3Fh	MAXLAT[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	MAXLAT	RO	Maximum latency specifies how often a device needs to gain access to the PCI bus. The SSA7785 ThunderBird Avenger™, function 2, is a target only, this register is read only and set to zero.

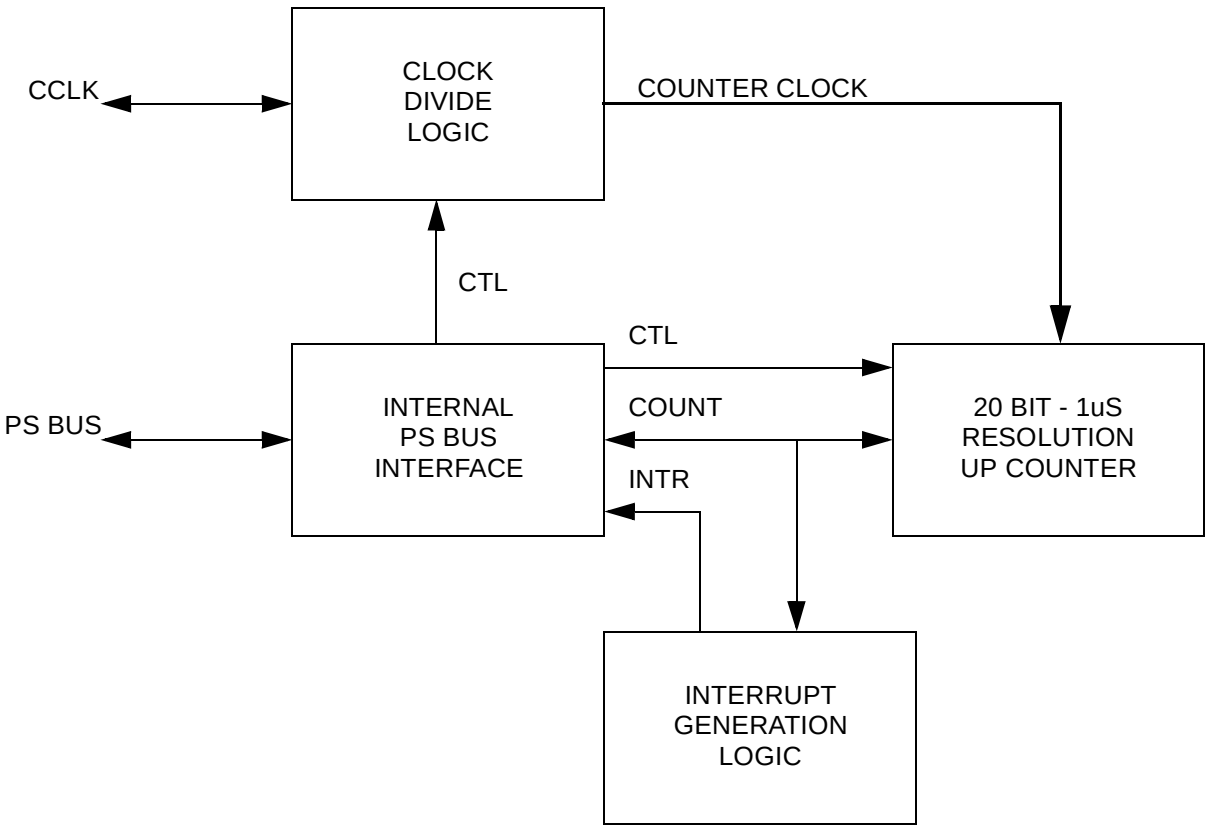
MULTIMEDIA TIMER

OVERVIEW

The Multimedia Timer is a 20 bit counter with 840ns resolution for general purpose use under host software control. The timer subsystem consists of the 20-bit counter and I/O space registers. It takes three I/O cycles to read the complete value of the Timer since the device allows only byte accesses.

The Multimedia Timer will get its time base by dividing down the CCLK clock. An interrupt and flag is provided to determine if the timer count has rolled over. The timer can either start from zero or be preloaded with a start value.

FIGURE 7 MULTIMEDIA TIMER BLOCK DIAGRAM



MULTIMEDIA TIMER REGISTER DEFINITION

There are five registers that control the multimedia timer. These registers are the timer control register, timer status, and timer count registers. The timer control register resides in PCI configuration space. The remainder of the timer registers are in I/O space.

MULTIMEDIA TIMER PCI CONFIGURATION REGISTERS

TABLE 69 TIMRCFG0 (RW/RO) - MULTIMEDIA TIMER CONFIG REGISTER 0

PCI CFG 0	D7	D6	D5	D4	D3	D2	D1	D0
Offset 64h	R	R	R	R	R	FSTCLK	TMRRST	R
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:3	R	RO	Reserved. These bits return zeros.

Bit	Name	R/W	Function
2	FSTCLK	RW	Fast Clock Enable. When set, the timer counter will use the CCLK clock instead of the 570 ns clock. This function will reduce the simulation and test time of the device.
1	TMRRST	RW	Timer Reset. When set, this bit holds the multimedia timer in reset. The multimedia timer is also reset by the system reset.
0	R	RO	Reserved. This bit returns a zero.

MULTIMEDIA TIMER I/O SPACE REGISTERS

TABLE 70 TMSTAT (RW/RO) - MULTIMEDIA TIMER STATUS REGISTER

SONGBASE	D7	D6	D5	D4	D3	D2	D1	D0
Offset 00h	R	R	R	R	TPLD	TRE-SUME	TMINT	TINTEN
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:4	R	RO	Reserved. These bits return zeros.
3	TPLD	RW	Timer Preload Indicator. When set, this indicates the timer will start counting from the values set in the timer count registers. When cleared, the timer will start counting from zero or its last value when stopped
2	TRESUME	RW	Timer Resume. When set, the timer will resume counting at the next 570 ns clock edge. When cleared, the timer will stop counting.
1	TMINT	WC	Timer Interrupt. When asserted, the multimedia timer has flagged an interrupt when the timer has counted to zero. The timer will continue to count. Writing a one to this bit will clear the interrupt.
0	TINTEN	RW	Timer Interrupt Enable. When set, the multimedia timer will generate an interrupt.

MULTIMEDIA TIMER COUNT REGISTERS

There are three registers required to hold the timer value. These three registers can be read at different cycles, It is recommended that the least significant byte be read first for the most accuracy.

TABLE 71 TMCOUNT2 (RW/RO) - MULTIMEDIA TIMER COUNT REGISTER 2

SONGBASE	D7	D6	D5	D4	D3	D2	D1	D0
Offset 03h	R	R	R	R	TMCOUNT2[7:0]			
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:4	R	RO	Reserved. These bits return zeros.

Bit	Name	R/W	Function
3:0	TMCOUNT2	RW	High Nibble Timer Count. This nibble is the most significant digits of the timer value.

TABLE 72 TMCOUNT1 (RW) - MULTIMEDIA TIMER COUNT REGISTER 1

SONGBASE	D7	D6	D5	D4	D3	D2	D1	D0
Offset 02h	TMCOUNT1[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	TMCOUNT1	RW	Middle Byte Timer Count. This byte is the middle significant digits of the timer value.

TABLE 73 TMCOUNT0 (RW) - MULTIMEDIA TIMER COUNT REGISTER 0

SONGBASE	D7	D6	D5	D4	D3	D2	D1	D0
Offset 01h	TMCOUNT0[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	TMCOUNT0	RW	Low Byte Timer Count. This byte is the least significant digits of the timer value.

PCI I/O SPACE GPIO SUPPORT

The Multimedia Timer house eight General Purpose I/O ports. These ports are independently controlled under host software.

TABLE 74 PGPIODIR (RW) - PCI GENERAL PURPOSE INPUT/OUPUT DIRECTION

SONGBASE	D7	D6	D5	D4	D3	D2	D1	D0
Offset 04h	PGPIO_DIR[7:0]							
POR Value	0	0	0	0	0	0	0	0

Bit	Name	R/W	Function
7:0	PGPIO_DIR	RW	PCI General Purpose I/O Data Direction Bit. These bits control whether the GPIO pins 0 through 7 act as an input or an output. 0 = Selected GPIO pin is an output. 1 = Selected GPIO pin is an input.

ThunderBird Avenger™ PCI Audio Accelerator

SAA7785

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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