256K X 8 Bit CMOS Video RAM

FEATURES

* **Dual port Architecture**
  256K x 8 bits RAM port
  512 x 8 bits SAM port
* **Performance range :**

Parameter \ Speed	-6	-7	-8
RAM access time (t_{RAC})	60ns	70ns	80ns
RAM access time (t_{CAC})	15ns	20ns	20ns
RAM cycle time (t_{RC})	110ns	130ns	150ns
RAM page mode cycle (t_{PC})	40ns	45ns	50ns
SAM access time (t_{SCA})	15ns	17ns	20ns
SAM cycle time (t_{SCC})	18ns	22ns	25ns
RAM active current	110mA	100mA	90mA
SAM active current	55mA	50mA	45mA

* **Fast Page Mode**
* **RAM Read, Write, Read-Modify-Write**
* **Serial Read (SR) and Serial Write (SW)**
* **Read / Real time read transfer (RT, RRT)**
* **Split Read Transfer with Stop Operation (SRT)**
* **Write and Split Write Transfer (New Mask), (WT,SWT)**
* **Block Write (BW), Flash Write (FLW) and Write-per-Bit with Masking Operation (New Mask)**
* **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
* **Common Data I/O Using three state RAM Output control**
* **All Inputs and Outputs TTL Compatible**
* **Refresh: 512 Cycle/8ms**
* **KM428C256 : 60, 70, 80ns**
* **Plastic 40-Pin 400 mil SOJ**
* **Plastic 40/44-Pin 400 mil TSOP II (Forward and Reverse Type)**

GENERAL DESCRIPTION

The Samsung KM428C256 is a CMOS 256K x 8 bit Dual Port DRAM. It consists of a 256K x 8 dynamic random access memory (RAM) port and 512 x 8 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 4096 bits.
It operates like a conventional 256K x 8 CMOS DRAM.
The RAM port has a write per bit mask capability.
Data may be written with New Mask. The RAM port has a Fast Page mode access, Block Write and Flash Write capability.

The SAM port consists of eight 512 bit high speed shift registers that are connected to the RAM array through a 4096 bit data transfer gate. The SAM port has serial read and write capabilities.

Data may be internally transferred bi-directionally between the RAM and SAM ports using read, write Split Transfers or normal Read/Write Transfer.

Refresh is accomplished by familiar DRAM refresh modes. The KM428C256 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

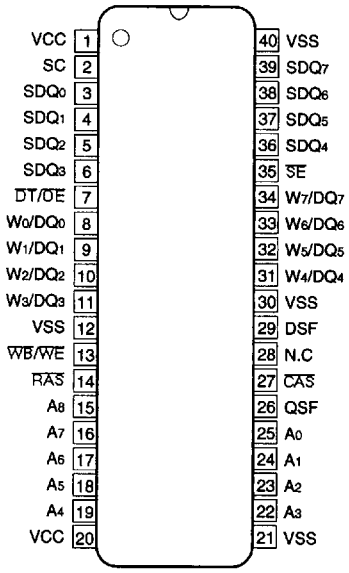
All inputs and I/O's are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN DESCRIPTION

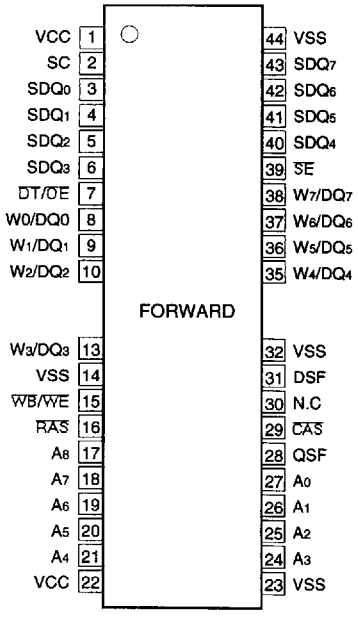
SYMBOL	TYPE	DESCRIPTION
$\overline{RAS}$	IN	Row address strobe. $\overline{RAS}$ is the control input that latchs row address bits. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "High".
$\overline{CAS}$	IN	Column address strobe. $\overline{CAS}$ is the control input that latchs column address bits. $\overline{CAS}$ also acts as an output enable for the output buffer on the RAM port.
Address	IN	Address inputs for the DRAM operation, these inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 262,144 available. 9 row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following 9 column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).
$\overline{WB}/\overline{WE}$	IN	The $\overline{WB}/\overline{WE}$ inputs is a multifunction pin. When $\overline{WB}/\overline{WE}$ is "High" at the falling edge of $\overline{RAS}$, during RAM port operation, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "Low" at the falling edge of $\overline{RAS}$, during RAM port operation, the W-P-B function is enabled.
$\overline{DT}/\overline{OE}$	IN	The $\overline{DT}/\overline{OE}$ input is also a multifunction pin. Enables an internal Transfer operation at the falling edge of $\overline{RAS}$ when Transfer enable.
DSF	IN	DSF is used to indicate which special functions (BW, FW, Split Transfer, etc.) are used for a particular access cycle.
Wi/DQi	IN /OUT	Data I/O for DRAM access. These pins act as inputs for Mask and register load cycles, DQ Mask and Column Mask for BW.
SC	IN	Clock input to the serial address counter and data latch for the SAM register.
QSF	OUT	QSF indicates which half of the SAM is being accessed. Low if address is 0~255, High if address is 256~511.
SDQi	IN/OUT	Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle.
$\overline{SE}$	IN	In a serial read cycle, $\overline{SE}$ is used as an output control. When $\overline{SE}$ is "High", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.
Vcc	SUPPLY	Power supply
Vss	SUPPLY	Ground

PIN CONFIGURATION (TOP VIEWS)

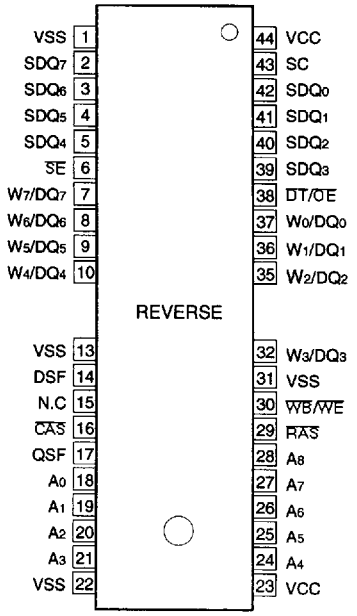
40 Pin 400 mil SOJ



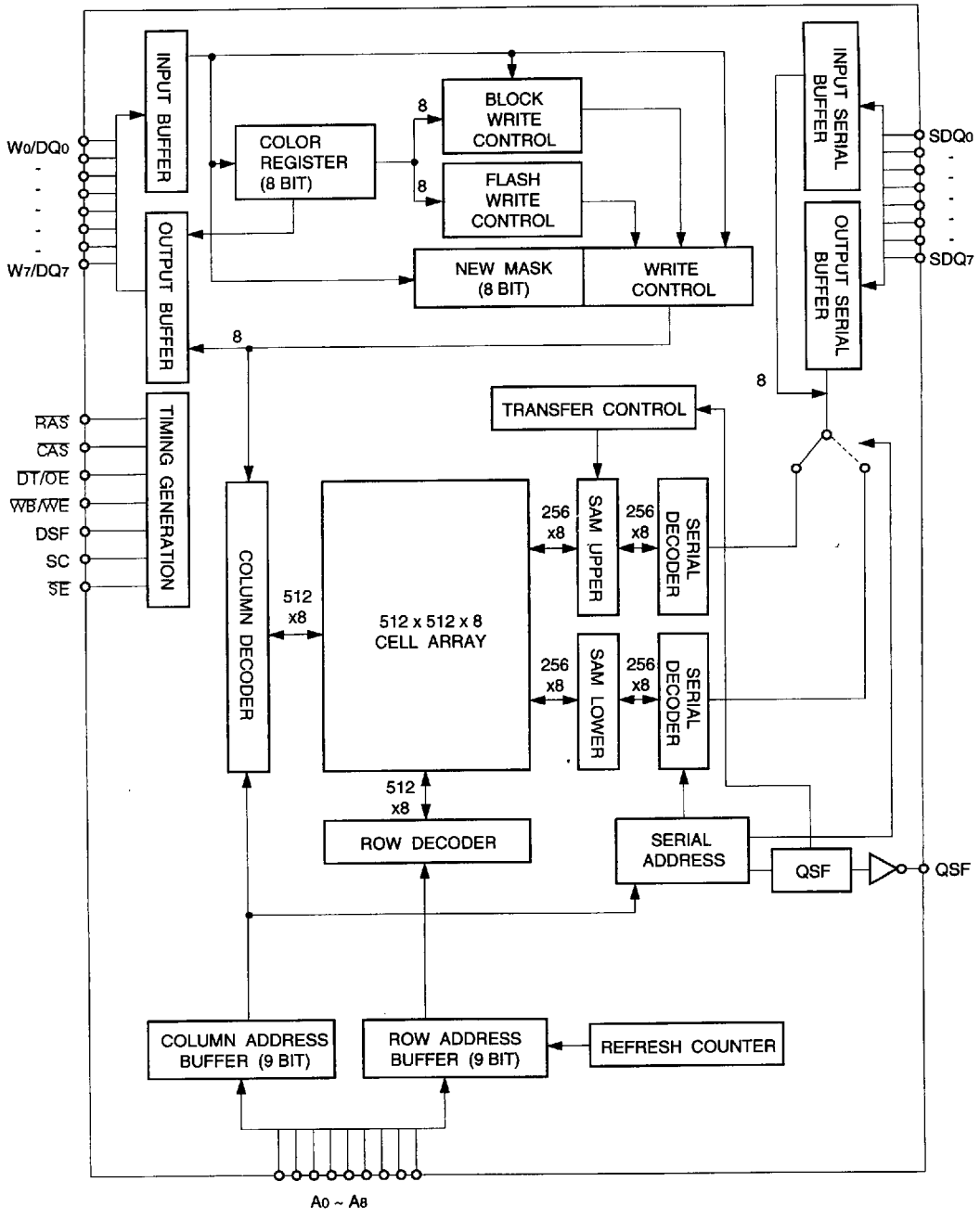
40/44 Pin 400 mil TSOP II



40/44 Pin 400 mil TSOP II



BLOCK DIAGRAM



FUNCTION TRUTH TABLE

Mnemonic Code	RAS falling edge					CAS	Address*1		DQi Input*2		Write Mask	Color Register	Function
	CAS	DT/OE	WE	DSF	SE	DSF	RAS	CAS	RAS	CAS/WE			
CBR	0	X	X	X	X	-	X	X	X	-	-	-	CBR Refresh
ROR	1	1	X	0	X	-	Row	X	X	-	-	-	RAS-only Refresh
RW	1	1	1	0	X	0	Row	Col.	X	Data	No	-	Normal DRAM Read/ Write (No. Mask)
RWNM	1	1	0	0	X	0	Row	Col.	WMi	Data	Use	-	Masked DRAM Write (New Mask)
MFLW	1	1	0	1	X	X	Row	X	WMi	X	Use	Use	Masked Flash Write (New Mask)
BW	1	1	1	0	X	1	Row	Col. (A2~A8)	X	Col. Mask	No	Use	Block Write (No Mask)
BWNW	1	1	0	0	X	1	Row	Col. (A2~A8)	WMi	Col. Mask	Use	Use	Masked Block Write (New Mask)
LCR	1	1	1	1	X	1	Row*3	X	X	Color Data	-	Load	Load Color Register
RT	1	0	1	0	X	X	Row	Tap	X	X	-	-	Read Transfer
SRT	1	0	1	1	X	X	Row	Tap	X	X	-	-	Split Read Transfer
PWT	1	0	0	0	1	X	Row*3	Tap	X	X	-	-	Pseudo Write Transfer
MWT	1	0	0	0	0	X	Row	Tap	WMi	X	Use	-	Masked Write Transfer (New Mask)
MSWT	1	0	0	1	X	X	Row	Tap	WMi	X	Use	-	Masked Split Write Transfer (New Mask)

X : Don't Care, - : Not Applicable, Tap : SAM Start (Column) Address

Notes :

*1 : These column show what must be present on the A_0 ~ A_8 outputs at the falling edge of RAS and CAS.

*2 : These column show what must be present on the DQ_0 ~ DQ_7 outputs at the falling edge of RAS, CAS or WB/WE, whichever is later.

*3 : The Row that addressed will be refreshed.

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, TA = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc + 1V	V
Input Low Voltage	V_{IL}	- 1.0	-	0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \le V_{IN} \le V_{CC} + 0.5V$, all other pins not under test=0 volts, $\overline{SE} \ge V_{CC}-0.2V$)	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

CAPACITANCE (V_{CC} = 5V, f = 1MHz, T_A=25 °C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}$ /$\overline{WE}$, $\overline{DT/OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_7/DQ_7)	C_{DQ}	2	7	pF
Input/Output Capacitance (SDQ_0~SDQ_7)	C_{SDQ}	2	7	pF
Output Capacitance (QSF)	C_{QSF}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter (RAM Port)	SAM port	Symbol	KM428C257			Unit
			-6	-7	-8	
Operating Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)	Standby	ICC1	110	100	90	mA
	Active	ICC1A	155	140	125	mA
Standby Current ($\overline{RAS}$, $\overline{CAS}$, DT /$\overline{OE}$, WB/$\overline{WE}$ =VIH, DSF = VIL)	Standby	ICC2	10	10	10	mA
	Active	ICC2A	55	50	45	mA
$\overline{RAS}$ Only Refresh Current*1 ($\overline{CAS}$ =VIH, $\overline{RAS}$ Cycling @ tRC=min)	Standby	ICC3	100	90	80	mA
	Active	ICC3A	145	130	115	mA
Fast Page Mode Current*1 ($\overline{RAS}$=VIL, $\overline{CAS}$ Cycling @ tPC=min)	Standby	ICC4	80	75	70	mA
	Active	ICC4A	125	115	105	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)	Standby	ICC5	90	85	80	mA
	Active	ICC5A	135	125	115	mA
Data Transfer Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)	Standby	ICC6	140	125	110	mA
	Active	ICC6A	185	165	145	mA
Flash Write Cycle Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)	Standby	ICC7	90	85	80	mA
	Active	ICC7A	135	125	115	mA
Block Write Cycle Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)	Standby	ICC8	110	105	100	mA
	Active	ICC8A	155	145	135	mA
Color Register Load or Read Current*1 ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)	Standby	ICC9	90	85	80	mA
	Active	ICC9A	135	125	115	mA

Note*1 : Real values dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as average current. In Icc1, Icc3, Icc6, Icc7, Icc8, Icc9 address transition should be changed only once while $\overline{RAS}$=VIL. In Icc4 address transition should be changed only once while $\overline{CAS}$ =VIH.

AC CHARACTERISTICS (0 °C≤TA≤70 °C, VCC=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		175		200		ns	
Fast page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write	tPRWC	80		85		90		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,5,11
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,5,6
Access time from column address	tAA		30		35		40	ns	3,11
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (fast page mode)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	5,6
$\overline{RAS}$ to column addr. delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
$\overline{CAS}$ precharge time	tCPT	20		25		30		ns	
$\overline{CAS}$ p recharge time (fast page mode)	tCP	10		10		10		ns	
Row addr. set-up time	tASR	0		0		0		ns	
Row Addr. hold time	tRAH	10		10		10		ns	
Column addr. set-up time	tASC	0		0		0		ns	
Column addr. hold time	tCAH	15		15		15		ns	
Column addr. hold referenced to $\overline{RAS}$	tAR	50		55		60		ns	
Column addr. to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	tWCR	45		55		60		ns	15
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	15		15		15		ns	10
Data hold referenced to $\overline{RAS}$	tDHR	50		55		60		ns	15
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ Precharge ro $\overline{WE}$ Delay(Page Mode)	tCPWD	60		65		70		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	40		45		45		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	85		95		105		ns	8
Column addr. to $\overline{WE}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ set-up time (CBR refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time (CBR refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	10		10		10		ns	
Access time from output enable	tOEA		15		20		20	ns	
Output enable to data input delay	tOED	15		15		15		ns	
Output buffer turn-off delay from $\overline{OE}$	tOEZ	0	15	0	15	0	15		7

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Output enable command hold time	tOEH	15		15		15		ns	
Data to $\overline{CAS}$ delay	tDZC	0		0		0		ns	
Data to output enable delay	tDZO	0		0		0		ns	
Refresh period (512 cycle)	tREF		8		8		8	ms	
$\overline{WB}$ set-up time	tWSR	0		0		0		ns	
$\overline{WB}$ hold time	tRWH	10		10		15		ns	
DSF hold time referenced to $\overline{RAS}$ (II)	tFHR	45		55		60		ns	13
DSF set-up time referenced to $\overline{RAS}$	tFSR	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$ (I)	tRFH	10		10		15		ns	13
DSF set-up time referenced to $\overline{CAS}$	tFSC	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	tCFH	10		15		15		ns	
Write per bit mask data set-up time	tMS	0		0		0		ns	
Write per bit mask data hold time	tMH	15		15		15		ns	
$\overline{DT}$ high set-up time	tTHS	0		0		0		ns	
$\overline{DT}$ high hold time	tTHH	10		10		15		ns	
$\overline{DT}$ low set-up time	tTLS	0		0		0		ns	
$\overline{DT}$ low hold time	tTLH	10		10		15		ns	
$\overline{DT}$ low hold ref. to $\overline{RAS}$ (real time read transfer)	tRTH	50		60		65		ns	
$\overline{DT}$ low hold ref. to $\overline{CAS}$ (real time read transfer)	tCTH	15		20		25		ns	
$\overline{DT}$ low hold ref. to col. addr. (real time read transfer)	tATH	20		25		30		ns	
$\overline{SE}$ setup referenced to $\overline{RAS}$	tESR	0		0		0		ns	
$\overline{SE}$ hold time reference to $\overline{RAS}$	tREH	10		10		10		ns	
$\overline{DT}$ to $\overline{RAS}$ precharge time	tTRP	40		50		60		ns	
$\overline{DT}$ precharge time	tTP	20		20		20		ns	
$\overline{RAS}$ to first SC delay (read transfer)	tRSD	60		70		80		ns	
$\overline{CAS}$ to first SC delay (read transfer)	tCSD	25		30		35		ns	
Col. Addr. to first SC delay (read transfer)	tASD	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	tTSL	5		5		5		ns	
$\overline{DT}$ to first SC delay time (read transfer)	tTSD	10		10		15		ns	
Last SC to $\overline{RAS}$ set-up time (serial input)	tSRS	30		30		30		ns	
$\overline{RAS}$ to first SC delay time (serial input)	tSRD	20		20		25		ns	
$\overline{RAS}$ to serial input delay time	tSDD	30		40		50		ns	
Serial output buffer turn-off delay from $\overline{RAS}$	tSDZ	10	30	10	30	10	35	ns	7
Serial input to first SC delay time	tSZS	0		0		0		ns	
SC cycle time	tSCC	18		22		25		ns	
SC pulse width (SC high time)	tSC	6		7		7		ns	14
SC precharge (SC low time)	tSCP	6		7		7		ns	

AC CHARACTERISTICS (Continued)

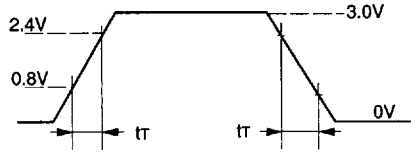
Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from SC	tSCA		15		17		20	ns	4
Serial output hold time from SC	tSOH	5		5		5		ns	
Serial input set-up time	tSDS	0		0		0		ns	
Serial input hold time	tSDH	10		15		15		ns	
Access time from $\overline{SE}$	tSEA		15		17		20	ns	4
$\overline{SE}$ pulse width	tSE	20		20		25		ns	
$\overline{SE}$ precharge time	tSEP	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	tSEZ	0	15	0	15	0	15	ns	7
Serial input to $\overline{SE}$ delay time	tSZE	0		0		0		ns	
Serial write enable set-up time	tSWS	0		0		0		ns	
Serial write enable hold time	tSWH	10		15		15		ns	
Serial write disable set-up time	tSWIS	0		0		0		ns	
Serial write disable hold time	tSWIH	10		15		15		ns	
Split transfer set-up time	tSTS	20		25		25		ns	
Split transfer hold time	tSTH	20		25		25		ns	
SC-QSF delay time	tSQD		20		25		25	ns	
$\overline{DT}$-QSF delay time	tTQD		20		25		25	ns	
$\overline{RAS}$-QSF delay time	tRQD		60		70		80	ns	
$\overline{CAS}$-QSF delay time	tCQD		20		35		40	ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved. ($\overline{DT}/\overline{OE}$ = High) If the internal refresh counter is used a minimum of 8 $\overline{CAS}$- before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all input signals.
   Input signal transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   D_{OUT} comparator level:V_{OH}/V_{OL} =2.0V / 0.8V
4. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   Dout comparator level: V_{OH}/V_{OL}= 2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. The parameters, t_{OFF}(max), t_{OEZ}(max), and t_{SDZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insured that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. During power-up $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ must be held High or Track with Vcc. After power-up, initial status of chip is described below.

PIN or REGISTER	STATUS
QSF	Hi-Z
Color Register	Don't Care
Tap Pointer	Invalid
Wi/DQi	Hi-Z
SAM Port	Input Mode
SDQi	Hi-Z

13. Operating input condition :



   Input pulse levels are from 0.0V to 3.0Volts.
   All timing measurements are referenced from V_{IL} (max) and V_{IH} (min) with transition time = 5.0ns
14. Assume t_T = 3ns.
15. t_{WCR}, t_{DHR} are referenced to t_{RAD} (max).

2-1

DEVICE OPERATIONS

The KM428C256 contains 2,097,152 memory locations. Eighteen address bits are required to address a particular 8bit word in the memory array. Since the KM428C256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM428C256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address and are strobed in by $\overline{CAS}$. This is the beginning of any KM428C256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM428C256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}$ / $\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD} (max) then the access time to valid data is specified by t_{RAC} (min). However, if $\overline{CAS}$ goes low after t_{RCD} (max) or the column address becomes valid after t_{RAD} (max), access is specified by t_{CAC} or t_{AA}.
The KM428C256 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

RAM Write

The KM428C256 can perform early write and Read-Modify-Write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$. In any type of write cycle Data-in must be valid at or before the falling edge of $\overline{WB}/\overline{WE}$.

New Masked Write Per Bit

The New Masked Write cycle is achieved by maintaining $\overline{CAS}$ high and $\overline{WB}/\overline{WE}$ low at the falling edge of $\overline{RAS}$. The mask data on W_0/DQ_0 ~ W_7/DQ_7 pins are latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data is low, writing is inhibited into the RAM which is remained without changes. When the mask data is high, data is written into the RAM. The mask data is valid for only one cycle, defined by an active $\overline{RAS}$ period. Mask data must be provided in every write cycle that a masking operation is desired.

The Early Write cycle is achieved by $\overline{WB}/\overline{WE}$ low before $\overline{CAS}$ falling and the Late Write cycle is achieved by $\overline{WB}/\overline{WE}$ high before $\overline{CAS}$ falling. During the Early or Late Write cycle, input data through W_0/DQ_0 ~ W_7/DQ_7 must meet the set-up and hold time at the falling edge of $\overline{CAS}$ or $\overline{WB}/\overline{WE}$.
When $\overline{WB}/\overline{WE}$ is high at the falling edge of $\overline{RAS}$, no operation masking is performed.

Table 1. Truth table for write-per-bit function

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	WI/DQI	FUNCTION
↓	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	INHIBIT WRITE

DEVICE OPERATIONS (Continued)

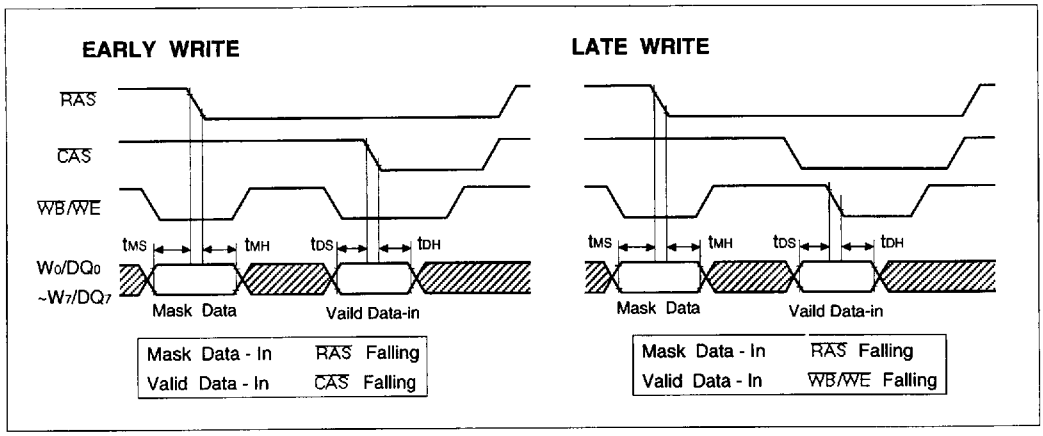


Figure 1. New Masked Write Cycle Example 1 (Early Write & Late Write)

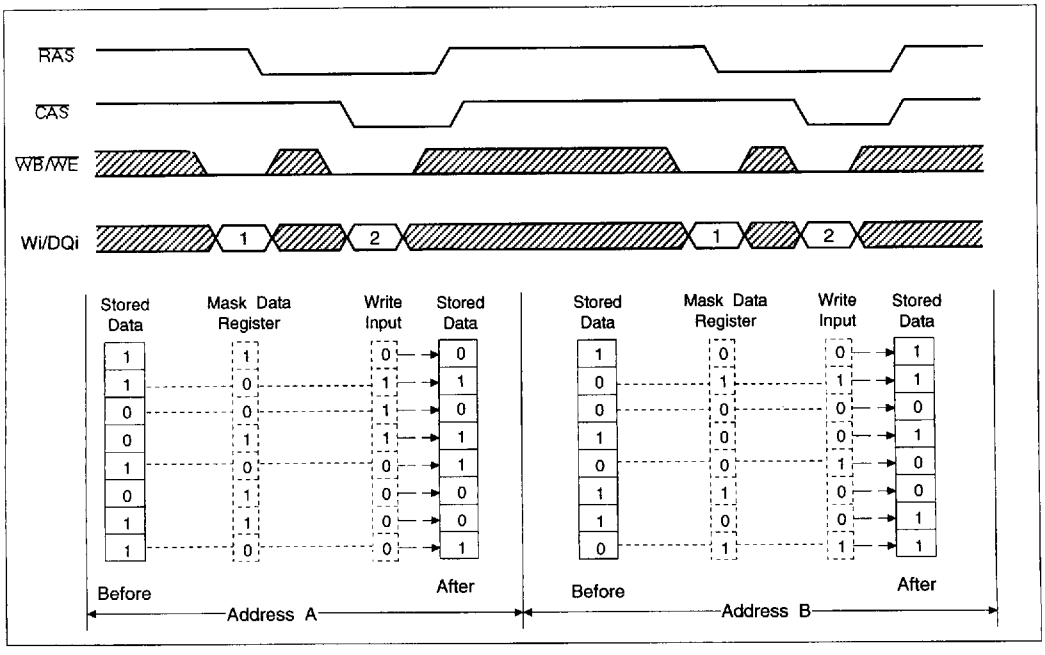


Figure 2. New Mask Write Cycle Example 2.

Fast Page Mode

Fast page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. In this cycle, read, write, read-modify-write and block write cycles can be mixed.

In one $\overline{RAS}$ cycle , 512 word memory cells of the same row address can be accessed. While $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column address. This eliminates the time required to set up and strobe sequential row address for the same page.

DEVICE OPERATIONS (Continued)

Load Color Register (LCR)

A Load Color Register cycle is performed by keeping DSF high on the both the falling edge of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded on the falling of the $\overline{CAS}$ (early write) or $\overline{WE}$ (delayed write) via the W_0/DQ_0~W_7/DQ_7 pins. This data is used in Block Write and Flash Write cycles and remains unchanged until the next Load Color Register cycle.

Block Wirte

In Block Write cycle, four adjacent column location can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 8-bit Color Register must be loaded with the data to be written by performing a Load Color Register (LCR) cycle. When a Block Write cycle is performed, each bit of the Color Register is written into four adjacent location of the same row of each corresponding bit plane (8).
This result in a total of 32-bits being written in single Block Write cycle compared to 8-bits in a normal Write cycle.
The Block Write cycle is performed if DSF is low on the falling edge of $\overline{RAS}$ and high on the falling edge of $\overline{CAS}$.
Address Lines: The row address is latched on the falling edge of $\overline{RAS}$.

Since four bits are being written at a time, when the minimum is increment required for the column address is four. Therefore, when the column address is latched on the falling edge of $\overline{CAS}$, the 2LSBs, A_0 and A_1 are ignored and only bits(A_2~A_8) are used to define the location of the first bit out of the four to be written.
Data Lines: On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0 ~ W_3/DQ_3 pins provided column mask data. This is, for each of the four bits in all 8-bit-plane, writing of Color Register contents can be inhibited.
For example, if $W_0/DQ_0 = 1$ and $W_1/DQ_1 = 0$, then the Color Register contents will be written into the first bit out of the four, but the second remains unchanged. Fig. 3 shows the correspondence of each data line to the column mask bits.

Masked Block Write (BWNM)

A Masked Block Write cycle is identical to a New Mask Write-per-bit cycle except that each of the 8-bit planes being masked is operating on 4-column locations instead of one.
To perform a Masked Block Write cycle, both DSF and $\overline{WB}/\overline{WE}$ must be low at the falling edge of $\overline{CAS}$. Mask data is latched into the device via the W_0/DQ_0~W_7/DQ_7 pins one falling edge of $\overline{RAS}$ and needs to be re-entered for ever new $\overline{RAS}$ cycle.

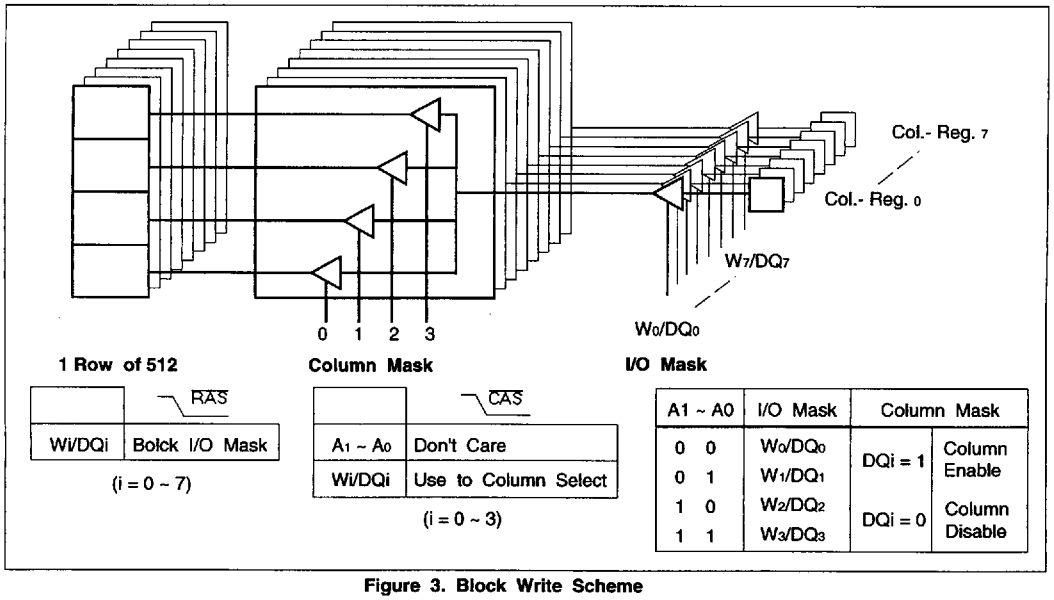


Figure 3. Block Write Scheme

DEVICE OPERATIONS (Continued)

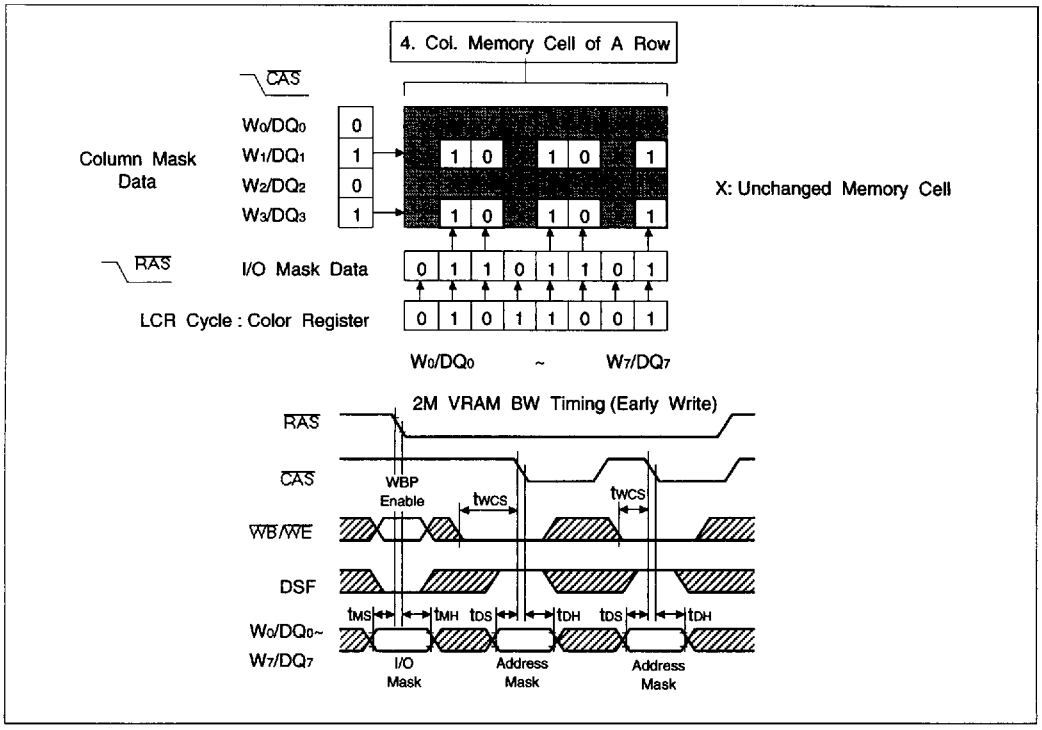


Figure 4. Block Write Example and Timing

Flash Write

The Flash Write cycle is a way of writing each bit of the Color Register into the whole row (512 columns) simultaneously. This function is used for fast screen clear or background color change. 512 columns in each bit plane are written, for a total of 4096 bits (512 x 8 bit planes) in one cycle. While this cycle writes significantly more data than the Block Write cycle, it is also less selective.

If $\overline{WB}/\overline{WE}$ is low and DSF is high on the falling edge of $\overline{RAS}$, a Flash Write cycle is performed. Also on this edge, the data present on the Wi/DQi pins is used as mask data and needs to be provided for every Flash Write cycle. A Load Color Register cycle must have been performed before initiating a Flash Write cycle.

Data Output

The KM428C256 has three state output buffers controlled by $\overline{DT}/\overline{OE}$, $\overline{CAS}$ and $\overline{RAS}$, $\overline{WB}/\overline{WE}$. If $\overline{DT}/\overline{OE}$ is high when $\overline{CAS}$ and $\overline{RAS}$ are low, the output state is in high impedance (High-Z). In any cycle, the output goes low impendance state from the first $\overline{CAS}$ falling edge. Invalid data maybe present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC}, and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM428C256 operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATIONS (Continued)

Refresh

The data in the KM428C256 is stored as a charge on a tiny capacitor within each memory cell. Due to leakage the data may be lost over a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 4096 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address(A_0 ~ A_8).

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh: The KM428C256 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low the on-chip refresh circuitry is enabled.
An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh : A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM428C256 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle.
The refresh row address is the provided by the on-chip refresh address counter.

Other Refresh Methods It is also possible to refresh the KM428C256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed.

There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Transfer Operation

Transfer operations are initiated when $\overline{DT/OE}$ is low at the falling edge of $\overline{RAS}$. The state of $\overline{WB/WE}$ When $\overline{RAS}$ goes low indicates the direction of transfer. (to or from DRAM) and DSF pin is used to designated the proper transfer mode like normal and Split Transfer. Each of the transfer cycle described is the truth table of transfer operation (Table 2.)

Read Transfer (RT)

The Read Transfer operation is set if $\overline{DT/OE}$ is low, $\overline{WB/WE}$ is high, and DSF is low when $\overline{RAS}$ goes low. The row address bits in the read transfer cycle indicate which eight 512 bit DRAM row portion are transferred to the eight SAM data registers. The column address bits indicate the start address of the SAM registers when SAM data read operation is performed. If MSB bit of column address is low during Read transfer operation, the QSF state will be set low and this indicates the start address of SAM register is present at the lower half of SAM port. (If A_8 is high, QSF will be high meaning that the start address is in upper half) Read Transfer may be achieved in two ways. If the transfer is to be synchronized with the SC, $\overline{DT/OE}$ is taken high after $\overline{CAS}$ goes low.
This is usually called "Real Time Read Transfer". Note that the rising edge of $\overline{DT/OE}$ must be synchronized with the rising edge of SC (t_{TSL} / t_{TSD}) to retain the continuity of serial read data output. If the tansfer does not have to be synchronized with SC, $\overline{DT/OE}$ may go high before $\overline{CAS}$ goes low and the actual data transfer will be timed internally.

Masked write Transfer (MWT)

Masked write transfer is initiated if $\overline{DT/OE}$, $\overline{WB/WE}$ and DSF are low when $\overline{RAS}$ goes low. This enables data of SAM

Table 2. Truth Table for Transfer Operation

$\overline{RAS}$ Falling Edge					Function	Transfer Direction	Transfer Data Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	DSF	$\overline{SE}$				
H	L	H	L	*	Read Transfer	RAM → SAM	512 x 8	Input → Output
H	L	L	L	L	Masked Write Transfer	SAM → RAM	512 x 8	Output → Input
H	L	L	L	H	Pseudo Write Transfer	-	-	Output → Input
H	L	H	H	*	Split Read Transfer	RAM → SAM	256 x 8	Not Changed
H	L	L	H	*	Masked Split Write Transfer	SAM → RAM	256 x 8	Not Changed

DEVICE OPERATIONS (Continued)

register (512bit) to be transferred to the selected row in the DRAM array. Masking is selected by latching Wi/DQi (i=0~7) inputs when $\overline{RAS}$ goes low.

The column address defines the start address of serial input and its MSB (A_8) defines QSF level. If A_8 is low, the QSF will be low level to designate that the start address is in positioned in the lower half of SAM. (For A_8=high, the QSF will be high and indicates that the start address will be positioned is the upper half of SAM) After write transfer cycle is completed, SAM port is set to input mode.

Split Read Transfer (SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions (between SC, $\overline{DT/OE}$, $\overline{RAS}$ and $\overline{CAS}$) because the transfer has to be occurred at the first rising edge of $\overline{DT/OE}$.

The Split Read Transfer cycle eliminates the need for this critical transfer timing, thereby simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower or upper half. Since transfer timing is controlled internally, there is no timing restriction between $\overline{DT/OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

A normal Read Transfer cycle must be excuted before performing a Split Read Transfer to set the state of QSF. A Split Read Transfer cycle is begun by keeping DSF and $\overline{WB/WE}$ high and $\overline{DT/OE}$ low at the falling edge of $\overline{RAS}$.

Address : The row address is latched on the falling edge of $\overline{RAS}$. The column address defined by (A_0 ~ A_7) defines the starting address of the SAM port from which data will begin shifting out. Column address pin A_8 is a "Don't Care".

The QSF pin indicates which SAM half is shifting out serial data (0=Lower, 1=Upper). A split Read Transfer will load data into the other half. The state of the QSF output changes when ths SAM address counter reaches a split SAM boundary (e.g. 255th or 511th bit).

Example of SRT applications are shown in Fig. 5 through Fig. 9.

The normal usage of Split Read Transfer cycle is described in Fig. 6. When Read Transfer cycle is executed, data from x1 row address is fully transferred to the SAM port and Serial Read is started from 0 (Tap address). If SRT is performed while data is being serially read from lower half SAM, data from x2 row address is transferred to upper half SAM.

The Tap address of SRT is loaded after the boundary location of lower half SAM (255th SC) is accessed and the QSF state is changed into high level at the rising edge of 255th SC.

Note that in this case "0+256" Tap address instead of "0" is loaded. The another example of SRT cycle is described in Fig. 6. When Serial Read is performed after executing RT and SRT in succession the data access by first SC is the data of RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 7 and Fig. 8 are example of abnormal SRT cycle.

If SRT1 and SRT2 are performed insuccession before accessing the boundary like Fig. 7, the data transferred by SRT2 overwrite the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle.

The Fig. 8. indicates that SRT cycle is not performed until Serial Read is completed to the boundary location 511.

In this case, the internal serial counter is designed to designate "0" address after boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that there is not allowed period of SRT cycle. Since a SRT cycle must be ended before t_{STH} and started after t_{STS}, a split transfer is not allowed during $t_{STH}+t_{STS}$ (See Fig. 9). This is also true in Masked Split Write Transfer. A Split Read Transfer does not change the direction of the SAM I/O port.

Masked Split Write Transfer (MSWT)

This transfer function is very similar to the SRT except the data transfer direction is from RAM to SAM. MSWT is enabled if $\overline{DT/OE}$ low, $\overline{WB/WE}$ low, and DSF high when $\overline{RAS}$ goes low. The bit masking of this cycle is the same as that of MWT(Masked Write Transfer) and the SAM port direction is not changed by performing MSWT. And the column address is latched in as the start address of SAM port and the MSB (A_8) is a "Don't care". The example of MSWT is described in Fig. 10. The opening cycle MWT is needed before MSWT can be performed.

DEVICE OPERATIONS (Continued)

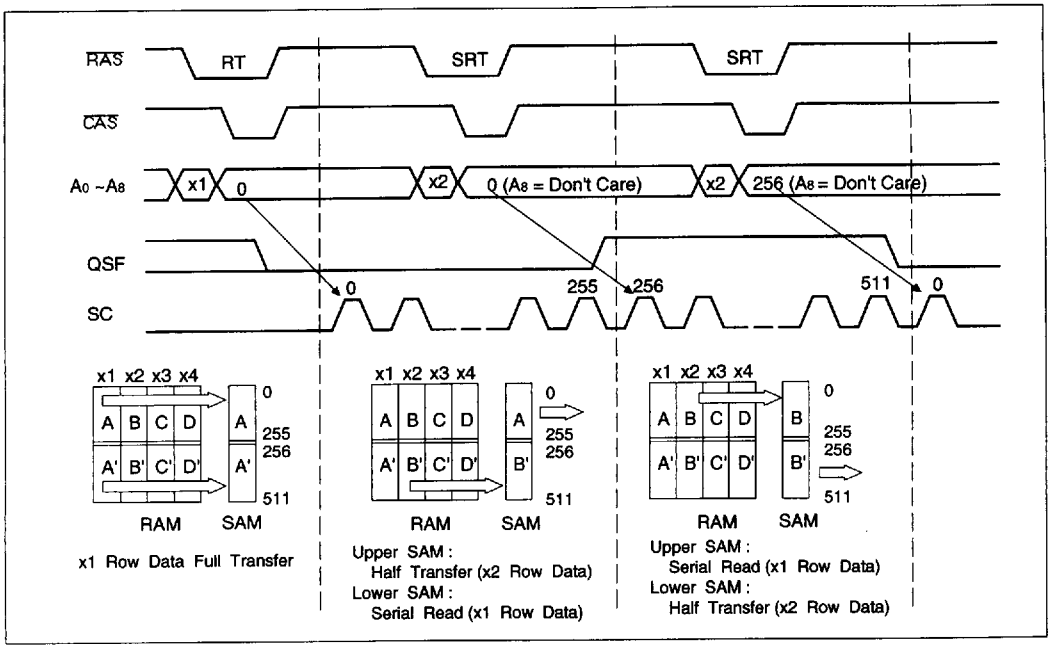


Figure 5. Split Read Transfer Normal Usage

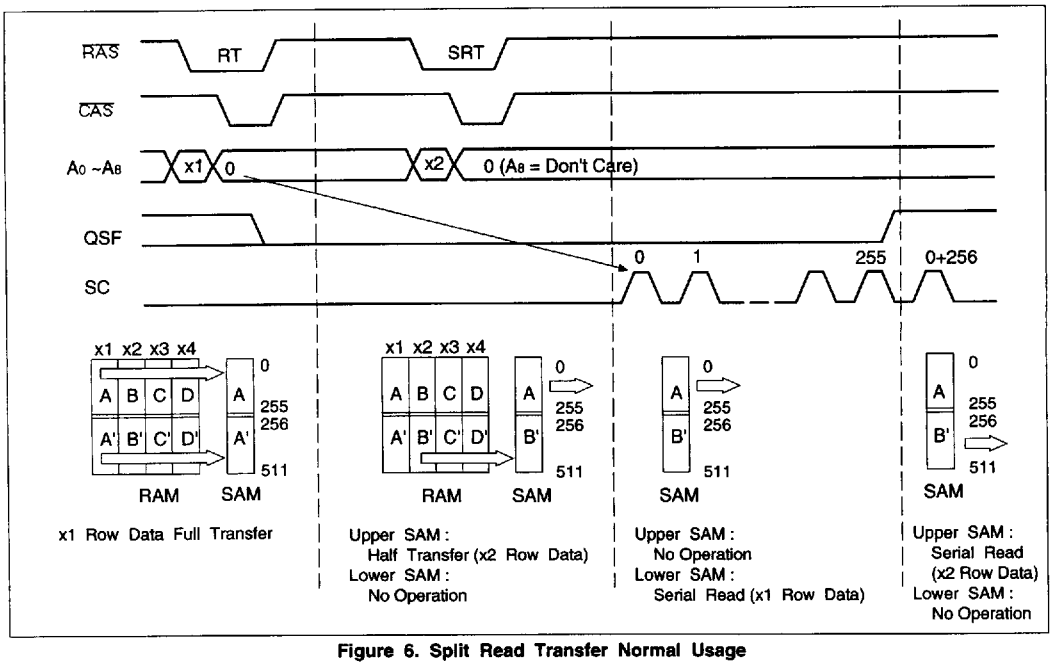


Figure 6. Split Read Transfer Normal Usage

DEVICE OPERATIONS (Continued)

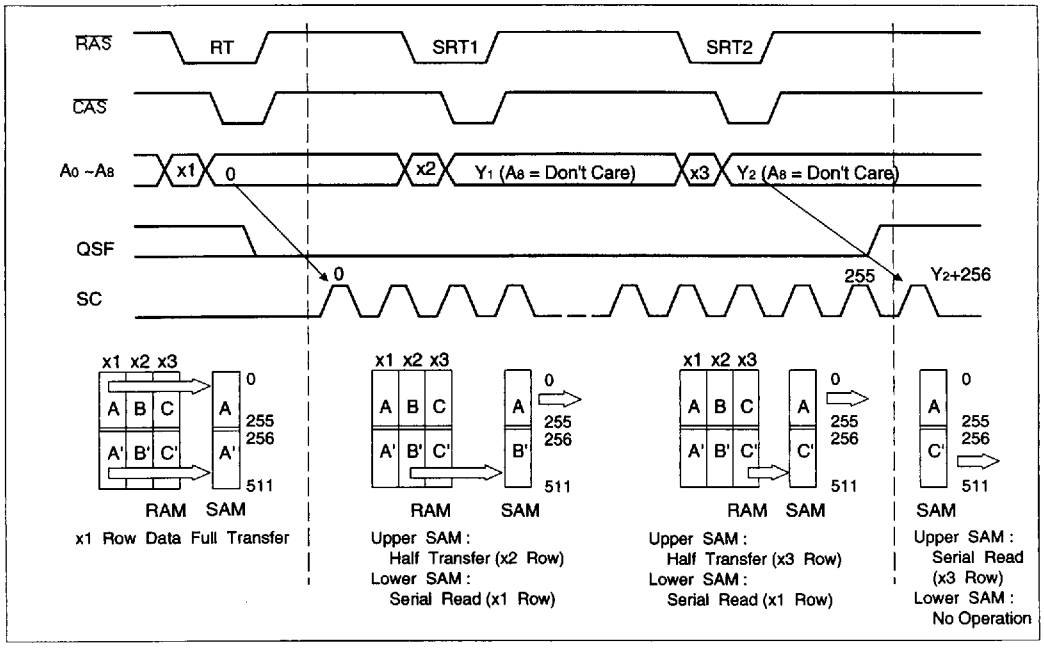


Figure 7. Split Read Transfer Abnormal Usage (Case 1)

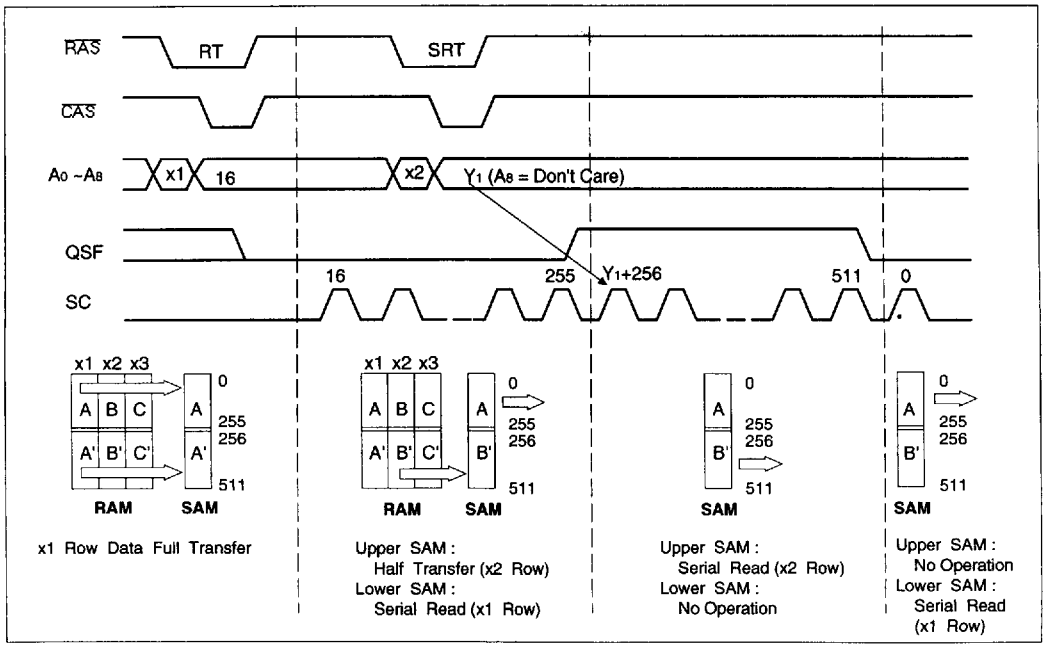


Figure 8. Split Read Transfer Abnormal Usage (Case 2)

DEVICE OPERATIONS (Continued)

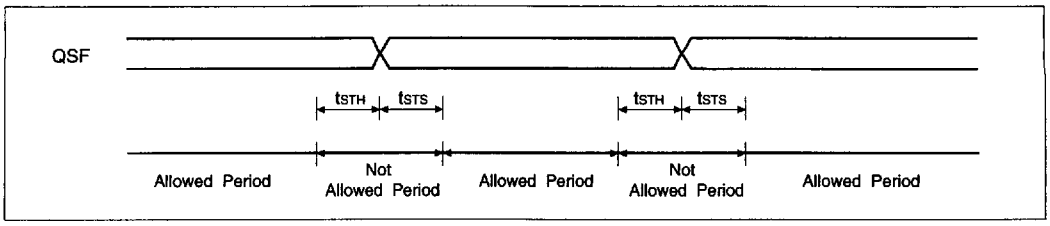


Figure 9 Split Transfer Cycle Limitation Period

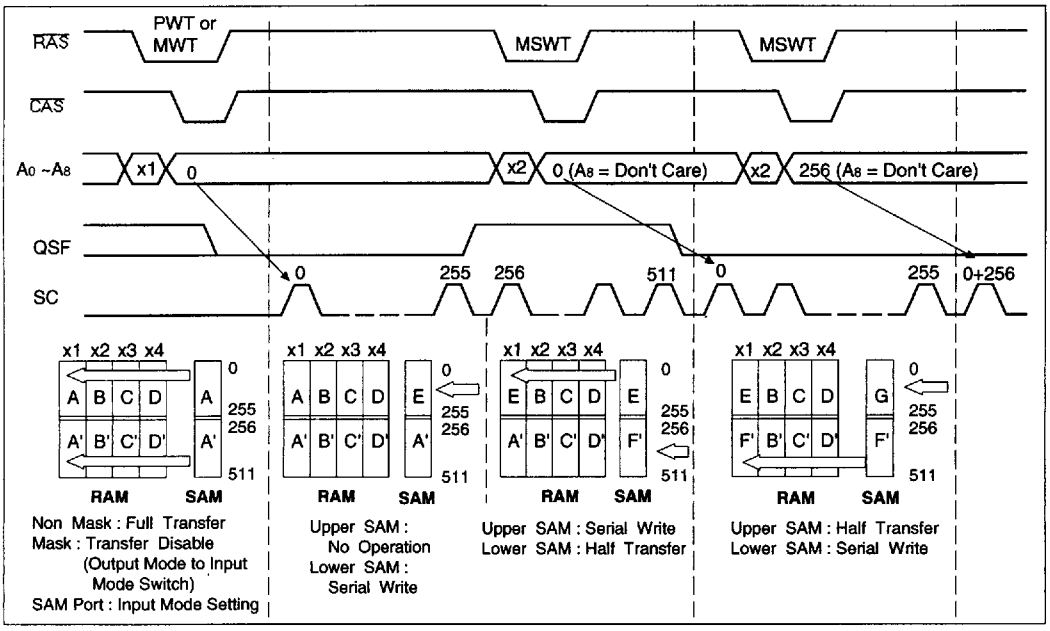
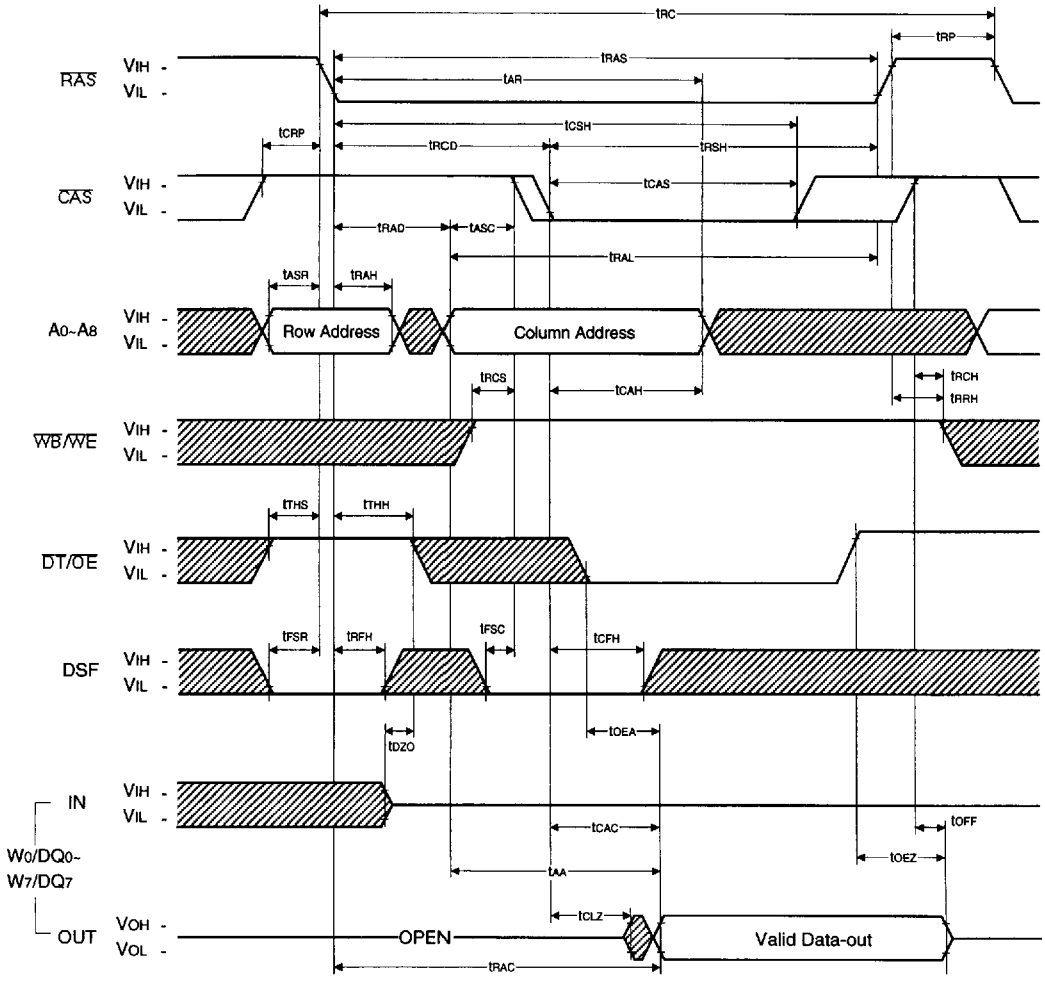


Figure 10. Masked Split Write Transfer Normal Usage

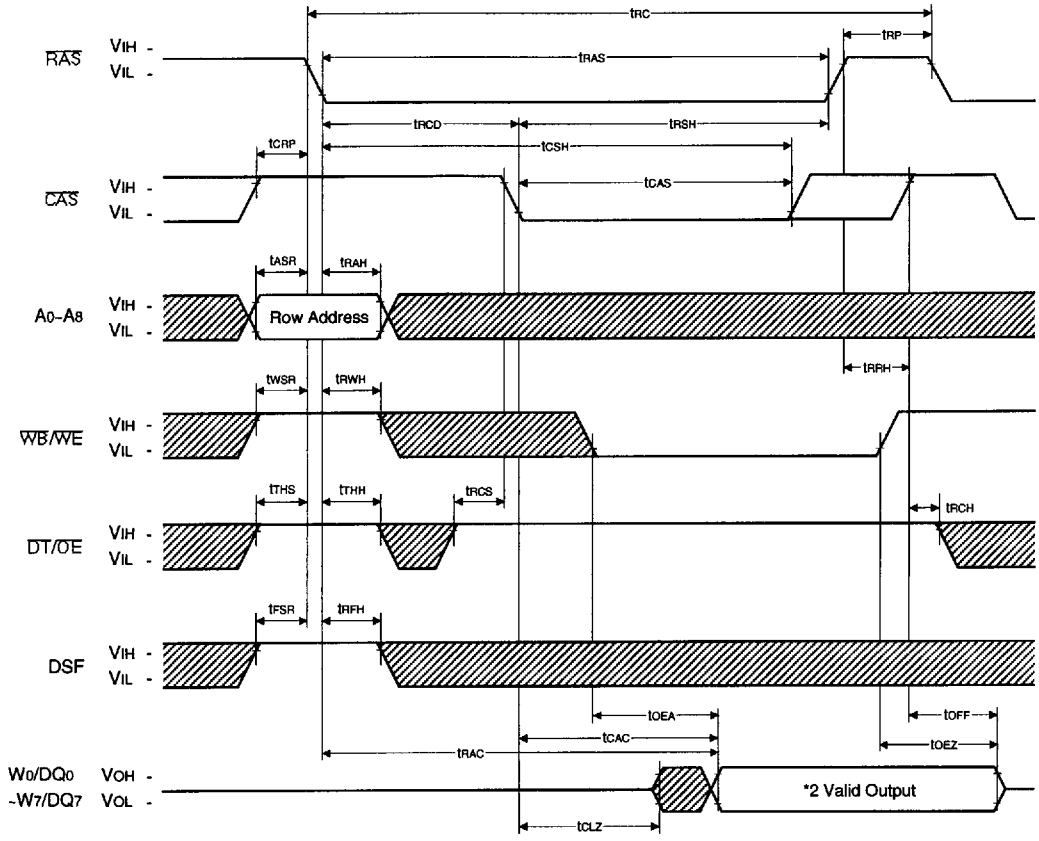
TIMING DIAGRAMS

READ CYCLE

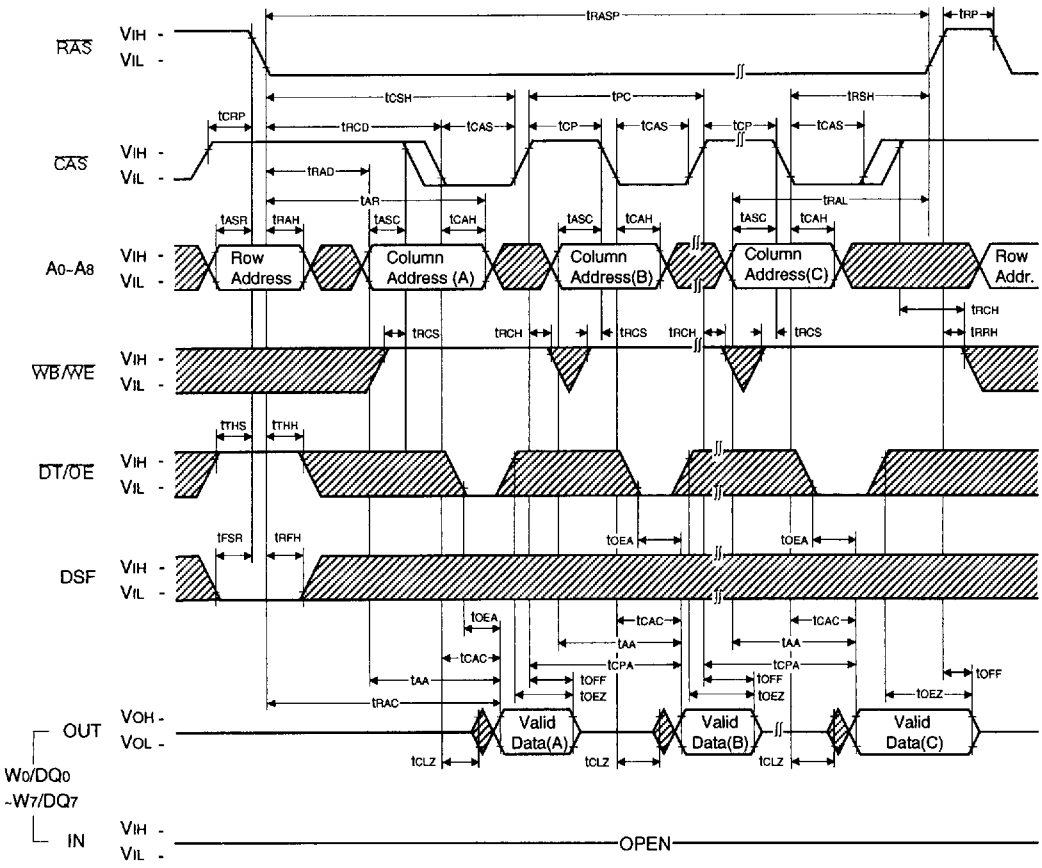


: Don't Care

READ COLOR REGISTER CYCLE



FAST PAGE MODE READ CYCLE



: Don't Care

TRUTH TABLE FOR WRITE CYCLE(1)

FUNCTION	RAS			CAS (2) (3) or WB/WE (Early Write) (Late Write)	
	*1 WB/WE	*2 DSF	*3 WI/DQI(4) (New Mask)	*4 DSF	*5 WI/DQI(4) (New Mask)
Normal write	1	0	X	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask)(5)	1	0	X	1	Column Mask
Masked Block Write(5)	0	0	Write Mask	1	Column Mask
Masked Flash Write	0	1	Write Mask	X	X
Load Color Register	1	1	X	1	Color Data

Note :

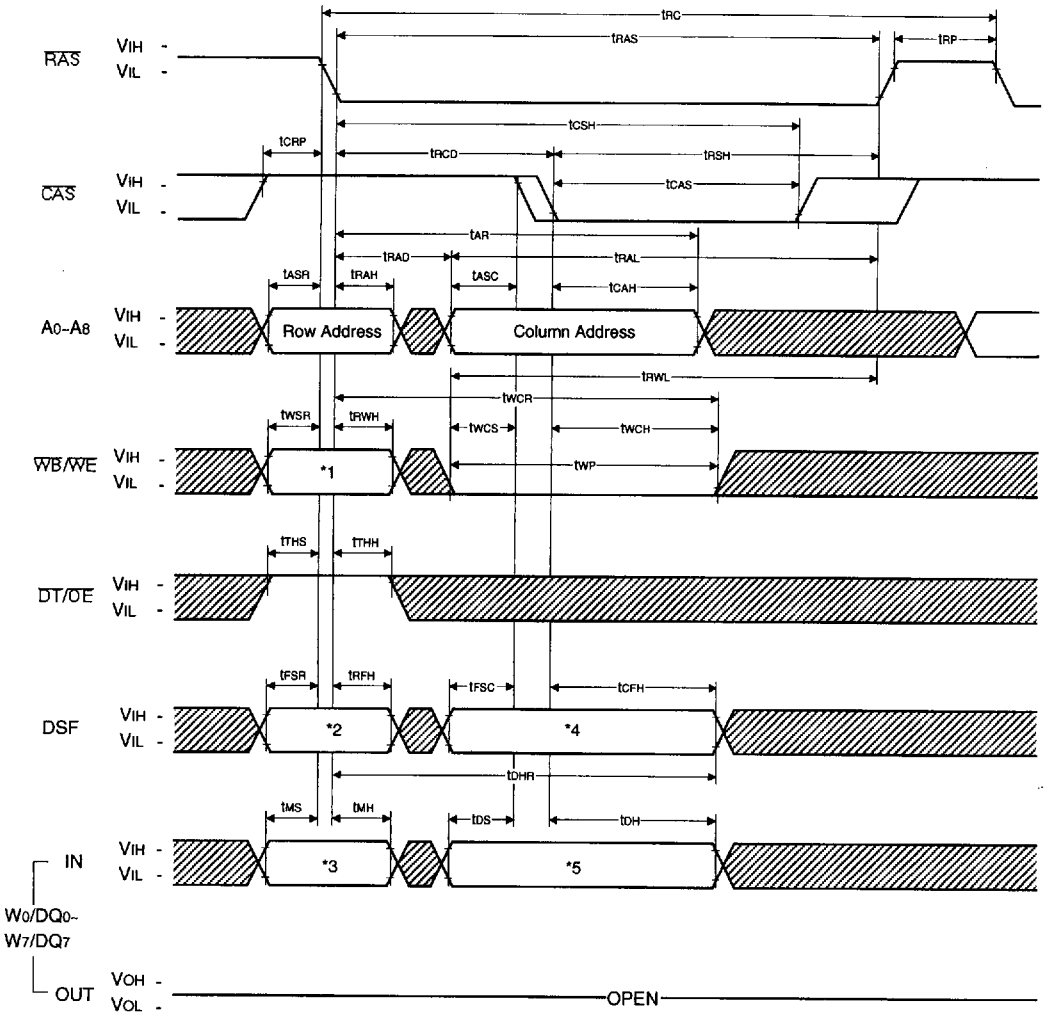
(1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram.

(2) On the Masked Flash Write cycle. all the signal inputs are "Don't Care" condition except $\overline{RAS}$ at the falling edge of $\overline{CAS}$. On the Block Write Cycles, Column Mask is latched only at the falling edge of $\overline{CAS}$ and $\overline{WB/WE}$ is "Don't Care" at the falling edge of $\overline{CAS}$.
Lately Block Write and Read Modify Block Write are not Allowed.

(3) Function table for Block Write Column Address A_0, A_1 are "Don't Care" during Block Write.

Column Address		*5	IF	
A_1	A_0	WI/DQI	WI/DQI=0	WI/DQI=1
0	0	W_0/DQ_0	No Change the Internal Data	Color Register Data are Write to the Corresponding Column Address Location
0	1	W_1/DQ_1		
1	0	W_2/DQ_2		
1	1	W_3/DQ_3		

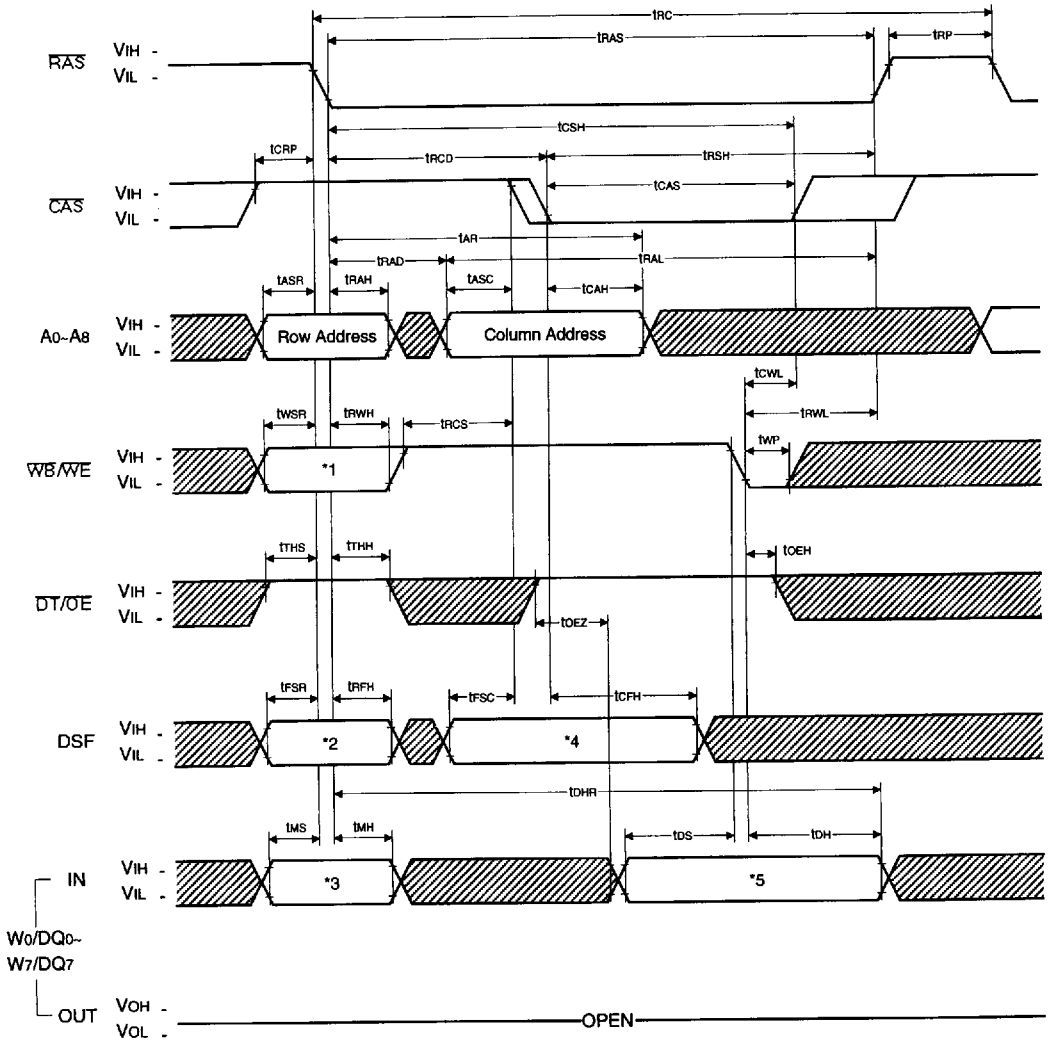
EARLY WRITE CYCLE



Note : In Block Write cycle, only Column Address A_2~A_8 are used.

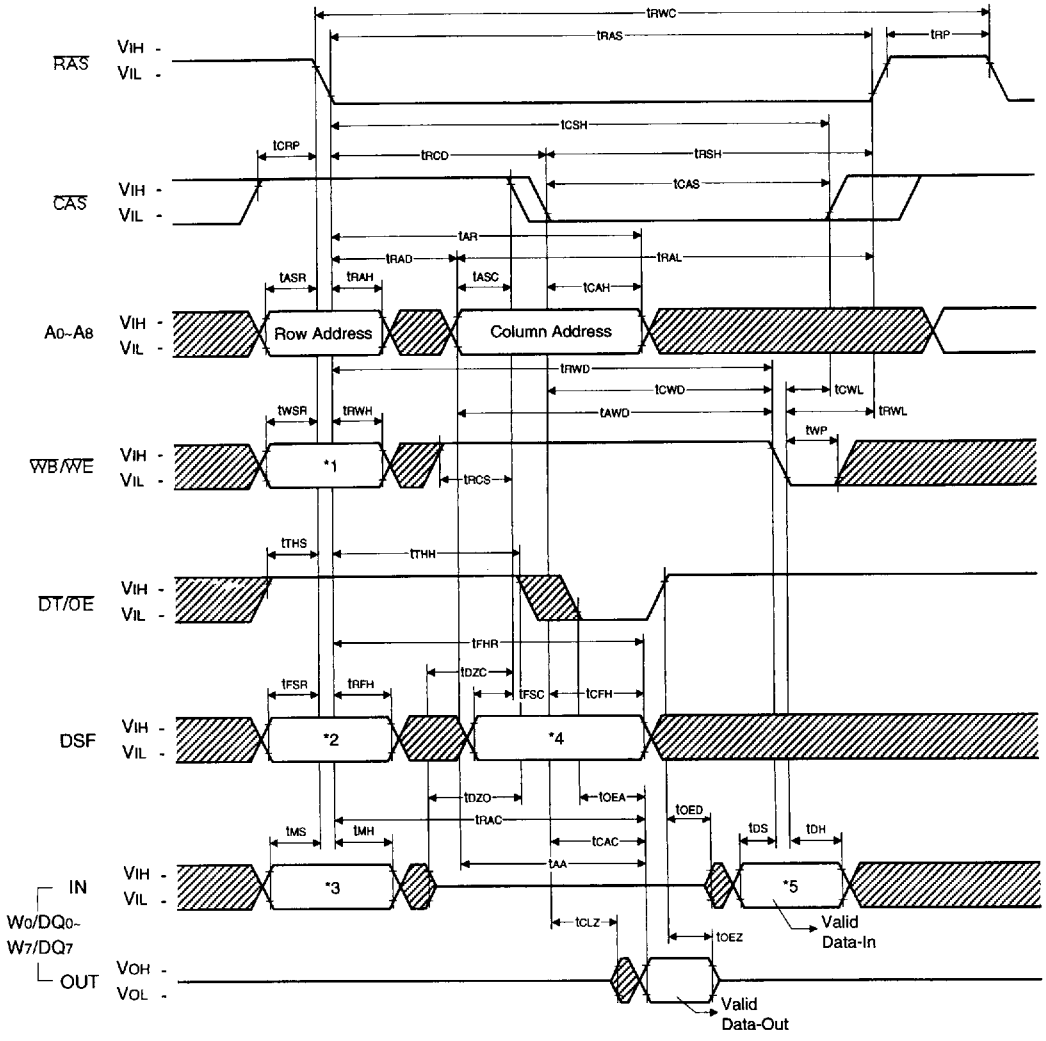
: Don't Care

LATE WRITE CYCLE



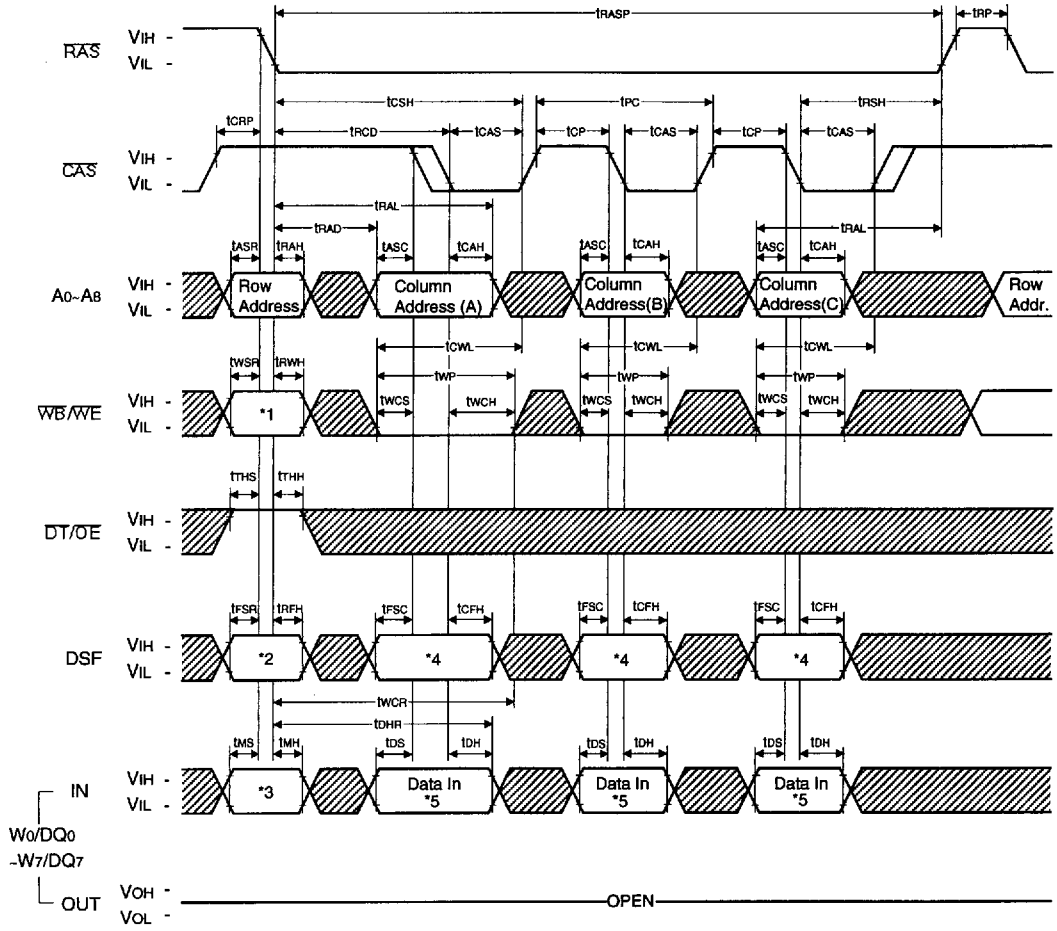
: Don't Care

READ-WRITE/READ-MODIFY-WRITE CYCLE



: Don't Care

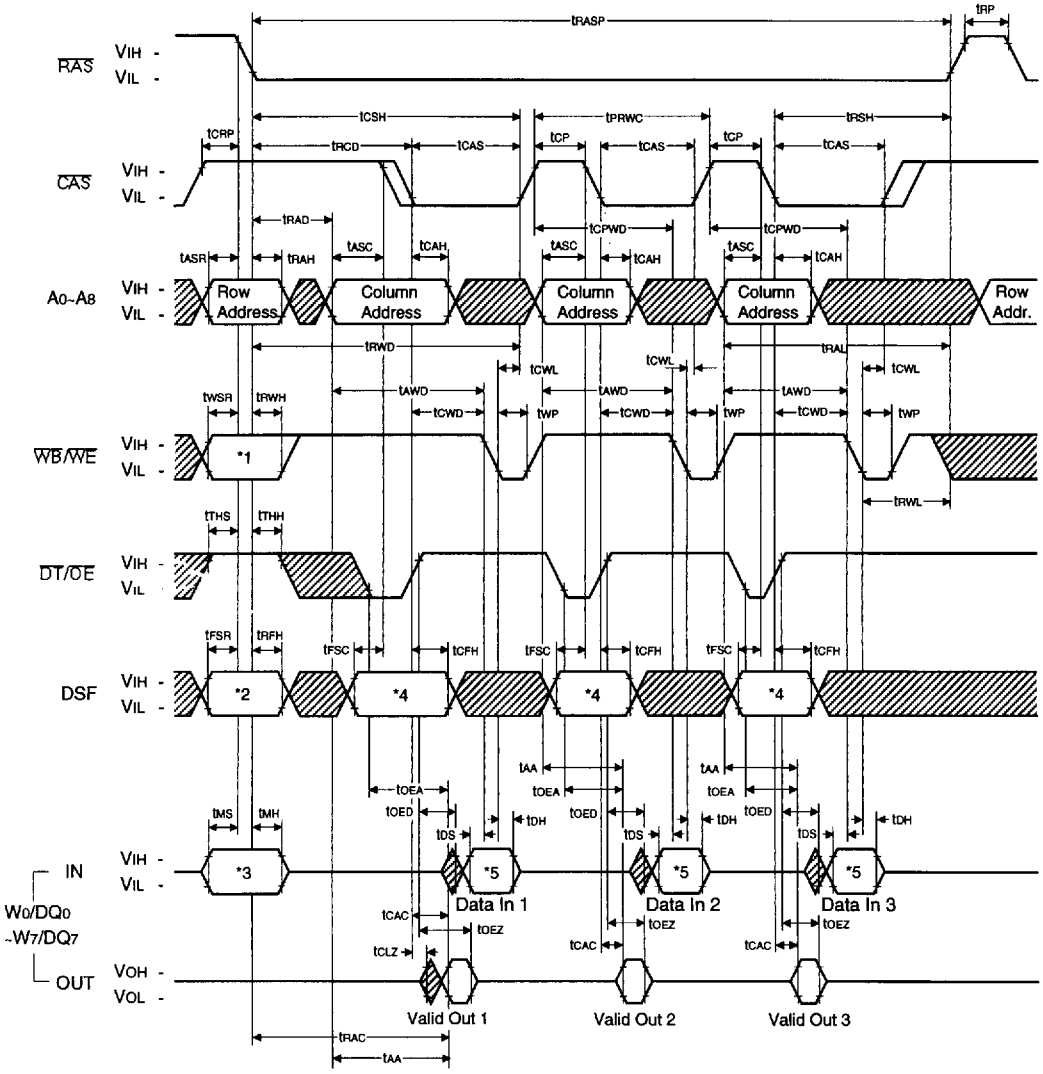
FAST PAGE MODE EARLY WRITE CYCLE



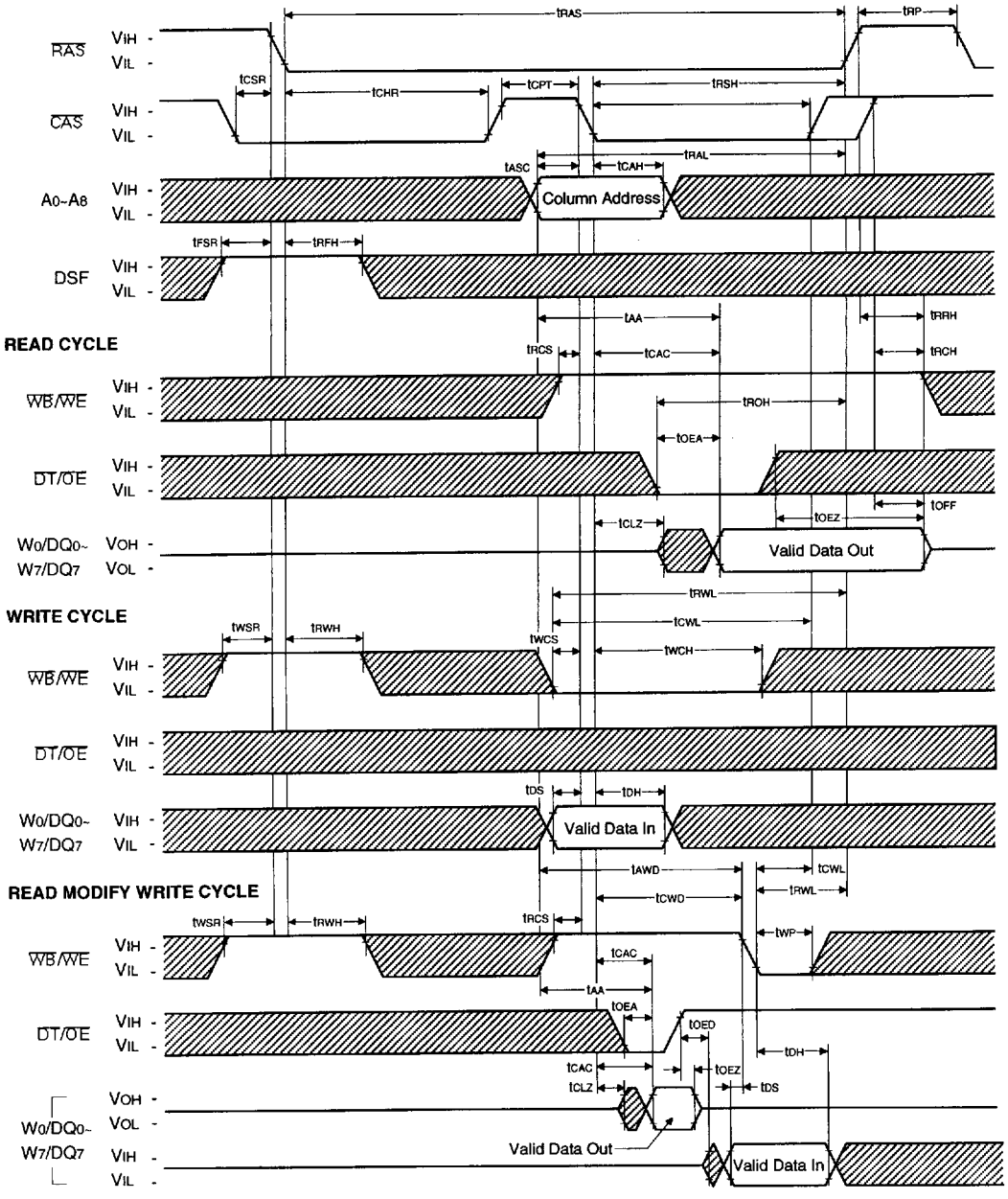
Note : In Block Write cycle, Only column address A2-A8 are used.

: Don't Care

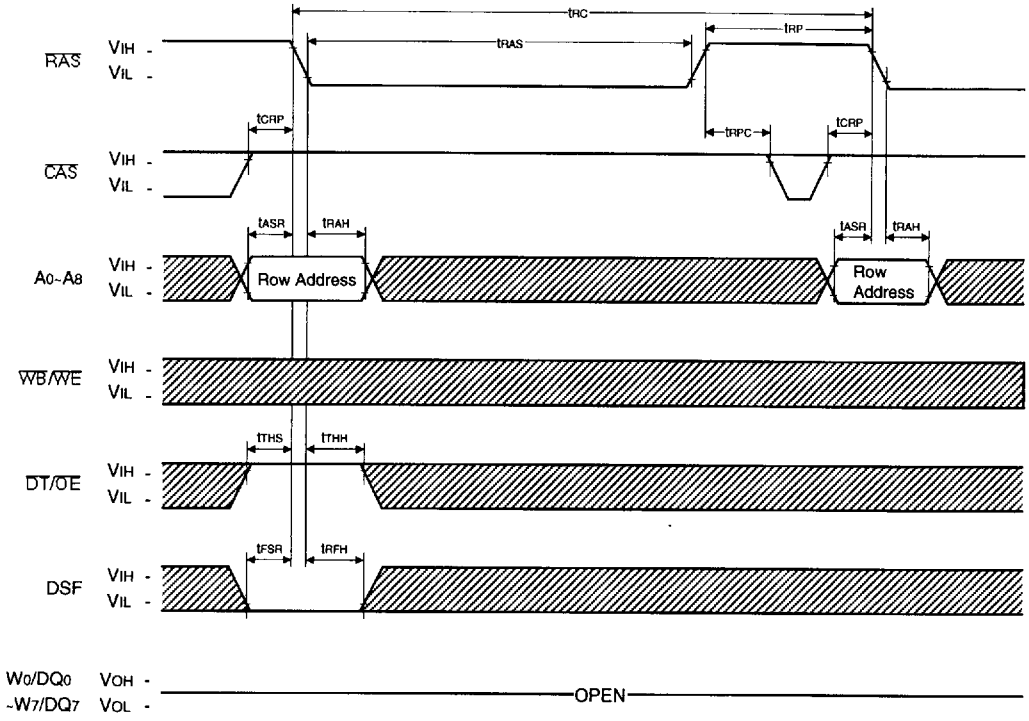
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

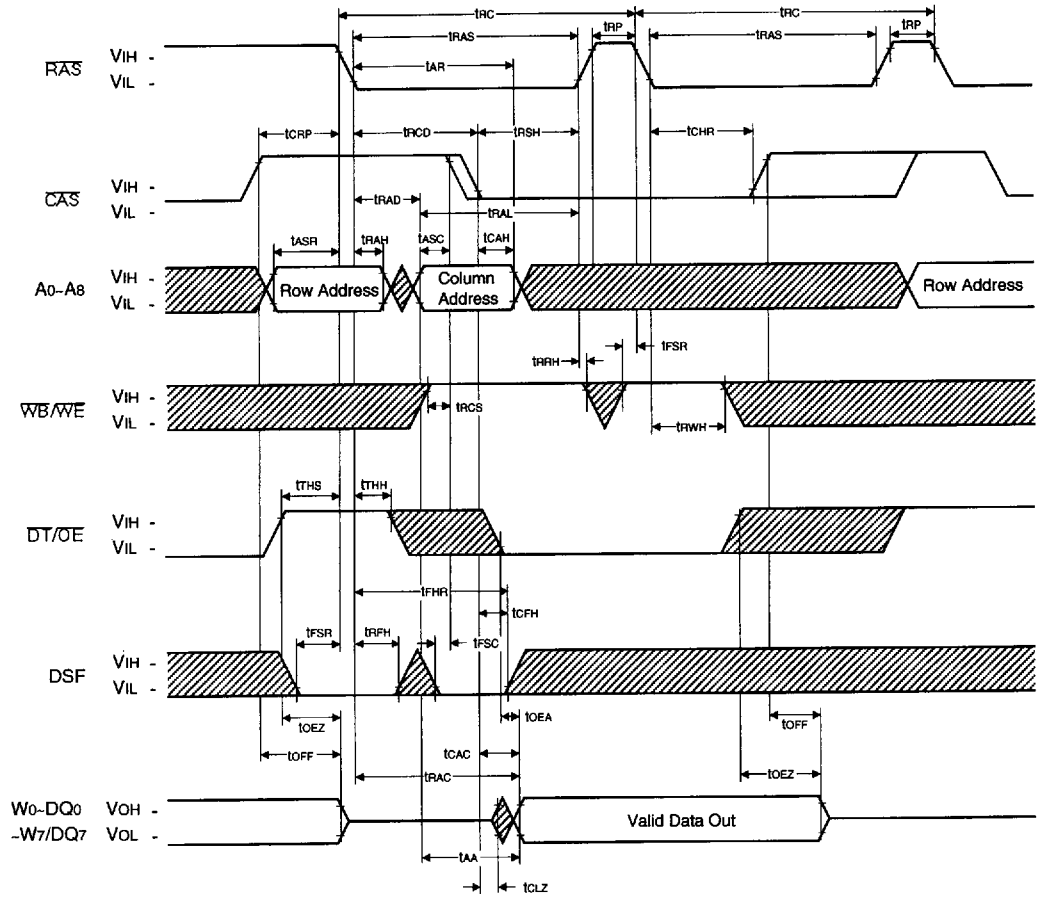


$\overline{RAS}$ ONLY REFRESH CYCLE



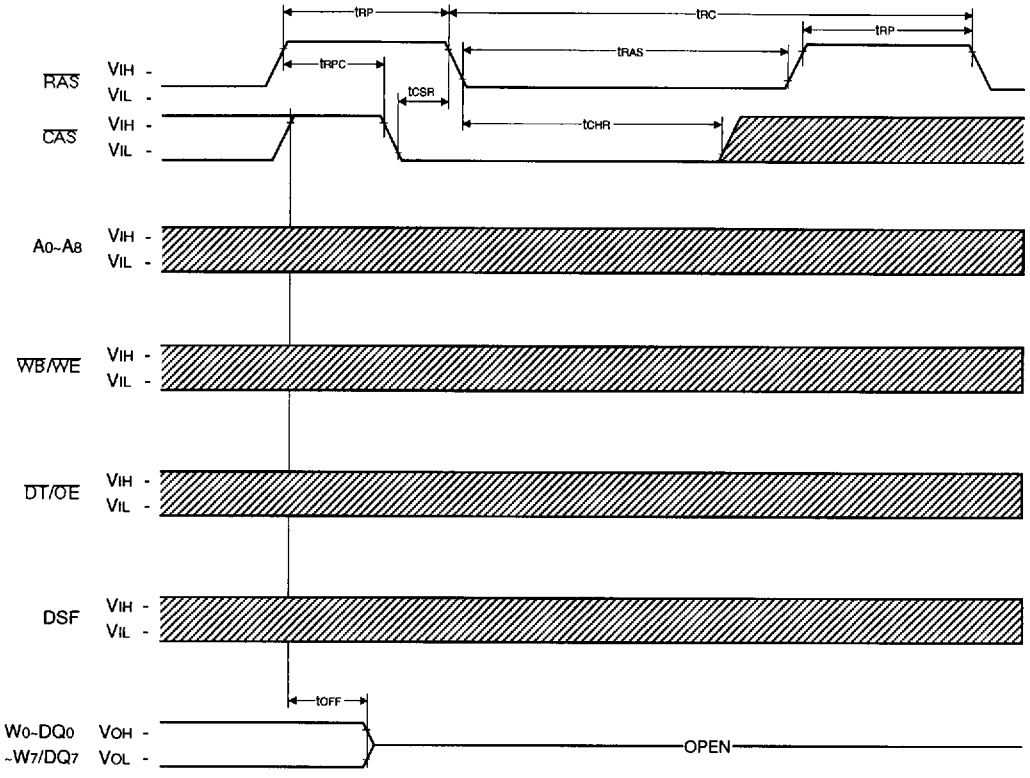
: Don't Care

HIDDEN REFRESH CYCLE



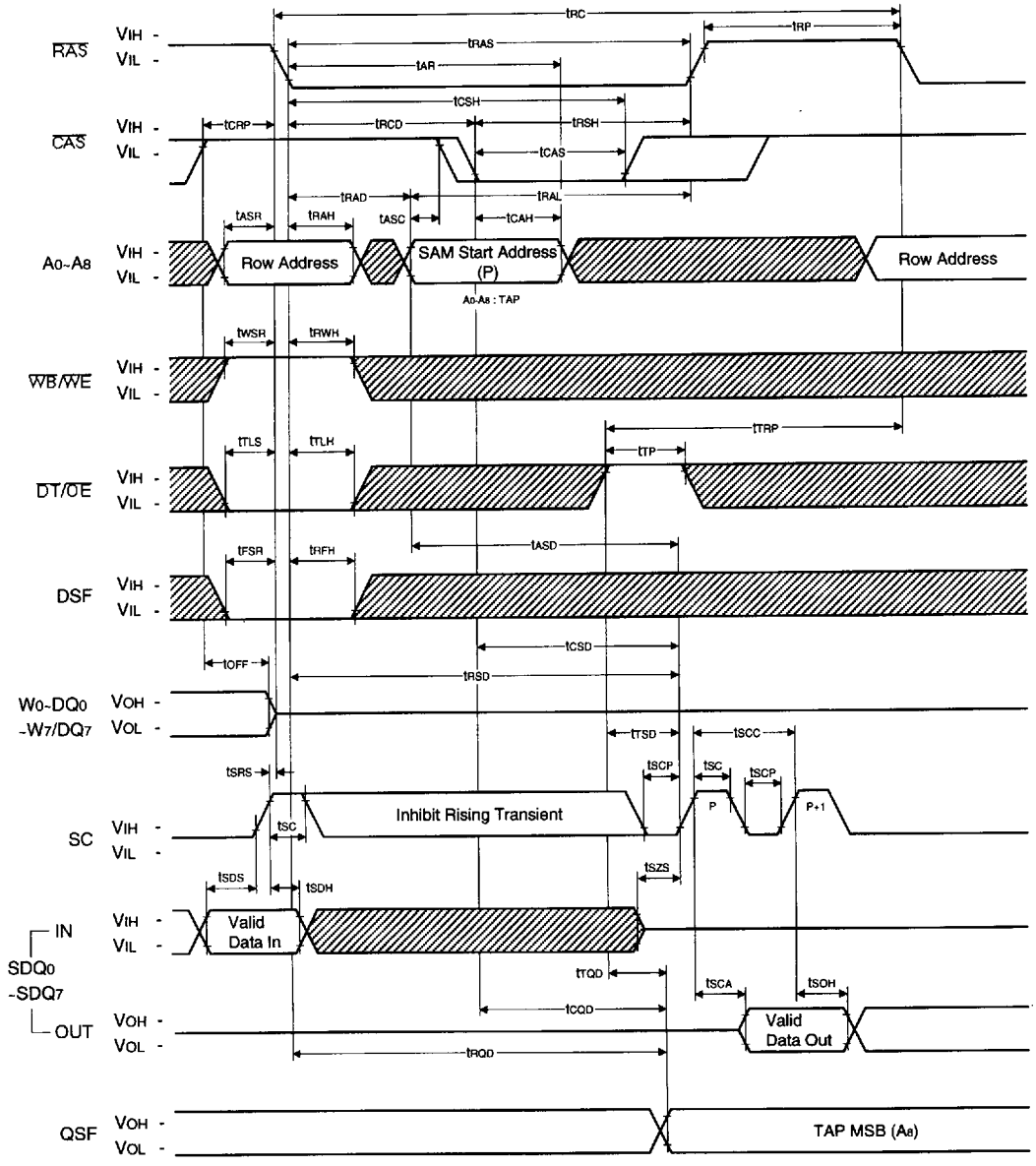
: Don't Care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



: Don't Care

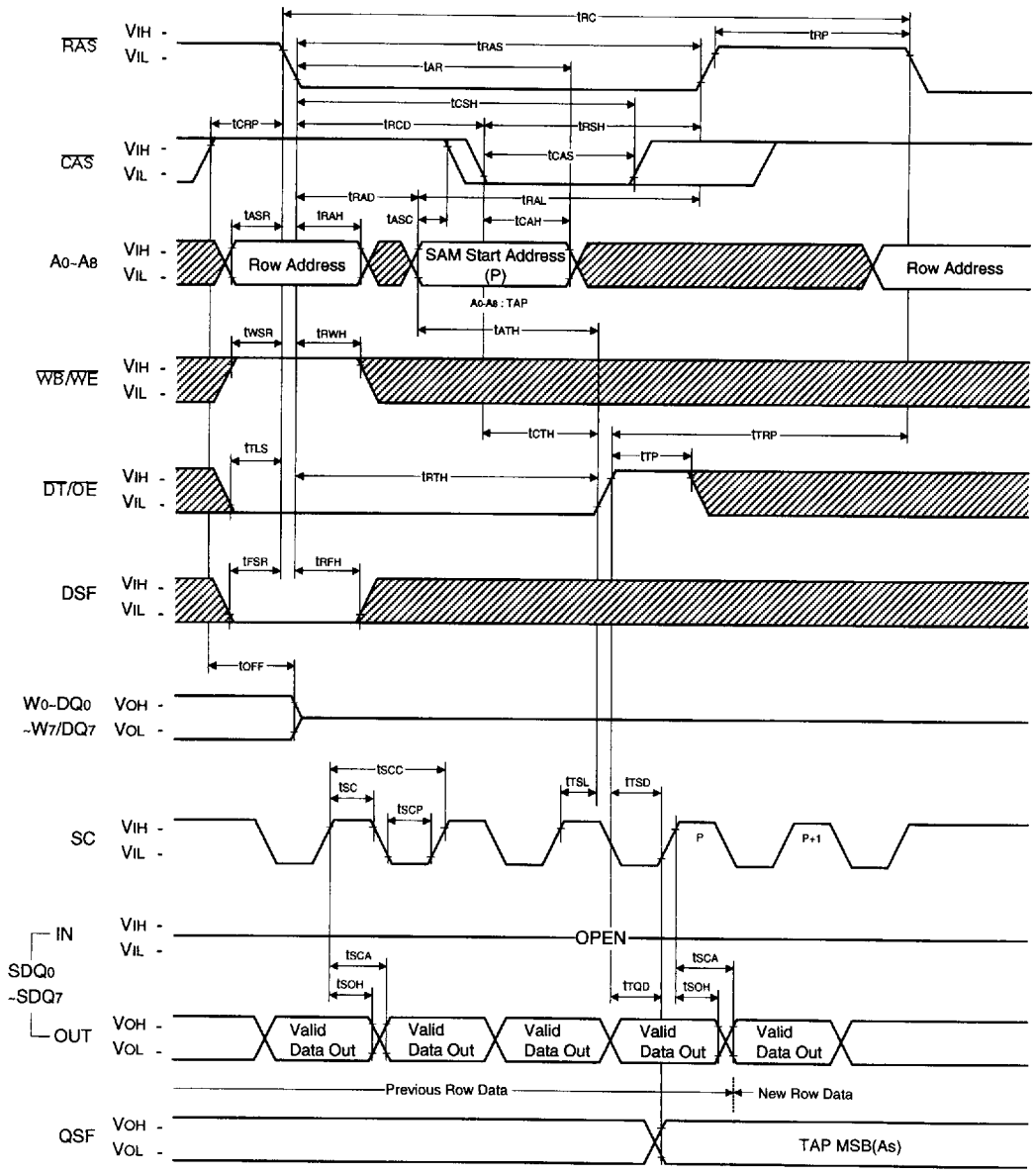
READ TRANSFER CYCLE (Previous Transfer is Write Transfer Cycle)



Note : $\overline{SE}$ = VIL

: Don't Care

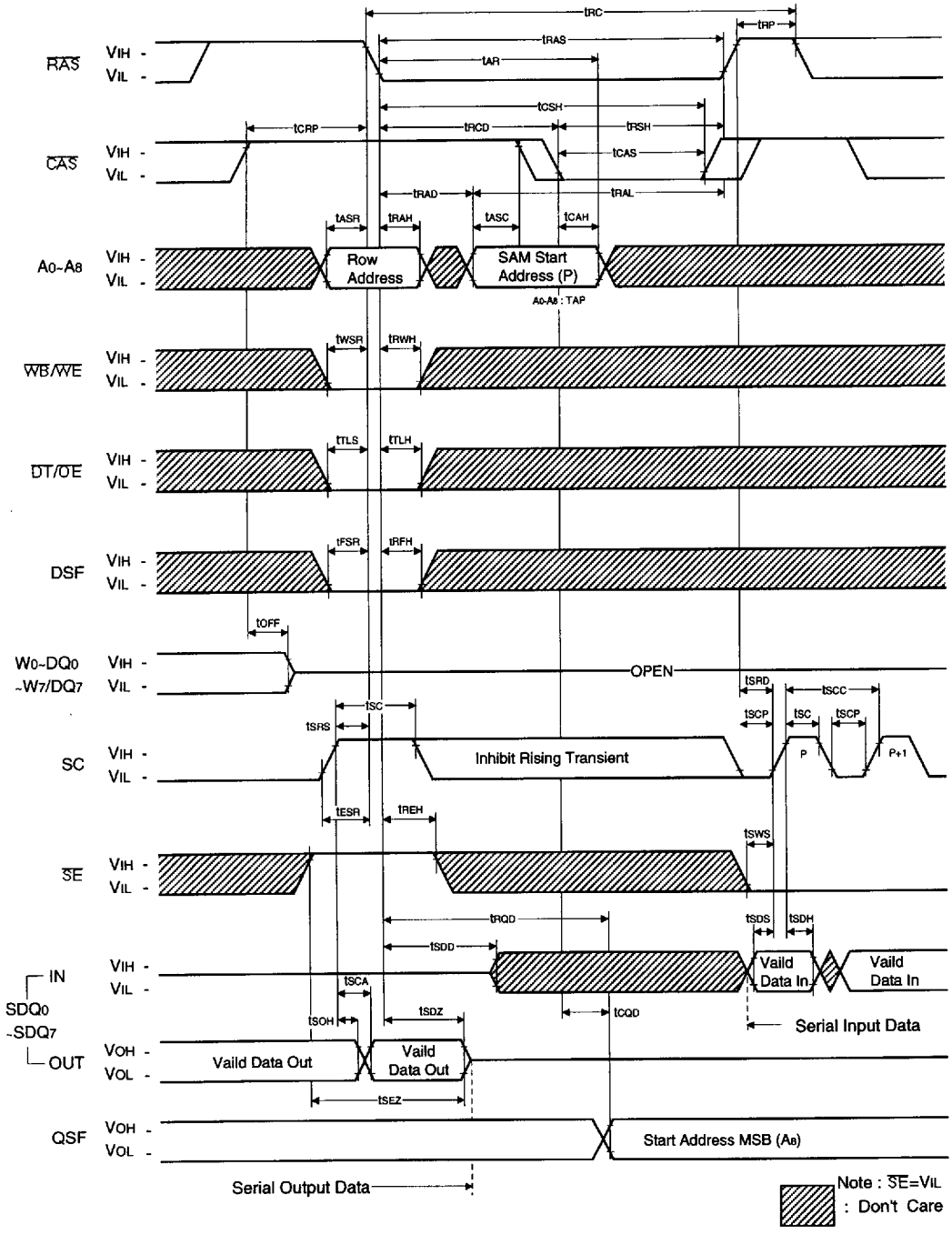
REAL TIME READ TRANSFER CYCLE



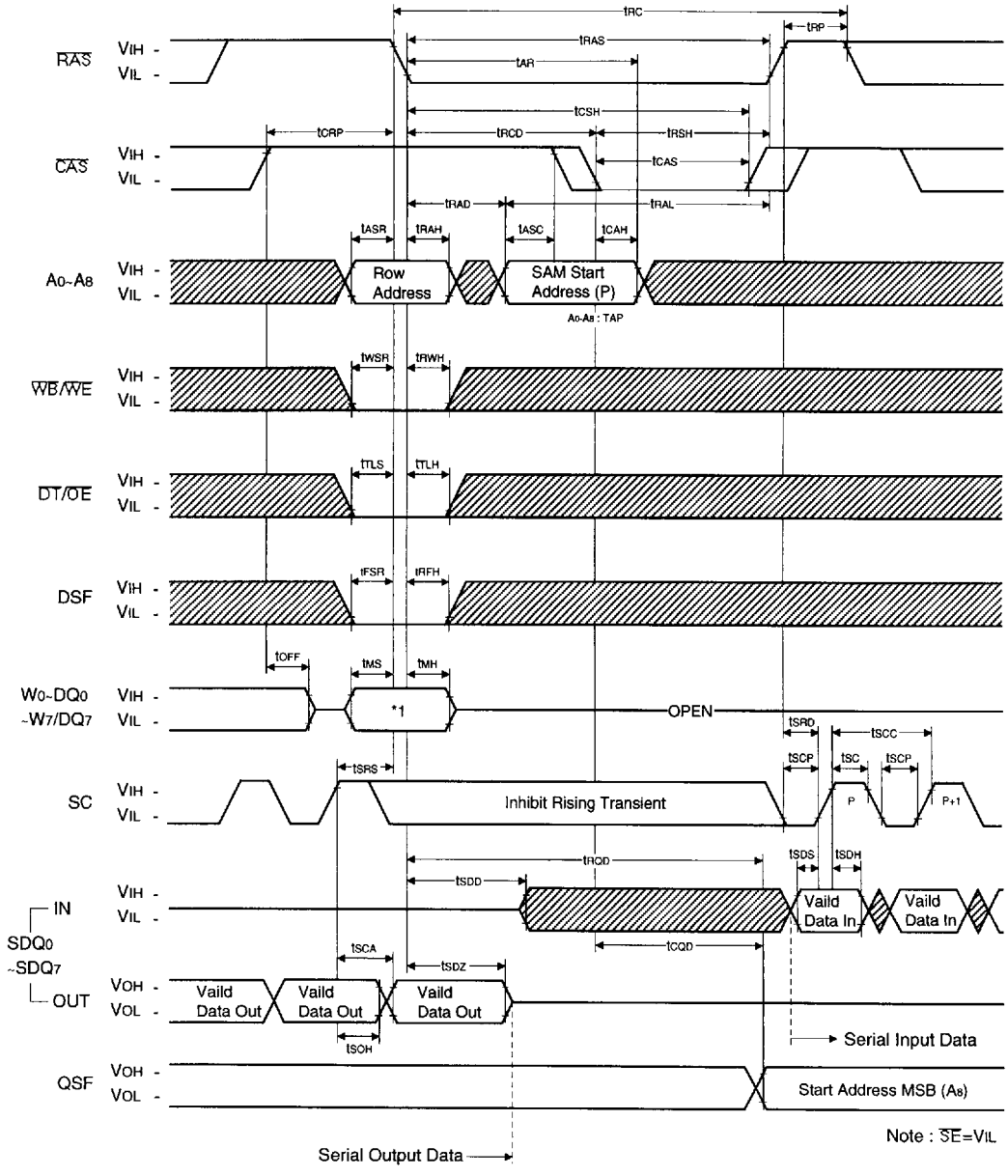
Note : $\overline{SE}$ = VIL

: Don't Care

PSEUDO WRITE TRANSFER CYCLE



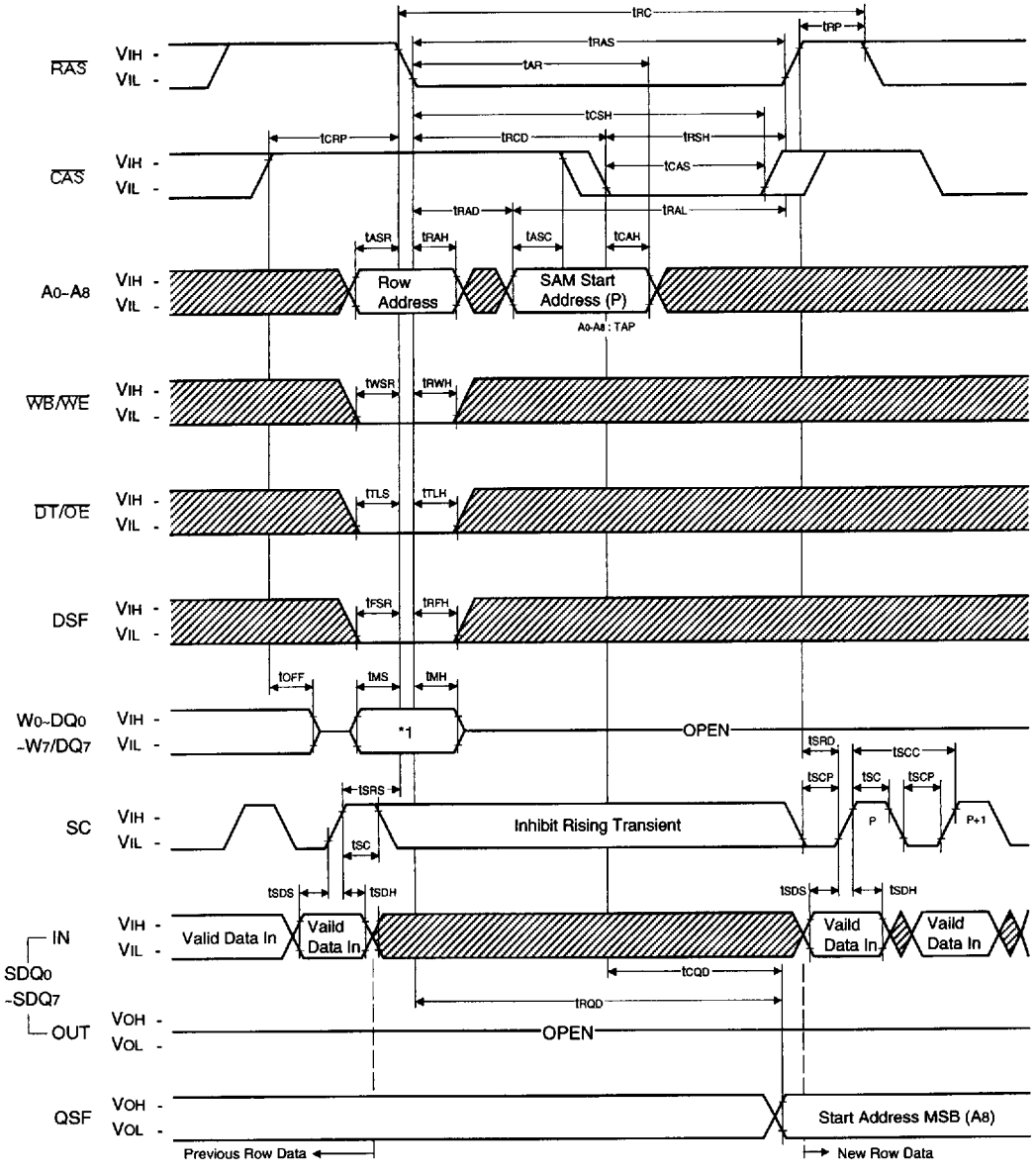
MASKED WRITE TRANSFER CYCLE (Output Mode to Input Mode Switch)



*1 WMi Data 0 : Transfer Disable
1 : Transfer Enable

: Don't Care

MASKED WRITE TRANSFER CYCLE

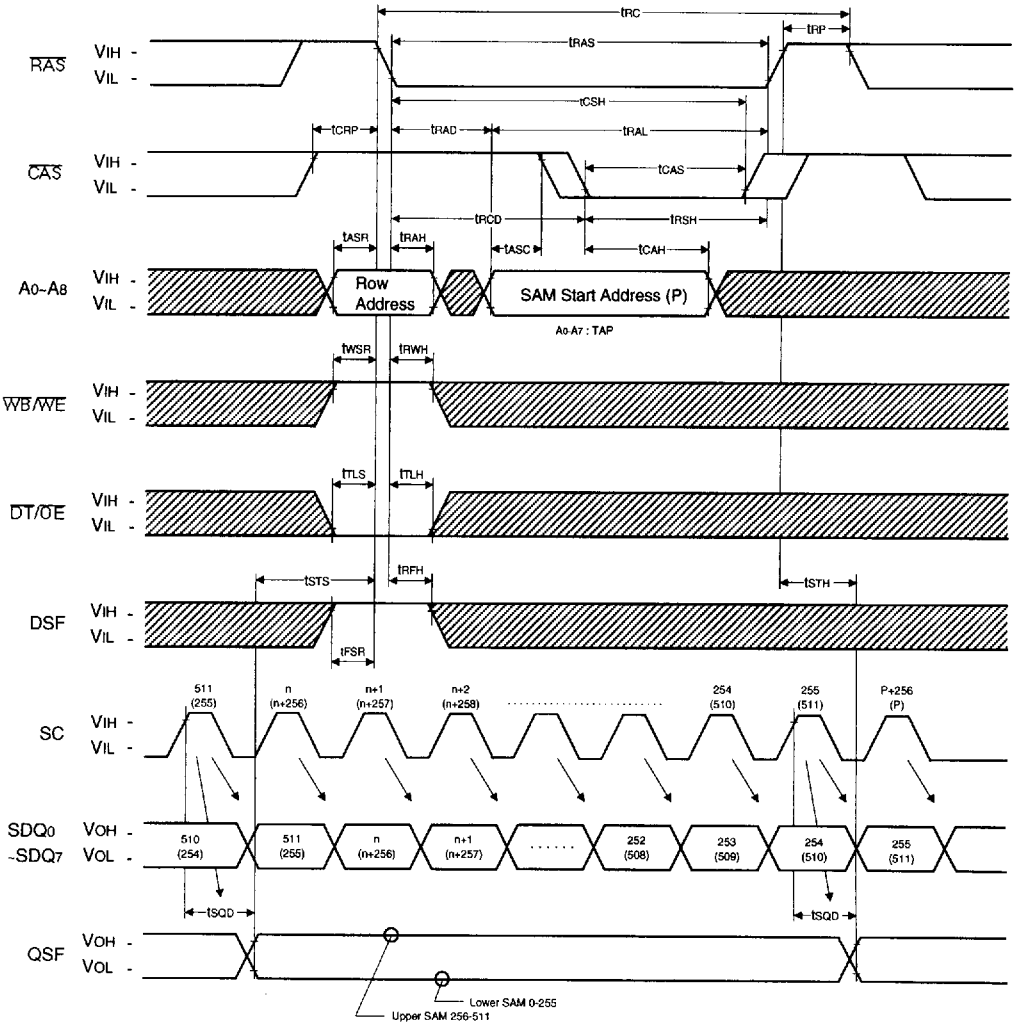


Note : $\overline{SE}$=VIL

*1 WM1 Data 0 : Transfer Disable
1 : Transfer Enable

: Don't Care

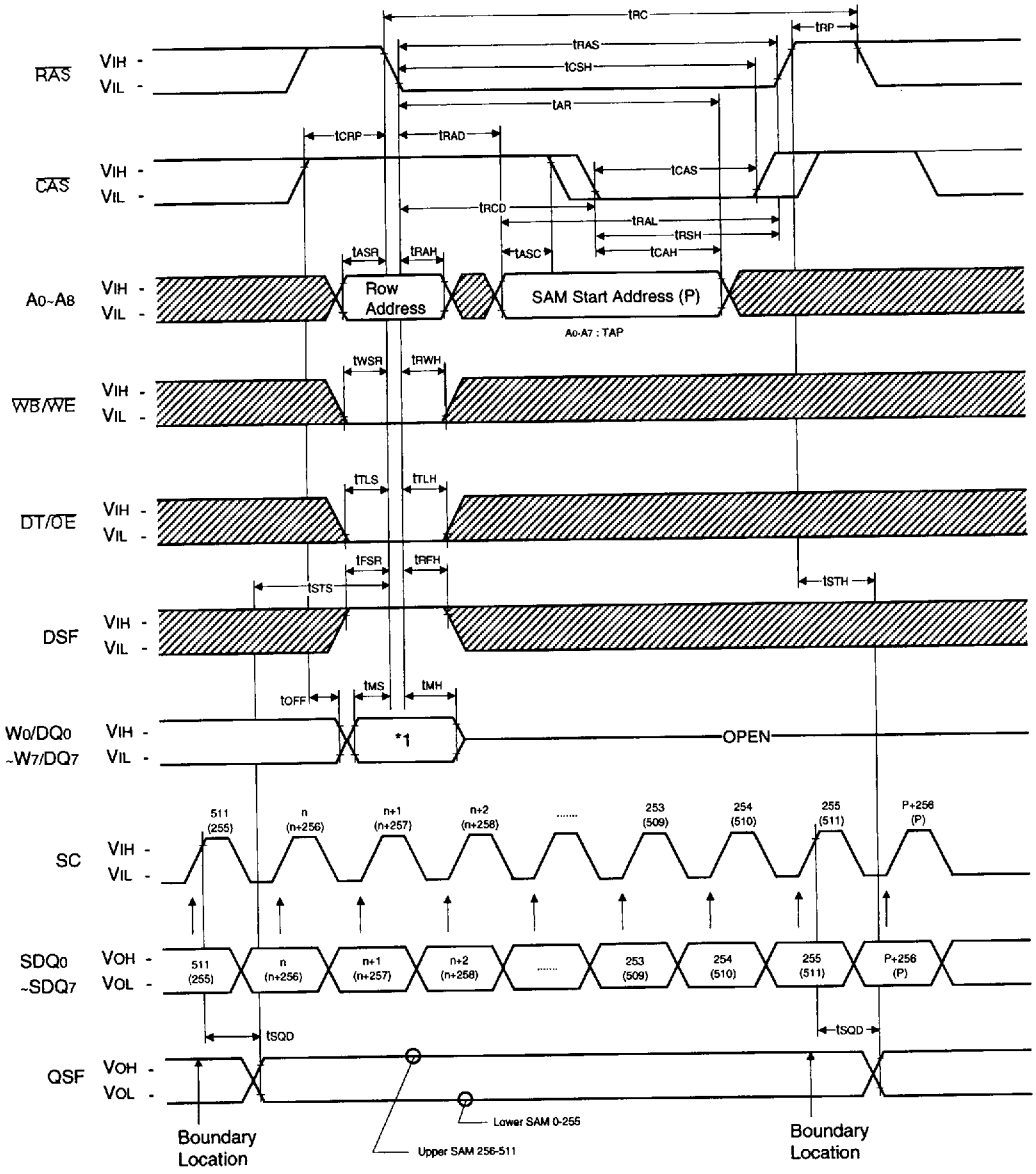
SPLIT READ TRANSFER CYCLE



Note : $\overline{SE}$=VIL

: Don't Care

MASKED SPLIT WRITE TRANSFER CYCLE

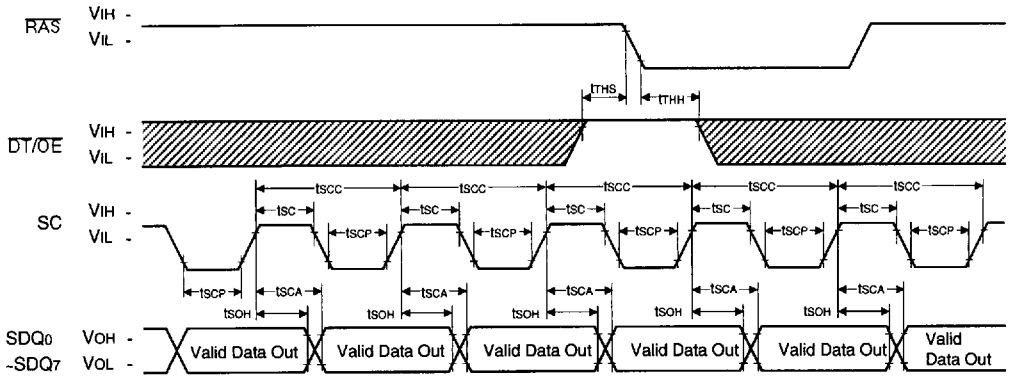


Note : $\overline{SE}$=VIL

*1 WM1 Data 0 : Transfer Disable
1 : Transfer Enable

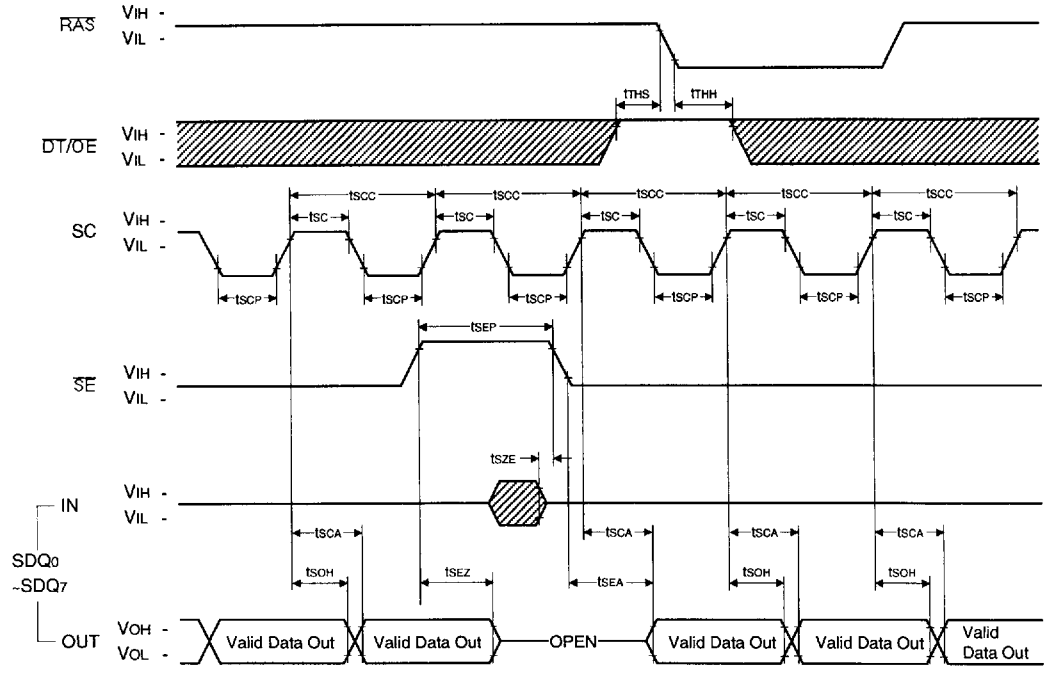
: Don't Care

SERIAL READ CYCLE ($\overline{SE}$=VIL)



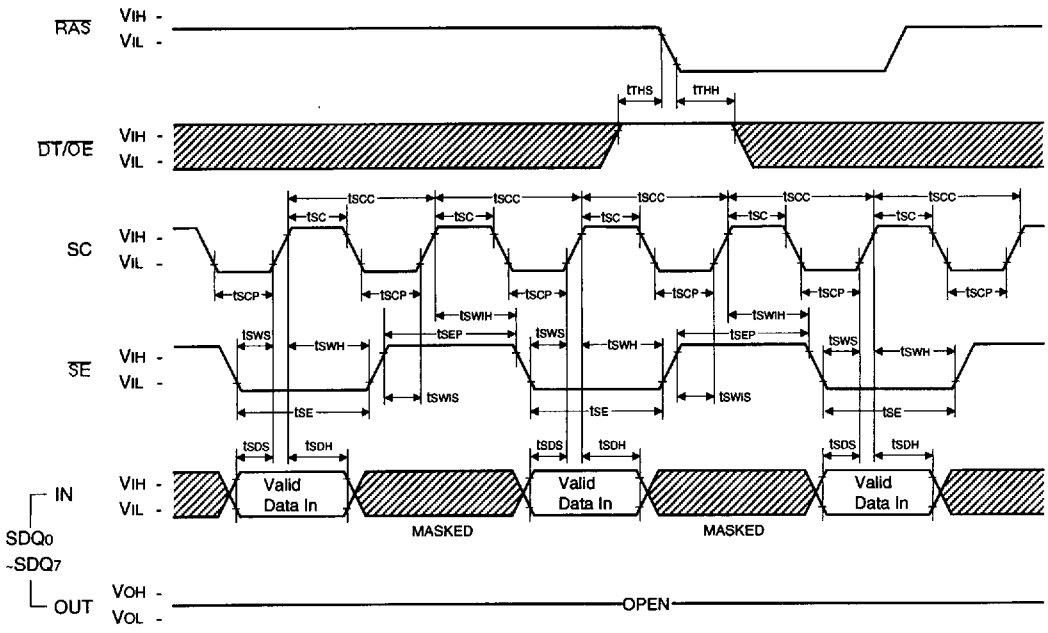
Note : $\overline{SE}$ = VIL

SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)

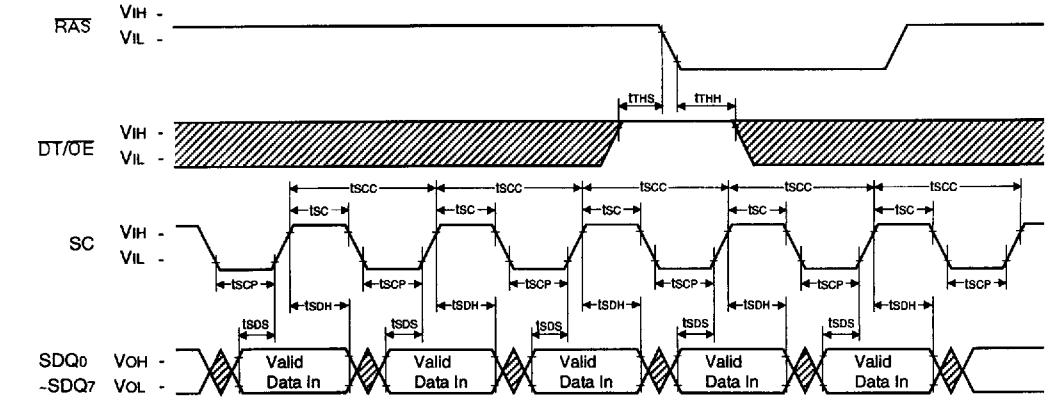


: Don't Care

SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



SERIAL WRITE CYCLE ($\overline{SE}$ = VIL)



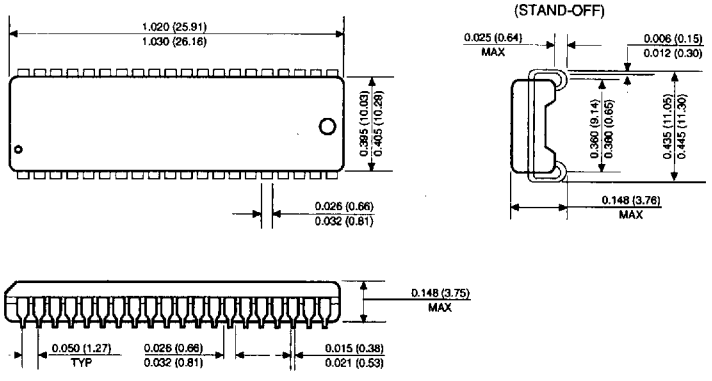
Note : $\overline{SE}$ = VIL

: Don't Care

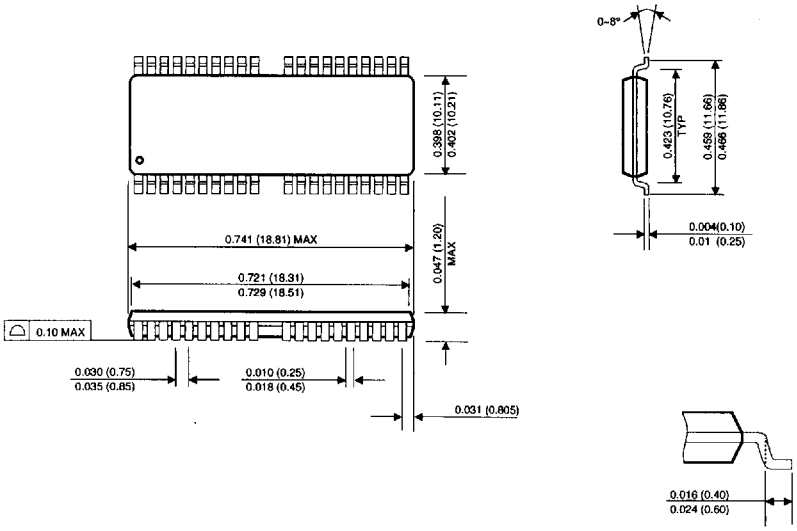
PACKAGES DIMENSION

40-PIN PLASTIC SOJ

Unit : Inches (millimeters)



40/44-PIN PLASTIC TSOP-II (Forward Type)



PACKAGES DIMENSION

64-PIN Plastic Shrink Small Out Line Package

Unit : Inches (millimeters)