

IMS 2630

8Kx8

IMS 2620

16Kx4

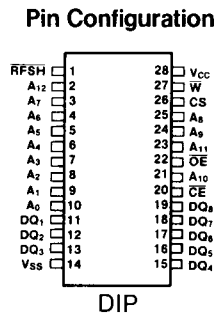
IMS 2600

64Kx1

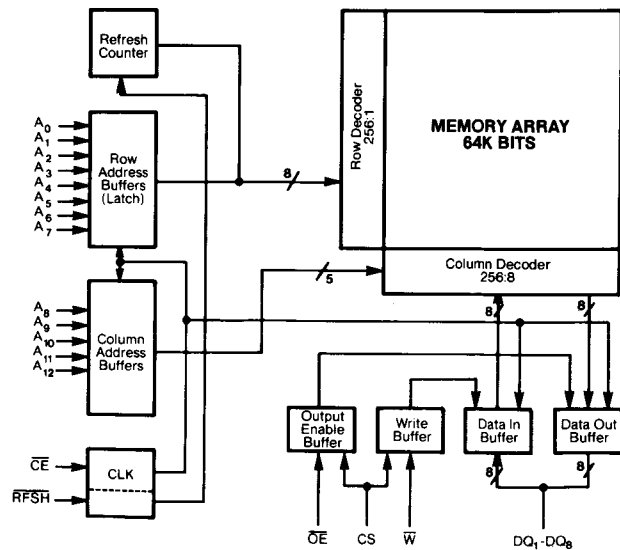
Features

- Byte wide 64K memory
- CE access times of 120 and 150ns
- Cycle times of 190 and 240ns
- Non-multiplexed addressing
- On chip refresh counter for pin 1 hidden refresh
- 4ms, 256 cycle refresh
- Low power 300mW active
30mW standby
- JEDEC standard pinout for byte wide memory devices

Pin Names	
A ₀ -A ₁₂	ADDRESS INPUTS
CE	CHIP ENABLE
CS	CHIP SELECT
W	WRITE ENABLE
OE	OUTPUT ENABLE
DQ ₀ -DQ ₇	DATA IN/DATA OUT
V _{CC}	+5V SUPPLY
V _{SS}	GROUND
RFSH	REFRESH ENABLE



Block Diagram



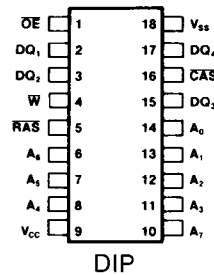
Features

- High performance 16Kx4 dRAM
- RAS Access of 100, 120 and 150ns
- Cycle times of 160, 190 and 230ns
- OE control for high speed access
- On chip refresh assist using $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$
- 4ms, 256 cycle refresh
- 25 Mbit data rate

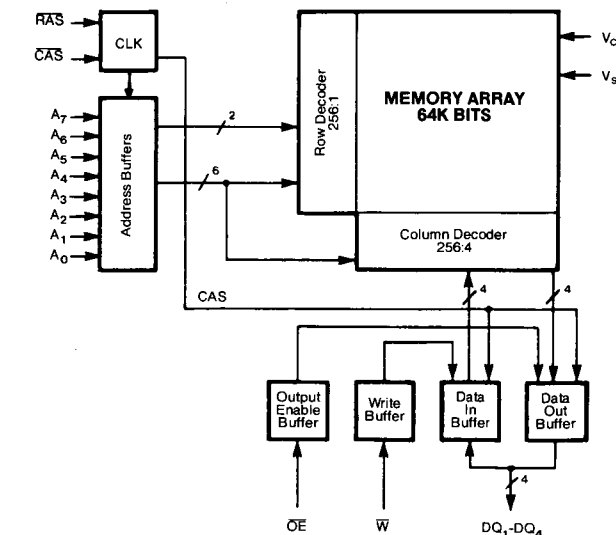
Pin Names	
A ₀ -A ₇	ADDRESS INPUTS
CAS	COLUMN ADDRESS STROBE
RAS	ROW ADDRESS STROBE
DQ ₁ -DQ ₄	DATA IN/DATA OUT
OE	OUTPUT ENABLE
W	WRITE ENABLE
V _{CC}	+5V SUPPLY
V _{SS}	GROUND

*Row Addresses A0-A7
Column Address A1-A6

Pin Configuration



Block Diagram

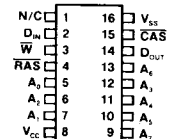


Features

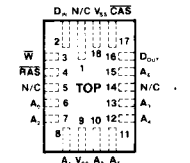
- $\overline{\text{RAS}}$ access of 100, 120 and 150ns
- Random Read and Write cycle times of 160, 190 and 230ns
- On chip refresh assist using $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$
- 4ms, 256 cycle refresh
- 55, 65 and 75ns Read or Write cycle in Nibble Mode
- Indefinite D_{OUT} hold under $\overline{\text{CAS}}$ control
- High performance 64Kx1 dRAM

Pin Names	
A ₀ -A ₇	ADDRESS INPUTS
CAS	COLUMN ADDRESS STROBE
RAS	ROW ADDRESS STROBE
D _{IN}	DATA IN
D _{OUT}	DATA OUT
W	WRITE ENABLE
V _{CC}	+5 VOLT SUPPLY INPUT
V _{SS}	GROUND

Pin Configuration

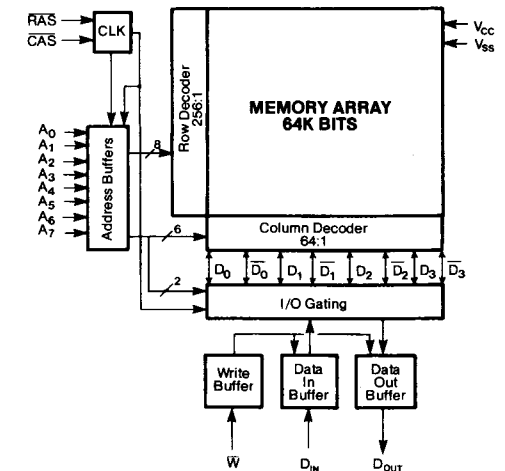


DIP

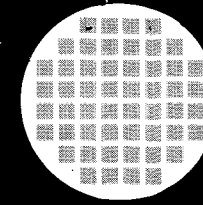


Chip Carrier

Block Diagram

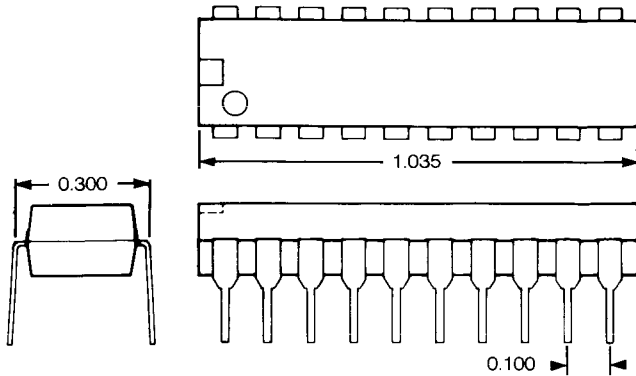


Device Packaging

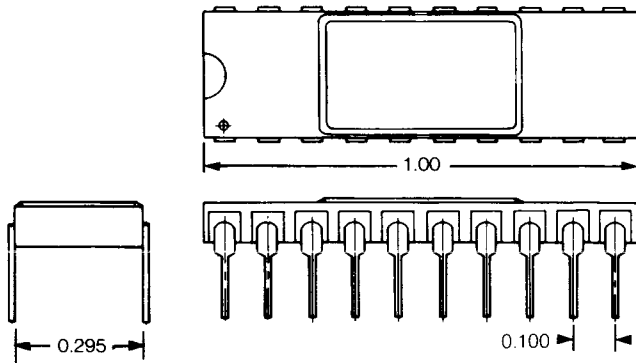


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STATIC RAM

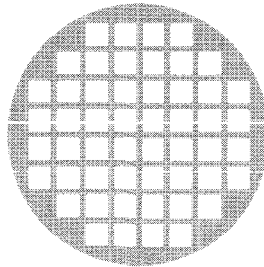
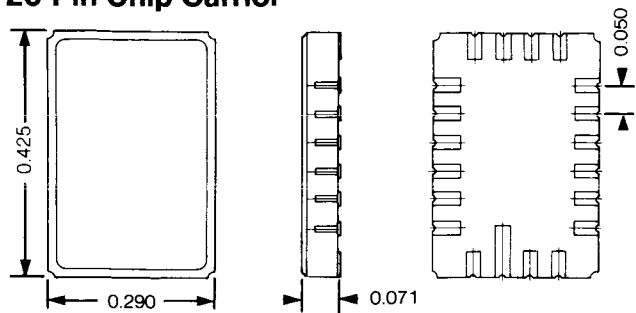
20 Pin Plastic Dual-in-Line



20 Pin Ceramic Dual-in-Line



20 Pin Chip Carrier



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