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CHAPTER 1 SPECIFICATIONS

(FB-500 Series)

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CHAPTER 1 SPECIFICATIONS

1-1 Major Specifications

Model Name				FB-501	FB-502	FB-503	FB-504
Type				Single-side	Single-side Double-track	Double-side	Double-side Double-track
Items			Unit				
Memory Capacity (MFM)	Unformatted Per Disk		Bytes	250K	500K		1M
	Formatted Per Disk		Bytes	164K	328K		656K
Media	Basic Format	Bytes/Sectors	Bytes	256			
		Sectors/Track		16 (Soft Sector)			
	Track Radius	OD	mm	57.151			
		ID	mm	36.514	36.249	34.396	34.131
	Number of Recording Sides			1		2	
	Number of Cylinders			40	80	40	80
	Number of Tracks			40	80		160
	Index			1			
Recording	Recording Method			FM/MFM			
	Packing Density		BPI	5536	5576	5876	5922
	Track Density		TPI	48	96	48	96
	Data Transfer Speed		Bits/sec	125K/250K			
Access Time	Average Latency		msec.	100			
	Seek Time		msec	6	3	6	3
	Settling Time		msec.	15	15	15	15
	Average Access Time		msec.	88			
	Head Load Time		msec.	———		Option (35ms)	
	Motor Starting Time		msec.	500			
Spindle Speed			RPM	300			

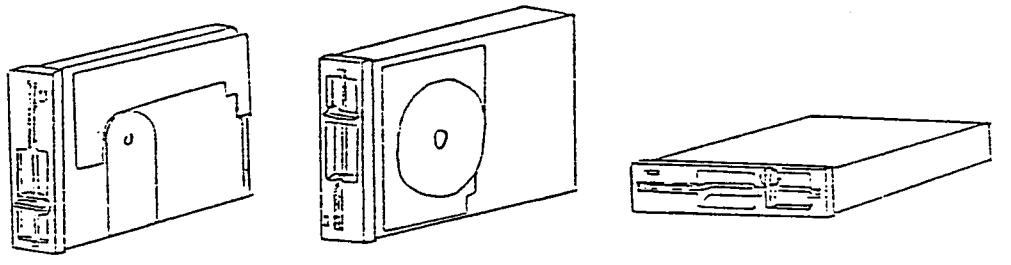
This drive has been designed conforming to the media specified in ISO, ANSI, ECMA, and JIS.

1-2 Mechanical Dimensions and Installation

(1)	Width	146mm (5.75 Inches)
(2)	Height	41mm (1.61 Inches)
(3)	Depth	204mm (8.03 Inches)
(4)	Dimensions	See Fig. 1-2
(5)	Weight	1.4Kg
(6)	Cooling System	Natual Air Cooling
(7)	Installation	3 Ways (See Fig. 1-1)

1. Vertical Mount: LED lamp up or down. [Fig (a) or (b)]

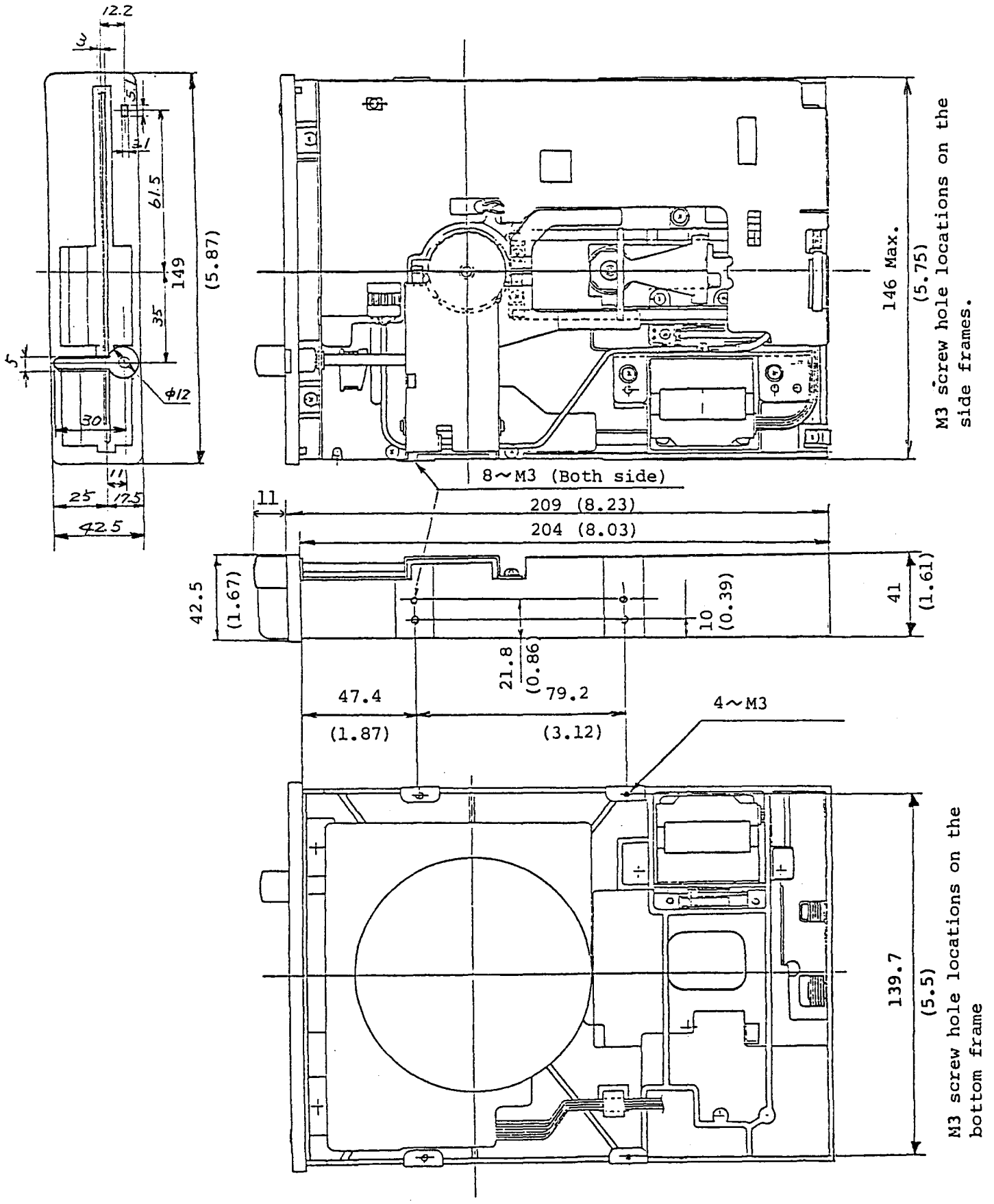
2. Horizontal Mount: Drive Motor down. [Fig (c)]



(a) (b) (c)

Fig. 1-1 Installation

NOTE: Use the mounting holes in the side frames or bottom frame of the FDD with M3 screws. (See Fig. 1-2)



NOTE: All dimensions are in mm.

Dimensions in ( ) are in inches.

~~Fig. 1-2 Dimensions~~

1-3 Physical Specifications

(1) Ambient Temp.

(a)	Operating	5 to 45°C (10 to 52°C for media. Refer to the ISO Specifications).
(b)	Shipping	-40 to 60°C
(c)	Storage	-22 to 53°C

(2) Relative Humidity

(a)	Operating	20 to 80%RH (Non-condensing)
(b)	Non-operating	8 to 90%RH (Non-condensing)
(c)	Max Wet-bulb Temp.	29°C (84°F)

(3) Vibration

(a)	Operating	Acceleration	: Less than 0.25G (10~25Hz)
(b)	Shipping	Acceleration	: Less than 2G (Less than 100Hz)

(The unit must be packaged as per the TEC standard.)

(4) Shock

(a)	Shipping	Acceleration	: Less than 40G (Less than 10ms)

(The unit must be packaged as per the TEC standard.)

(5) Dust

The drive should not be used in a dusty location.

1-4 Power Requirements

(1) +12V DC

(a)	Tolerance	:	±5%
(b)	Ripple Voltage	:	Less than 100mV P-P
(c)	Average Load Current	:	Approx. 0.7A (with head load mechanism) 0.5A (without head load mechanism)
(d)	Surge Current	:	1A (200msec at spindle motor start-up)

(2) +5V DC

(a)	Tolerance	:	±5%
(b)	Ripple Voltage	:	Less than 50mV P-P
(c)	Average Load Current	:	Approx. 0.5A
(d)	Max. Load Current	:	Less than 0.7A

1-5 Reliability

(1)	Mean Time Between Failures (MTBF)	:	10000 Power On Hours
(2)	Mean Time to Repair (MTTR)	:	30 minutes
(3)	Error Rates		
(a)	Soft Read Errors	:	Less than one error per 10^9 bits read.
(b)	Hard Read Errors	:	Less than one error per 10^{12} bits read.
(c)	Seek Errors	:	Less than one error per 10^6 seeks
(4)	Media Life	:	More than 3×10^6 passes/track
(5)	Media Insertions	:	More than 3×10^4 times

CHAPTER 2 CONSTRUCTIONS

The unit consists of the following components.

2-1 Magnetic Head

The single-side magnetic head uses a button type head and the double-side magnetic head uses a gimbal type, both using the tunnel erase method.

2-2 Head Positioning Mechanism

The head is positioned by the rotation of the stepping motor through the steel belt.

2-3 Head Load Mechanism for double-sided type only (Option)

The mechanical method by a small solenoid and return spring.

2-4 Disk Drive Mechanism

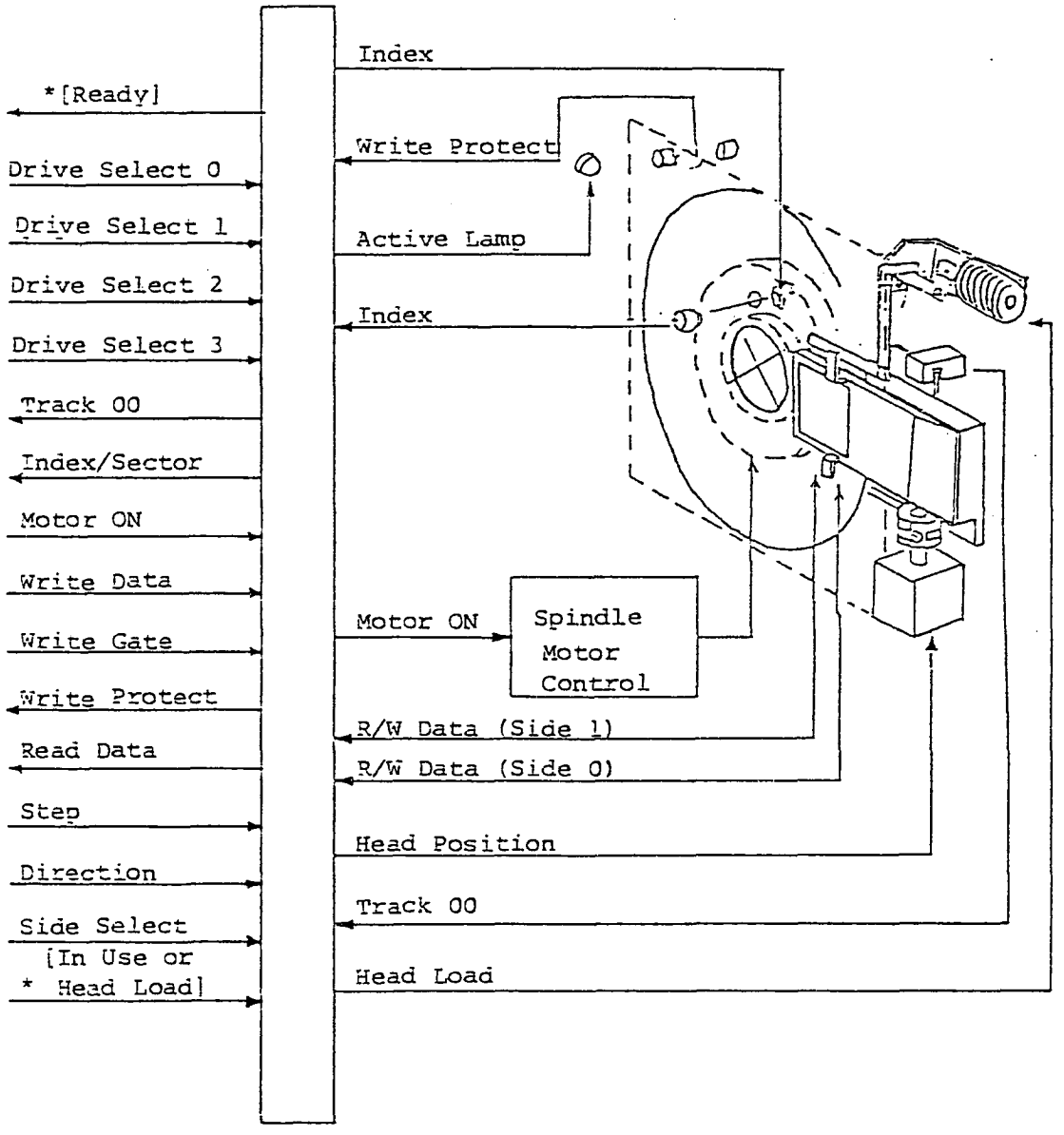
The diskette rotation mechanism uses the DC brushless direct-drive motor to directly rotate the spindle at 300rpm.

2-5 Read/Write and Control Electronics

The read/write and control electronics include the following circuits.

(1) Index/sector detection circuit
(2) Drive circuit for head-load solenoid
(3) Drive circuit for head positioning stepping motor
(4) Track 00 detection circuit
(5) Write enable notch detection circuit
(6) Read-write circiut
(7) Drive select circuit
(8) Side select circuit
(9) Spindle motor control circuit

The diagram for read/write and control electronics is shown in Fig. 2-2.



* Option

Fig. 2-1 Block Diagram

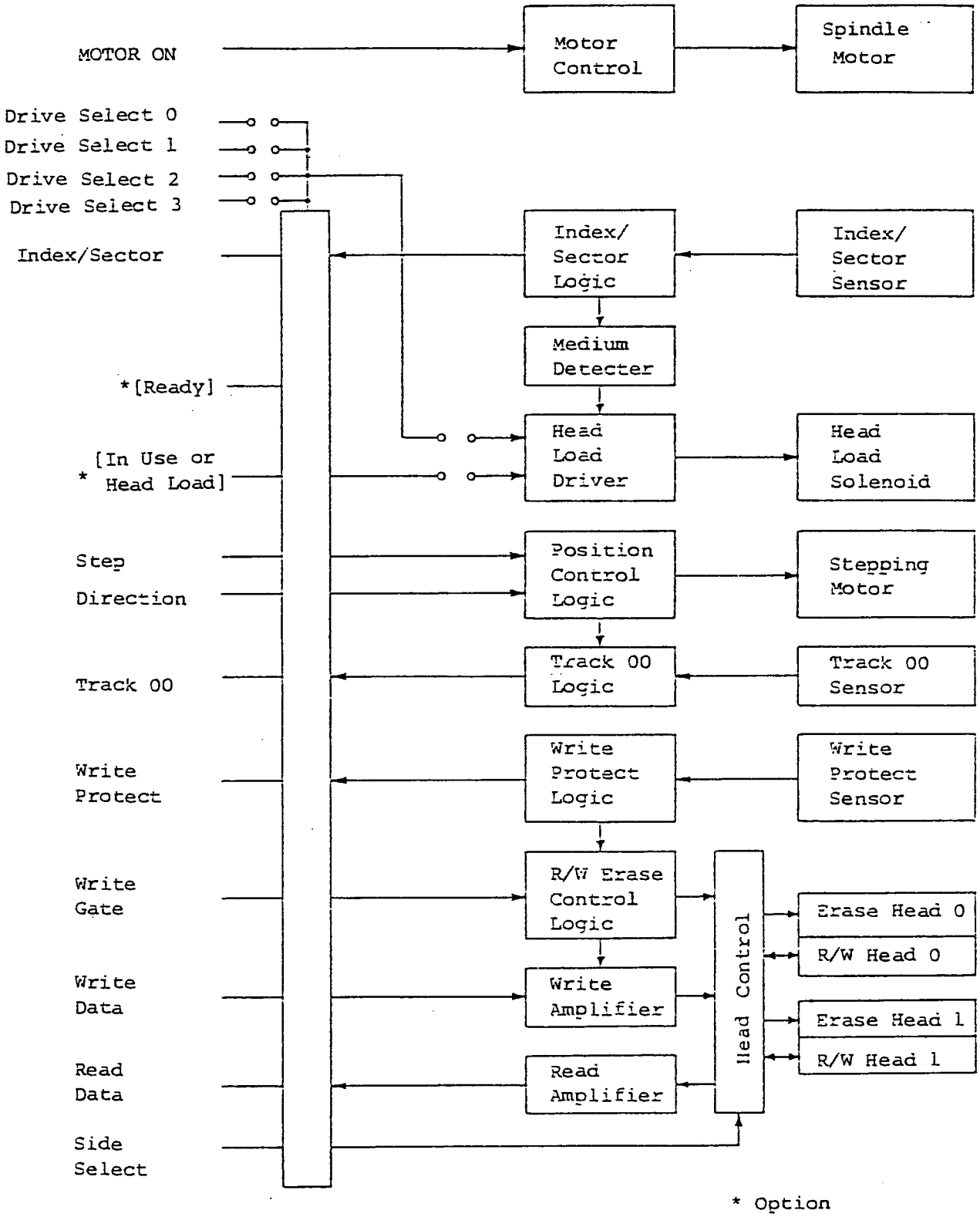


Fig.2-2 Electrical Block Diagram

CHAPTER 3 INTERFACE

The layout drawing of the interface is shown in Fig. 3-5. The interface is divided into a signal interface, power interface and frame ground.

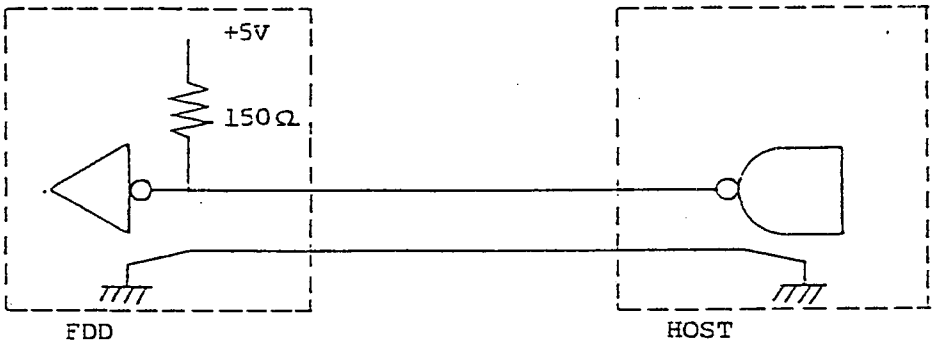
3-1 Signal Interface

The signal line is negative logic TTL compatible.

(1) Input circuit See Fig. 3-1

(2) Output circuit See Fig. 3-2

(1) Input

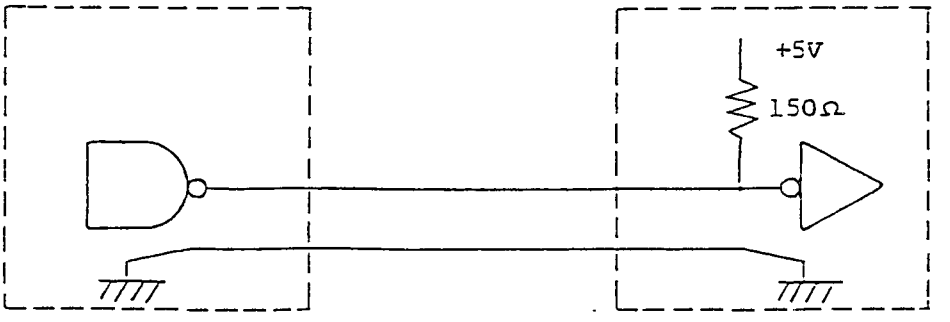


TI SN74LS14/7414 or equivalent

TI SN7438 or equivalent

Fig. 3-1 Input

(2) Output



TI SN7438 or equivalent

TI SN74LS14/ 7414 or equivalent

Fig. 3-2 Output

(3) Signal Level

(a) Input Signal Level

Low Level (True) : 0V~0.4V (Flow out current of less than 40mA)

Eigh Level (False) : 2.5V~5.25V

(b) Output Signal Level

Low Level (True) : 0V~0.4V (Sink current of less than 48mA)

Eigh Level (False) : 2.5V~5.25V

(4) I/O Signal and Pin Location

Pin No.		Signal Name	Signal Direction	
GND	Signal		FDD	HOST
1	2	NC		
3	4	*[IN USE OR HEAD LOAD]	←	
5	6	DRIVE SELECT 3	←	
7	8	INDEX/SECTOR	→	
9	10	DRIVE SELECT 0	←	
11	12	DRIVE SELECT 1	←	
13	14	DRIVE SELECT 2	←	
15	16	MOTOR ON	←	
17	18	DIRECTION	←	
19	20	STEP	←	
21	22	WRITE DATA	←	
23	24	WRITE GATE	←	
25	26	TRACK 00	→	
27	28	WRITE PROTECT	→	
29	30	READ DATA	→	
31	32	SIDE SELECT	←	
33	34	*[READY]	→	

Table 3-3 I/O Pin Location Table * Option

(5) Signal Connector

(a) Number of Pins 34

(b) Edge Card Connector on FDD

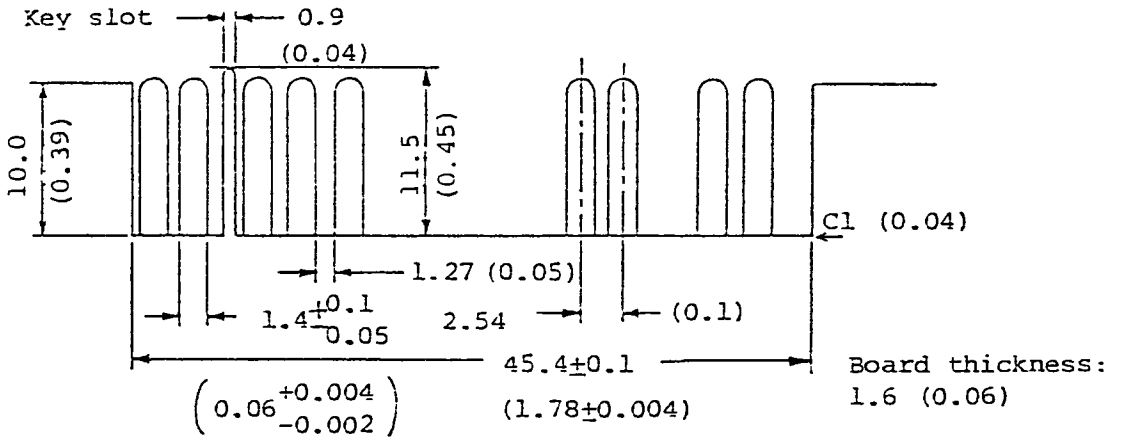
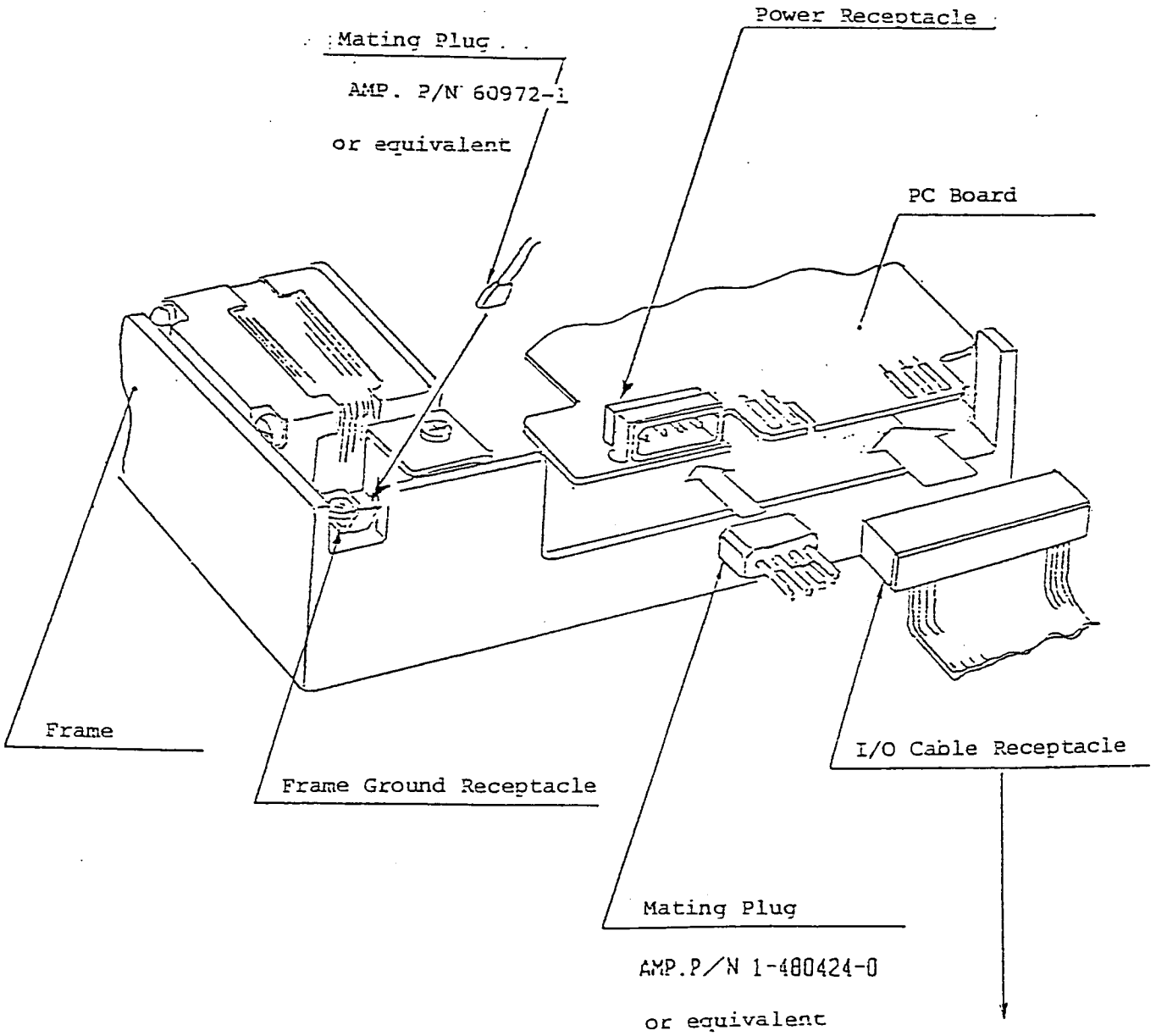


Fig. 3-4 Drawing of Edge Card Connector

NOTE: All dimensions are in mm. Dimensions in ( ) are in inches.

(c) Mating Connector : See Fig. 3-5.



Twisted Cable : AMP → P/N 583717-5 (Housing); P/N 1-583616-1 (Pin); P/N 583274-1 (Keying plug)

Flat Cable : 3M → P/N 3463-0001 (Connector); P/N 3439-0000 (Keying plug)

Fig. 3-5 Interface Layout

3-1-1 Input Signal Lines (FDD ← HOST)

(1) DRIVE SELECT 0 - 3

When one of four lines becomes LOW, only the drive with LOW signal will respond to the input lines, gate the output lines and turn the LED on.
Up to four drives can be controllable, and DRIVE SELECT (0～3) is pre-determined by shorting plug. (See Fig. 5 - 3).

(2) DIRECTION

This line is a control signal which defines direction of R/W head motion. If the input signal is LOW, the R/W head will move towards the center of the disk (STEP IN).
Conversely, if the input signal is HIGH, the R/W head will move away from the center of the disk (STEP OUT).
Any change in the DIRECTION must be made before receiving STEP pulse. (See Timing Chart)

(3) STEP

This signal is to move the R/W head by one track per one pulse. After receiving the final STEP pulse, the drive must wait at least Seek + Settling time to enable Read/Write securely.

(4) SIDE SELECT

This signal defines which side of a two-sided diskette to be written on or read from.
When this signal is LOW, side 1 head is selected, and when HIGH, side 0 head is selected. When switching from one side to the other, the waiting time is required before read/write operation starts.
At the write operation, this signal must remain the same until the tunnel erasure is completed. (See Timing Chart)

(5) WRITE GATE

LOW level enables write data to be written on the diskette. This signal becomes ineffective when WRITE PROTECT signal is LOW or the drive is not selected. HIGH level enables to read the data on the diskette.

(6) WRITE DATA

This line provides data to be written on the diskette. Each transition from HIGH to LOW of the FM/MFM signal will reverse the current through the R/W head, thereby writing a data bit. This line is enabled when WRITE GATE is LOW, WRITE PROTECT is HIGH and DRIVE SELECT is LOW.

(7) MOTOR ON

When this signal is LOW, the spindle motor rotates and when HIGH, the motor stops. The spindle motor reaches to the rated speed within 0.5 second. This line responds to the input signal regardless of the DRIVE SELECT signal.

(8) HEAD LOAD (Option for double-sided version only)

This signal line is used either HEAD LOAD or IN USE.
When this signal is low, R/W head loads against the diskette. The set-up time of the solenoid is required before using this signal.
This signal line responds to the input signal regardless of DRIVE SELECT line.

(9) IN USE (Option)

When DRIVE SELECT signal is low, LOW level of this line will turn the LED on and HIGH will turn the LED off.

3-1-2 Output Signal Lines (FDD → HOST)

(1) INDEX/SECTOR

The LOW signal is provided by the drive once each revolution of the diskette to indicate the beginning of the track.

(2) READ DATA

This line provides clock + data pulses which are converted from analog data detected by a R/W head.

(3) TRACK 00

The LOW state of this signal indicates that the R/W head is positioned at track 00.

(4) WRITE PROTECT

The LOW signal indicates that a write protected diskette is installed.
The drive will inhibit writing with a write protected diskette.

(5) READY (Option)

The LOW signal indicates that the diskette is rotating after properly inserted.

3.2 Power Interface

Power Connector

(a) Number of Pins : 4

(b) Power Connector Pins : See Fig. 3-6

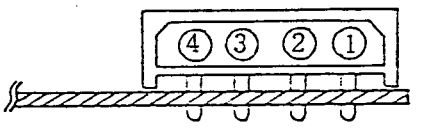
(c) Mating Plug (Host Side) : AMP P/N 1-480424-0

(d) Mating Pin (Host Side) : AMP P/N 170148-2 (AWG18 ~ 24)
AMP P/N 170121-4 (AWG14 ~ 20)

3.3 Frame Ground

Mating Terminal (Host Side) : AMP P/N 60972-1

NOTE: Use AWG24 or thicker cable for the power cable and ground cable.



PC board

1 PIN ------ DC +12V
2 PIN ------ OV RETURN (GROUND)
3 PIN ------ OV RETURN (GROUND)
4 PIN ------ DC +5V

Fig. 3-6 Power Connector Pins

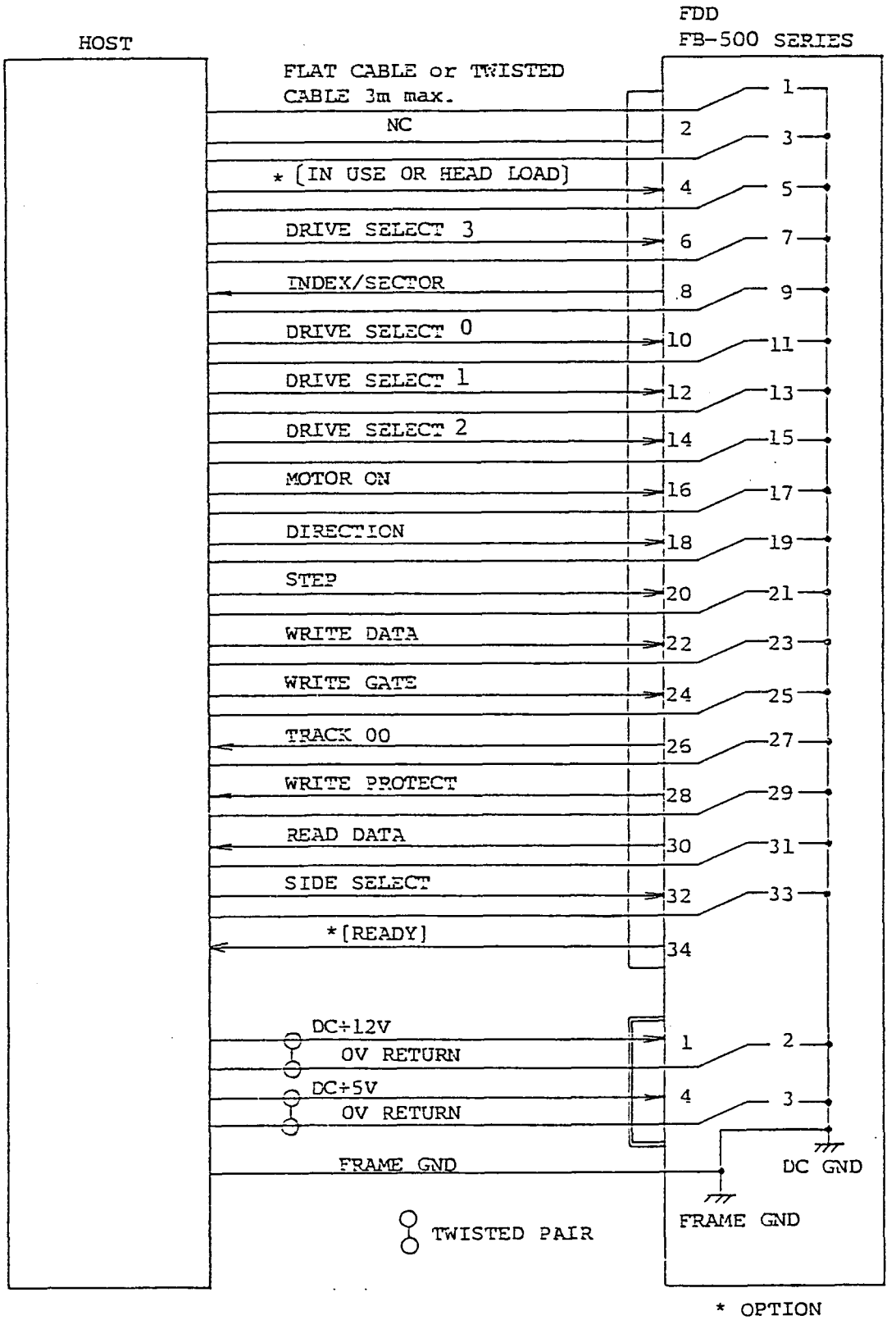
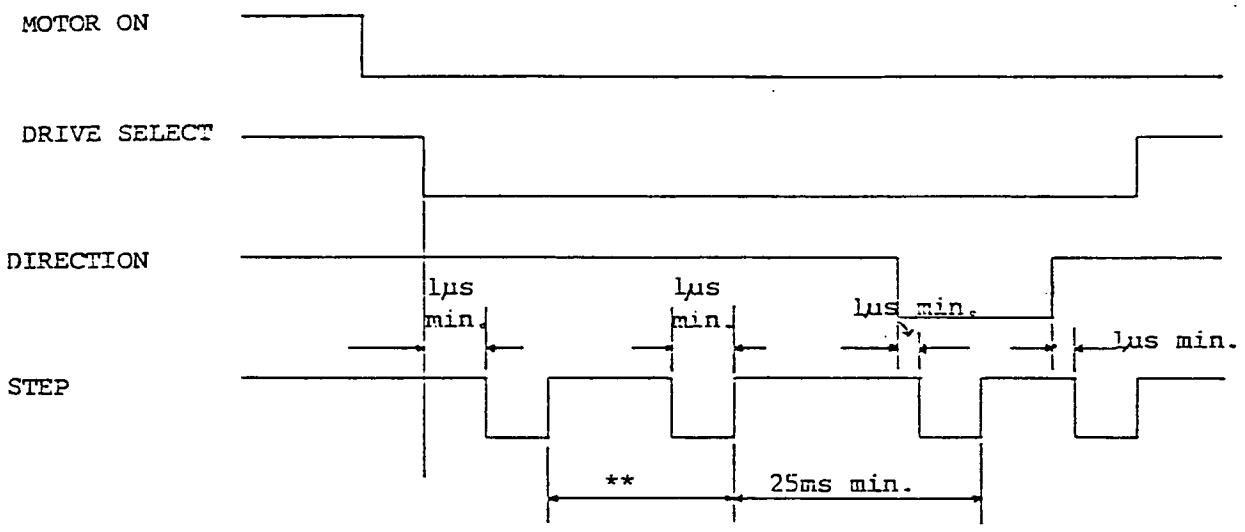


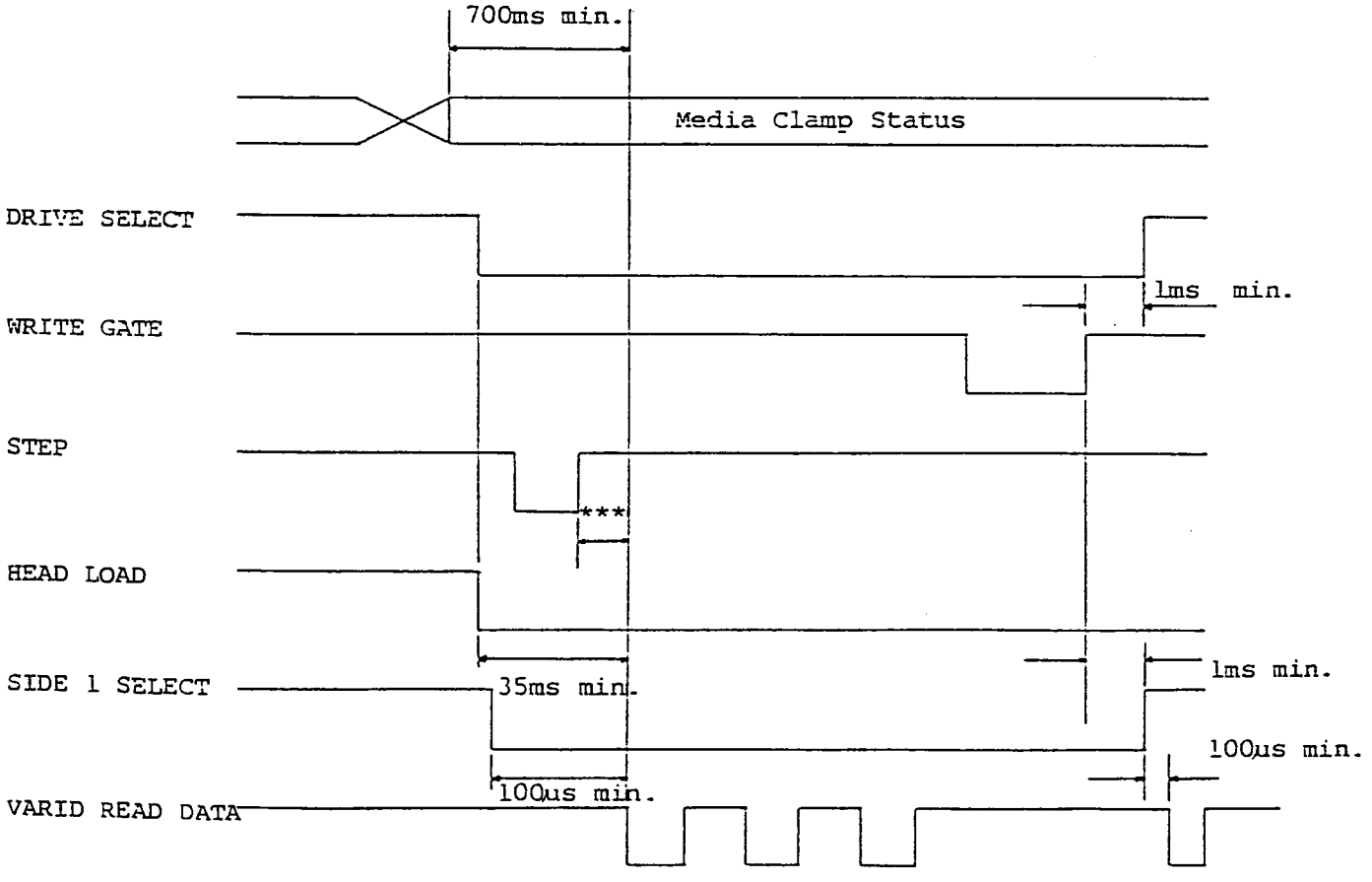
Fig. 3-7 Interface Connections

Chapter 4 Timing Chart



** = Seek Time
FB-501,503 6(ms) min.
502,504 3(ms) min.

Fig. 4-1 Track Access Timing



*** = Seek Settling Time
FB-501,503 21(ms) min.
502,504 18(ms) min.

Fig. 4-2 Read Data Timing

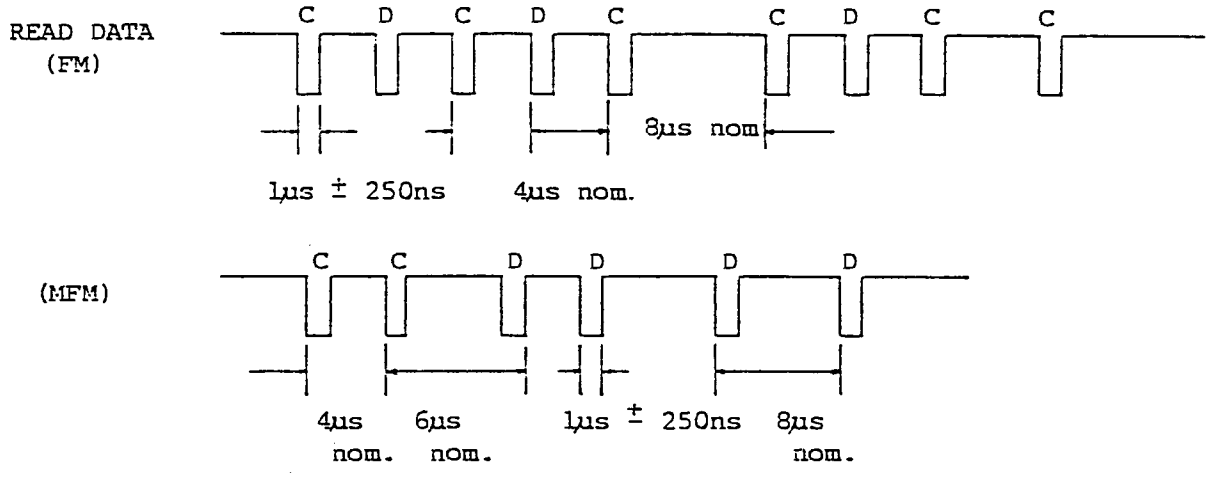
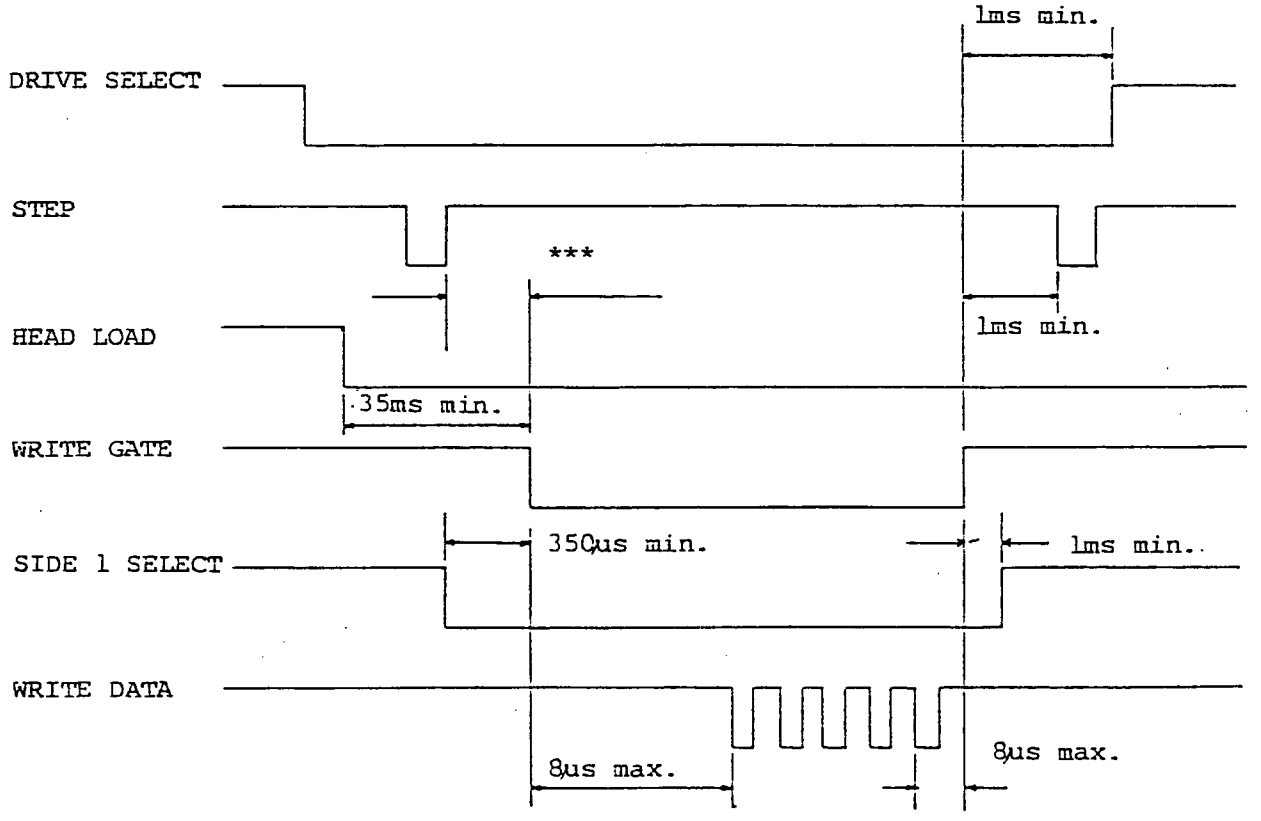


Fig. 4-3 READ DATA



*** = Seek Settling Time
FB-501,503 21(ms) min.
502,504 18(ms) min.

Fig. 4-4 Write Data Timing

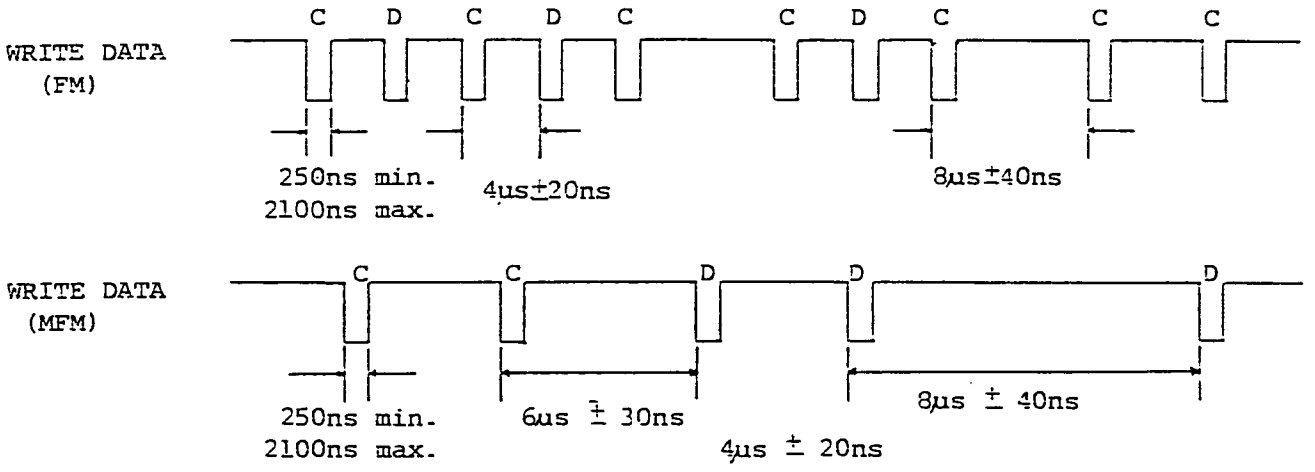


Fig. 4-5 WRITE DATA TIMING

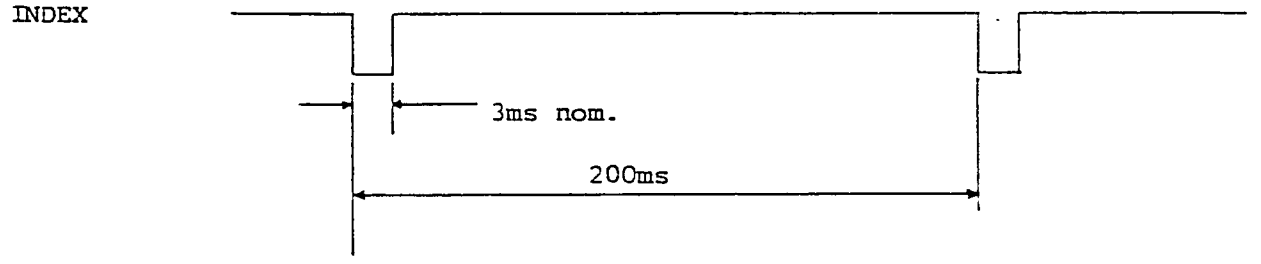


Fig. 4-6 INDEX TIMING

CHAPTER 5 SELECT PIN SETTING

5-1 Input Signal Termination

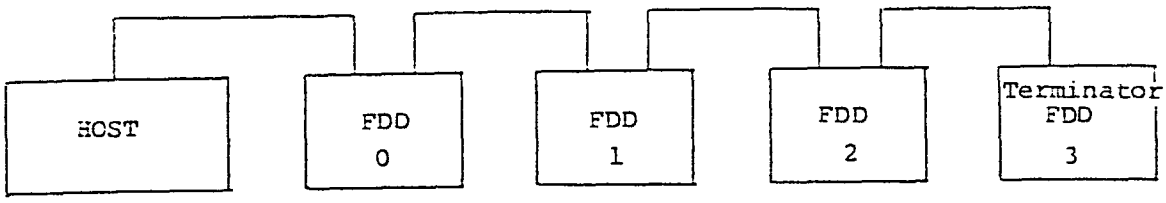
FB-500 can be connected either daisy chain or radial chain. Each drive has the line termination network (terminator). As shipped from the factory, the terminator is installed on each drive. Remove this network when not necessary. Daisy chain and radial chain are shown in Fig. 5-1 and 5-2 while the location of terminator is shown in Fig. 5-3.

5-2 FDD Number Shorting plug

The address of each drive is determined by the location of shorting plug. As shipped from the factory, a shorting plug is installed on the DRIVE SELECT 0. (See Fig. 5-3)

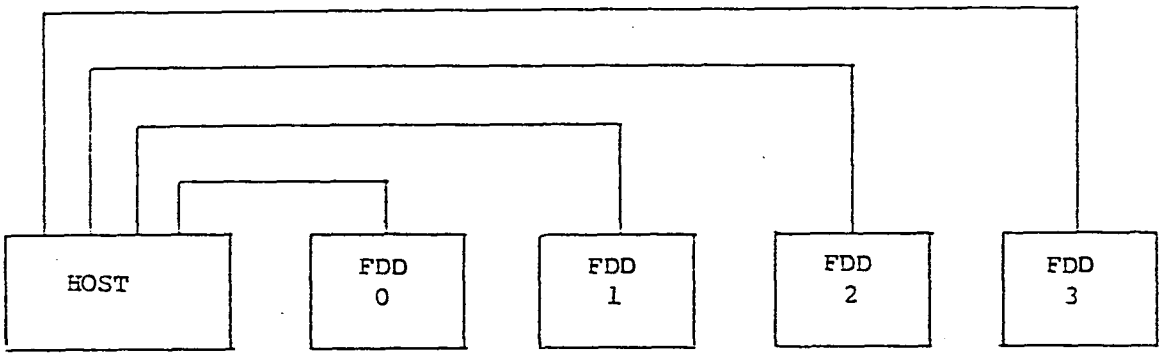
5-3 Shorting Plug for Testing (MX)

The output signal is always effective regardless of the DRIVE SELECT 0 ~ 3 signals. (See Fig. 5-3)



Only the FDD 3 must have the line terminator.

Fig. 5-1 Daisy Chain



Each FDD must have the line terminator.

Fig. 5-2 Radial Chain Method

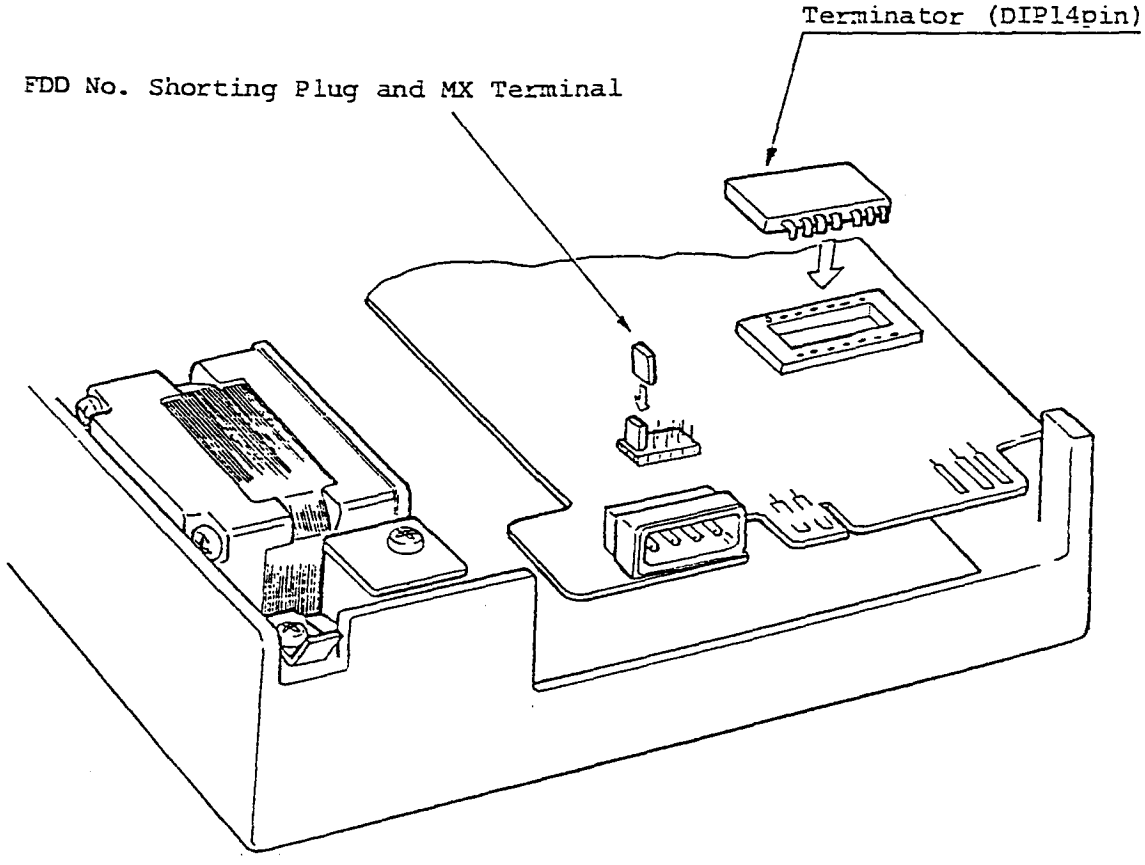


Fig. 5-3 FDD No. Setting and Terminator

Chpater 2 Mechanical Section

(FB-500 Series)

CONTENTS

1. DISK PROTECTION MECHANISM AND CLAMP MECHNISM

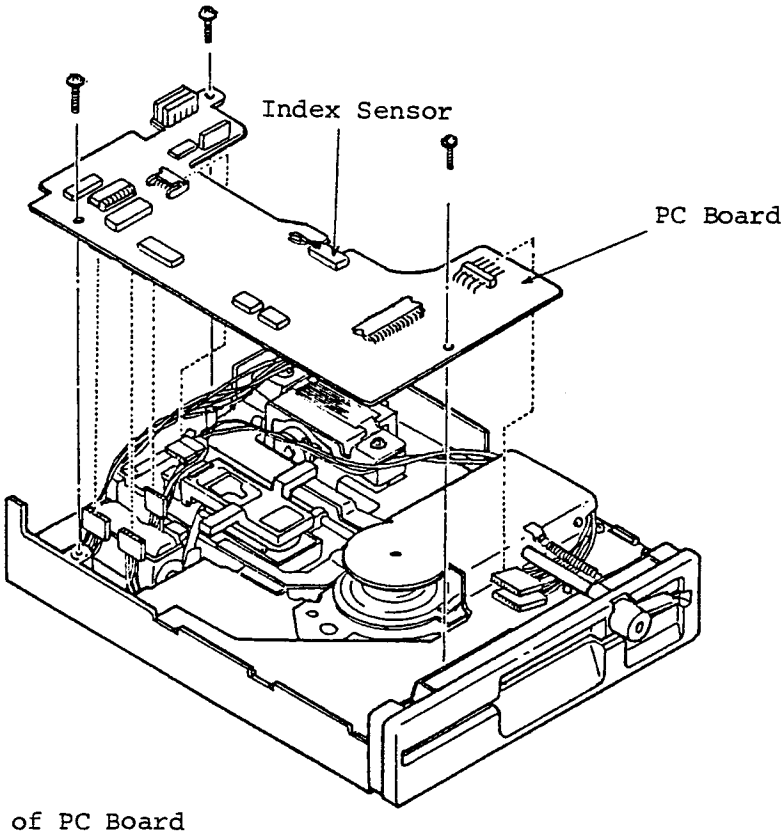
(1) The FB-503 and FB-504 are so designed that the door cannot be locked until the disk is completed inserted in the unit. In the FB-501 and FB-502, the head cannot touch and damage the disk because it is a single-side head.

(2) The clamp mechanism of the FB-500 Series accurately centers the disk to protect the center hole of the disk, thus lengthening the life of the disk.

(3) The shape of the front panel allows the disk to be inserted or removed easily.

2. INSTALLATION AND REMOVAL OF COMPONENTS

2.1 PC Board



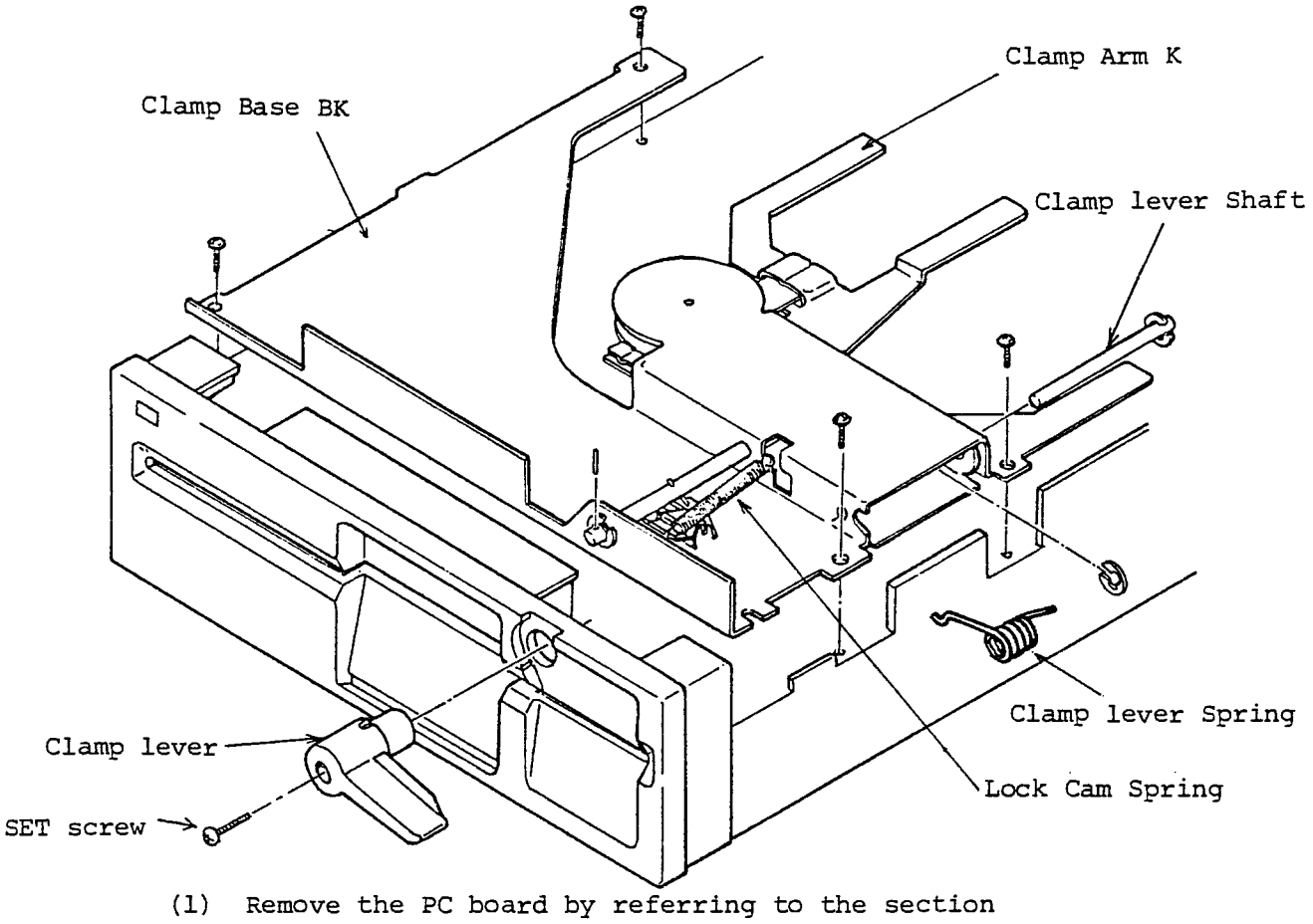
(1) Removal of PC Board

- o Remove the three set screws retaining the PC board to the base.
- o Detach all the connector cables.

(2) Installation of the PC board

- o Attach the connector cables to the PC board.
  Make sure that the connector cables are properly routed.
  In the case of the double-side head, be extremely careful to distinguish the upper from lower head cables.
  The cables of the upper head should be white-marked.
- o Tighten the three set screws of the PC board.
- o The write protector and index sensor are directly mounted on the PC board. The write protector requires almost no adjustment while it is necessary to adjust the index sensor whenever it is mounted on the PC board.
  The index sensor should be adjusted by referring to page 2-8.

2.2 Clamp Base BK and Clamp Arm K



(1) Remove the PC board by referring to the section 2.1(page 2-2).

(2) Remove the set screw retaining the clamp lever, and pull out the clamp lever from the shaft.
Pull out the pin inserted in the shaft.

(3) Remove the four set screws retaining the clamp base BK.

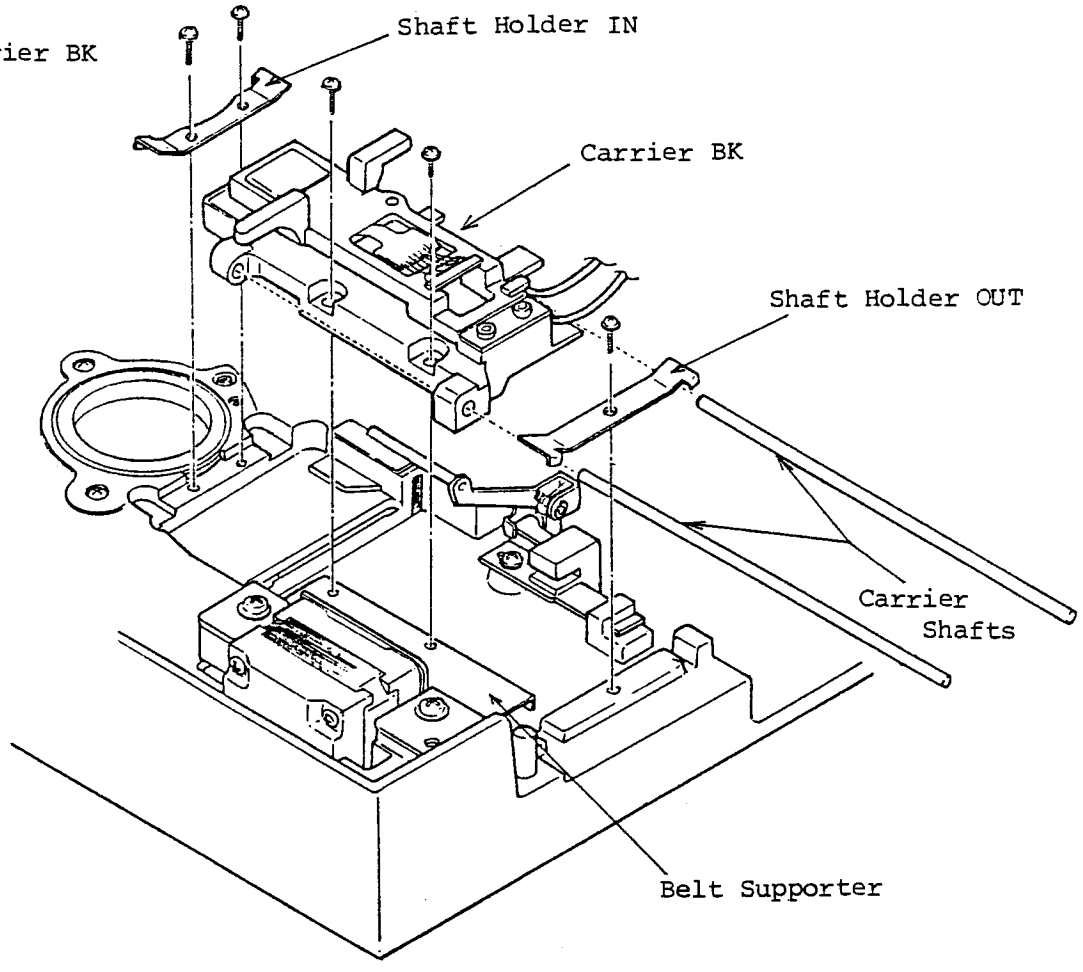
(4) Pull out the clamp lever shaft by removing the E-ring and clamp lever spring.

(5) In the above procedure, the clamp arm K parts from the clamp base BK.

(6) The clamp BK can be removed by separating the clamp base BK from the base and pushing down the clamp arm.

(7) Follow the above procedure in reverse for re-assembly.

2.3 Carrier BK



(1) Remove the PC board by referring to the section 2.1(page 2-2).

(2) Remove the clamp base BK by referring to the section 2.2 (page 2-3).

(3) Remove the two screws connecting the belt supporter to the carrier BK.

(4) Remove the head cable.

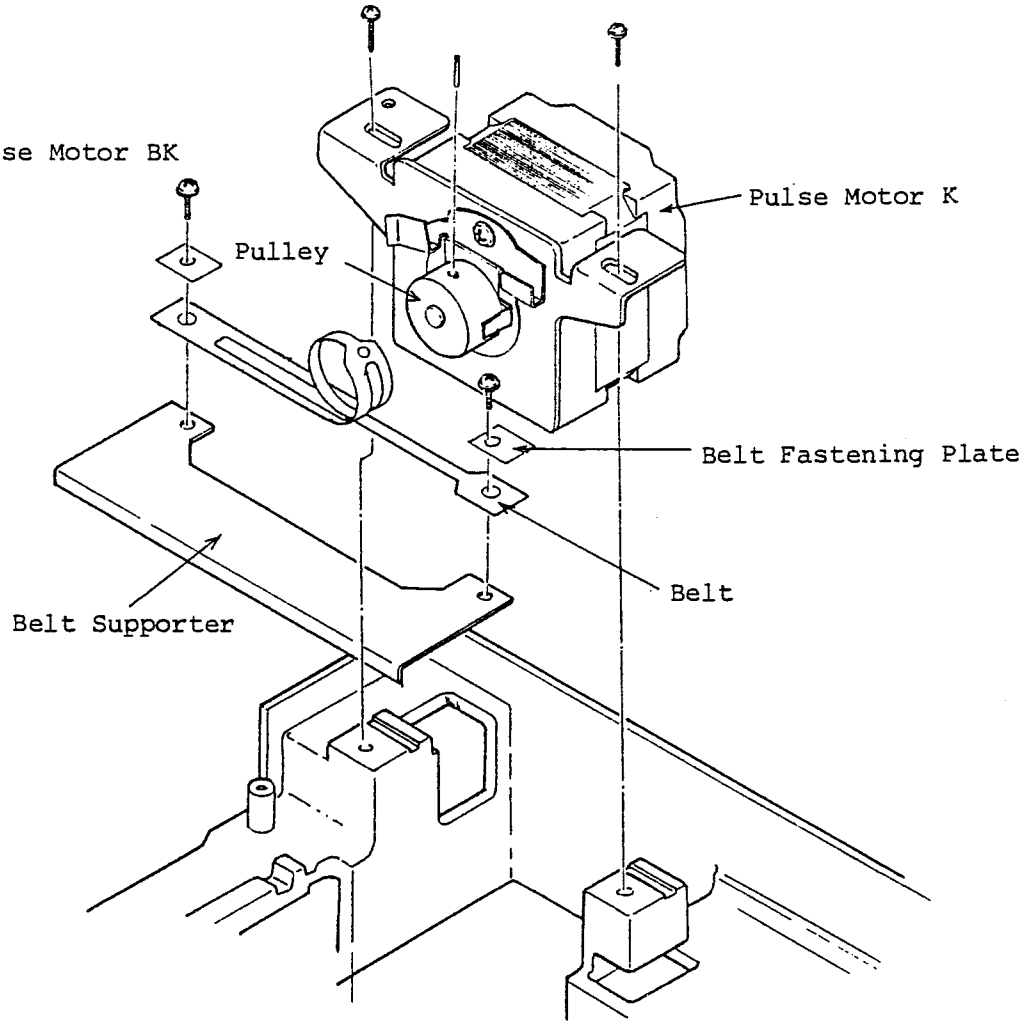
(5) Remove the set screws of the shaft holders OUT and IN, and remove the shaft holders OUT and IN.

(6) Remove both carrier shafts.

(7) When re-mounting the carrier, the adjustment requirements must be performed.

(8) Follow the above procedure in reverse for re-assembly.

2.4 Pulse Motor BK



(1) Remove the carrier BK from the base by referring to section 2.3 (page 2-4).

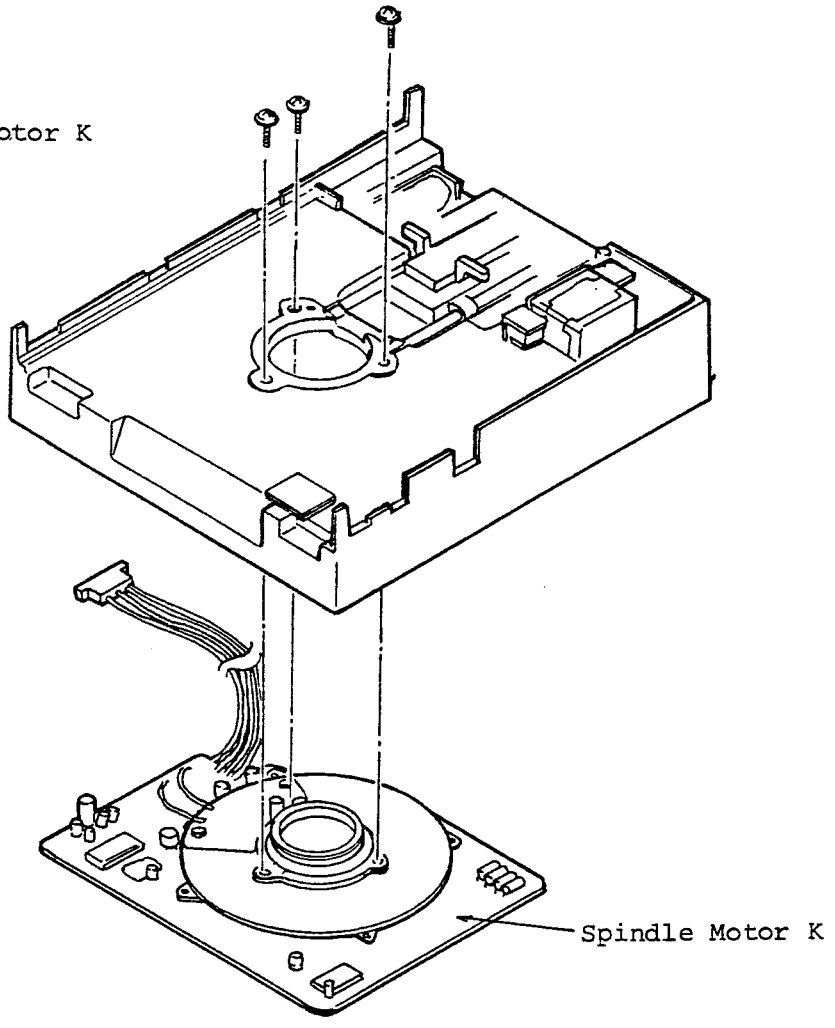
(2) Remove the screws positioning and retaining the pulse motor K.

(3) Remove the set screws of the belt supporter.

(4) Remove the pulley set screw of the pulley, which is retaining the belt.

(5) Follow the above procedure in reverse for re-assembly, after adjusting the steel belt tension.

2.5 Spindle Motor K



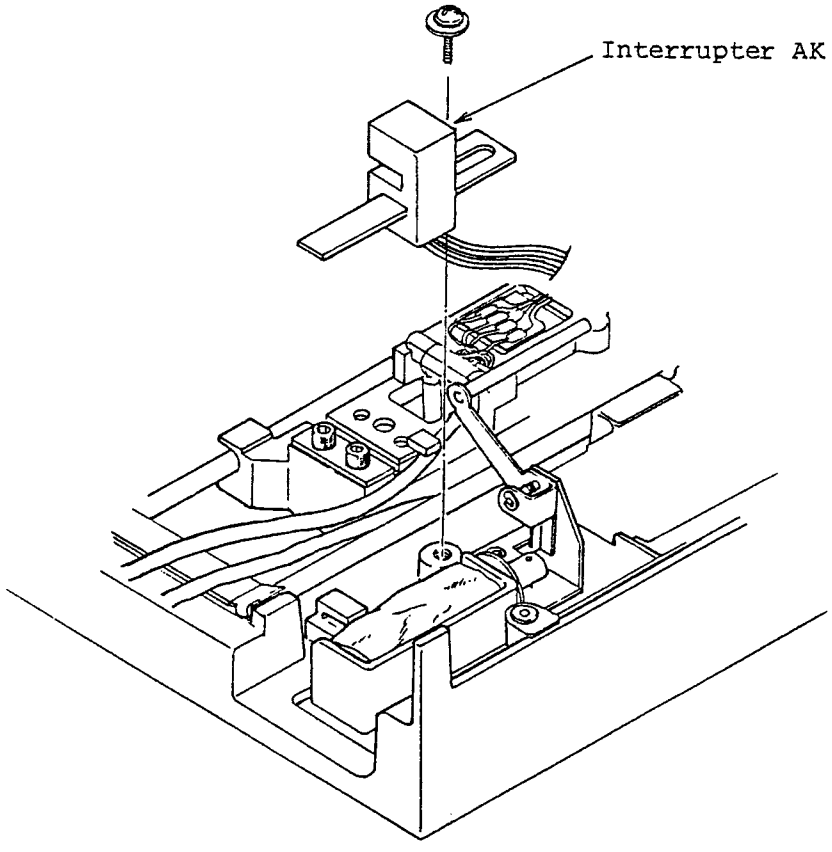
(1) Remove the PC board by referring to the section 2.1(page 2.2)

(2) Remove the clamp base K and clamp arm K by referring to section 2.2(page 2.3).

(3) Remove the three set screws holding the spindle.

(4) Follow the above procedure in reverse for re-assembly.

2.6 Interrupter and Adjustment of Track00



(1) Remove the PC board by referring to the section on 2.1(page 2.2)

(2) Remove the positioning set screw of the interrupter AK.

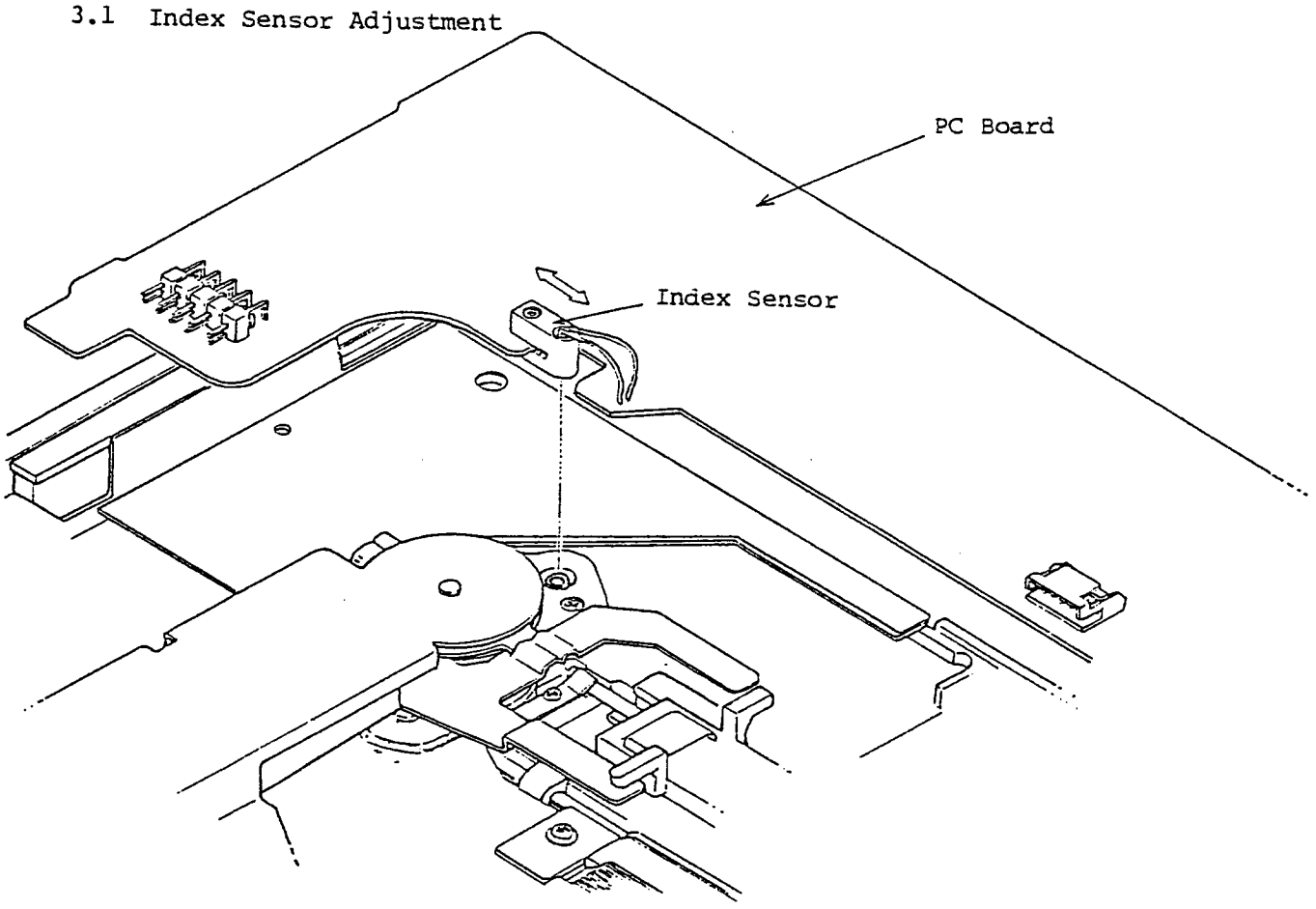
(3) Remove the interrupter.

(4) Temporarily tighten the positioning set screw when mounting the interrupter.

(5) Perform the TR00 adjustment in section 3.

3. ADJUSTMENT

3.1 Index Sensor Adjustment



(1) The index sensor optically detects the index hole in the disk.

(2) The index sensor should be adjusted in the following manner.

a. The LED of the index sensor is built in the DD motor K thus it cannot be adjusted in position.

b. The photo transistor is adjusted by loosening the socket screw.

c. Use a commercially available alignment diskette. The alignment diskette usually stores the index burst signal at two points, the outer track and inner track.

d. Connect the CH1 probe of the ocslloscope to pin 2 of TP-1, adn the CH2 probe to pin 3 ro 4 of TP-2. Connect the GND to pin 4 of TP1 or pin 2 of TP-2. (CH level: 40mV/div.d.c., time base: 50μs/div.)

e. The index burst signal appears as follows:

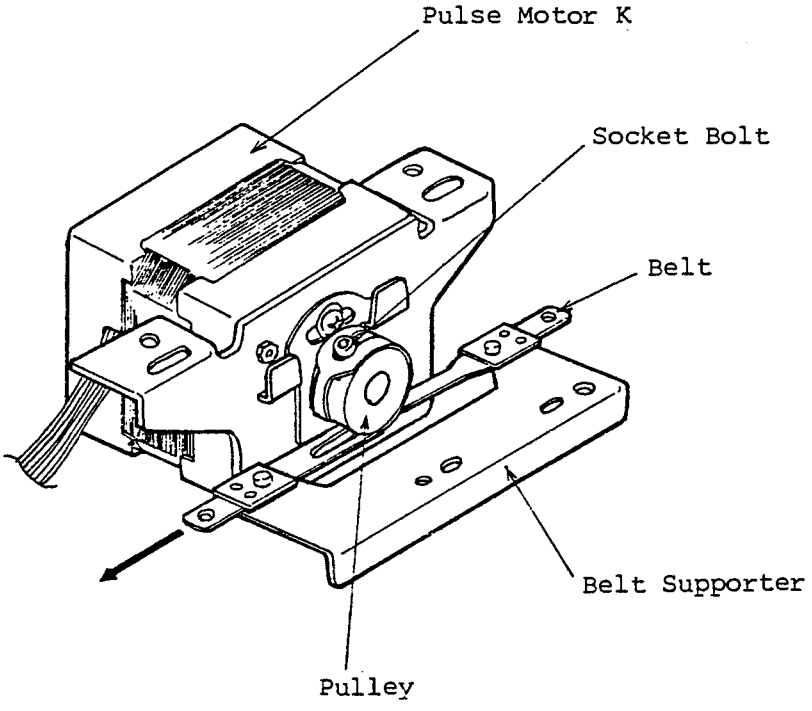
Outer Track: Within $200\mu s \pm 100\mu s$

Inner Track: Within above $\pm 50\mu s$

f. Move and adjust the transistor in position to meet the above values.

o For a double-side machine, make adjsutments until both sides meet the above values.

3.2 Tensioning and Adjustment of Steel Belt



(1) Remove the pulse motor BK by referring to the section 2.4 (page 2.5).

(2) Loosen the socket bolt for positioning the pulse motor and pulley, and pull out the pulley from the shaft of the pulse motor.

(3) Use the independent tool to tension and adjust the steel belt.

(4) Set the pulley on the jig, wind the belt round the pulley, and temporarily fix the pulley and belt with the set screw.

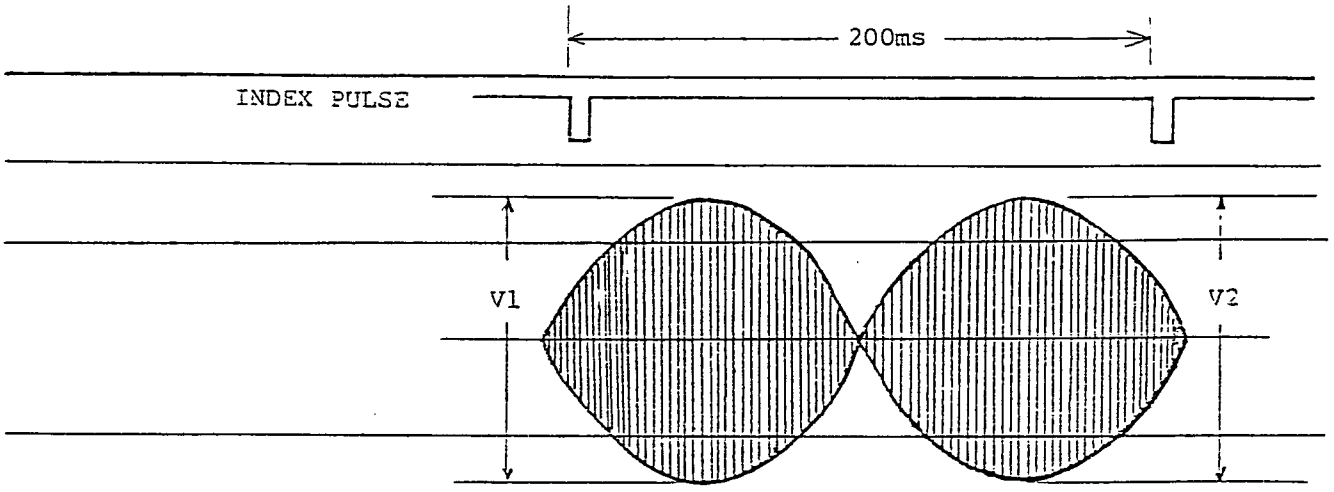
(5) Set the belt as shown in the figure, temporarily fix the right end belt holding screw. Pull the left end of the belt by a force of 1.2Kg with the tension gage, and then fasten the belt.

(6) When following step(5), be sure that the belt is wound in parallel with the pulley.

(7) Finally tighten the screw temporarily retaining the pulley and belt.

(8) Termporarily tighten the pulley and belt to the shaft of the pulse motor to provide excitation later.

3.3 Head/Radial Adjustment (CE Adjustment)



(1) Measure and adjust the reproduced signal waveform of track 16 (double track 32 for) of a commercially available alignment disk.

o At this time, observe the waveform by moving the carrier from outer side and inner side.

(2) Obtain the waveform shown in the figure above

(3) Externally trigger the fall of the index singal of pin 2 of TP-1. The waveform should be stationary.

(4) Connect CH1 to pin 2 of TP-2, and CH2 to pin 4 of TP-2, and GND to pin 4 of TP-1 or pin 2 of TP-2.
(CH level: 50mV/div. d.c., time base: 20mS/div.)

(5) A temperature and humidity correction table is provided for the alignment disk in each maker.
Adjust the measured value according to the table.

Measurement Reference

$100\% \geq (V1/V2 \text{ or } V2/V1) \times 100\% = 85\%$

Adjust to obtain the result of either of the above expressions.

Adjustment Points

For side 0 (lower head), make adjustments by moving the pulse to the right or left. For double sides, adjust the lower head first, then adjust side 1 (upper head) after switching the head. For the upper head, make adjustments by loosening the socket screws on the carrier and by moving the head to the right or left.

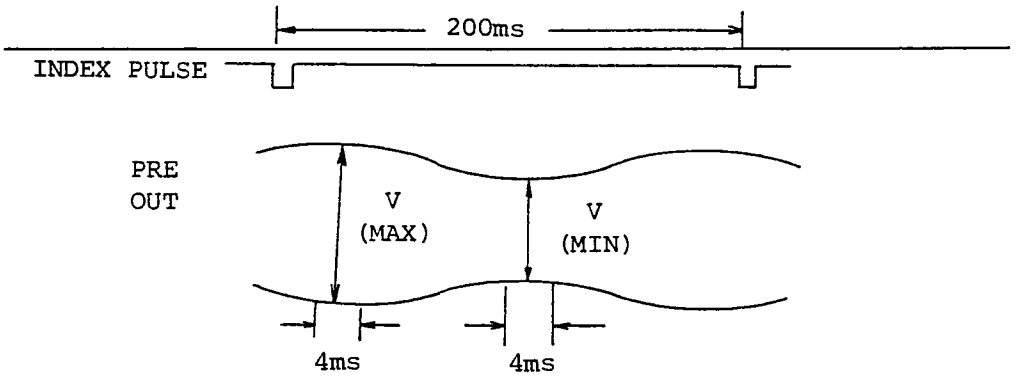
3.4 Head Output Adjustment

Follow the procedure below to adjust the head output.

(1) Use a disk which is normal and clean enough to detect any fault in the head.

(2) Start the motor.

(3) Write 2F signals on track 00 and track 39/79, and then reproduce them. Read the reproduced signal waveforms with the synchroscope.



(4) Obtain the waveform shown in the figure above.
Use a synchroscope with two channels and an external trigger function.

(5) Connect the external trigger to pin 2 of TP-2 (5V/div., d.c.), and synchronize on the fall of the signal.
Connect other channels 1 and 2 to pin 3 of TP-2 and pin 4 of TP-2 ground each probe.
Set to ADD mode, set either pin 3 or 4 of TP-2 to INVERT, and set the time base at 20ms/div.
Measure the average value of an area of at least 4 melliseconds as shown in the figure above.

(6) The adjustment criteria is for more than 900mV (single track) or 600mV (doule track) amplitude with the 2F signal on track 39/79. Adjust by loosening the set screw of the pulse motor and changing the posisiton of the pulse motor.

(7) Modulation : M

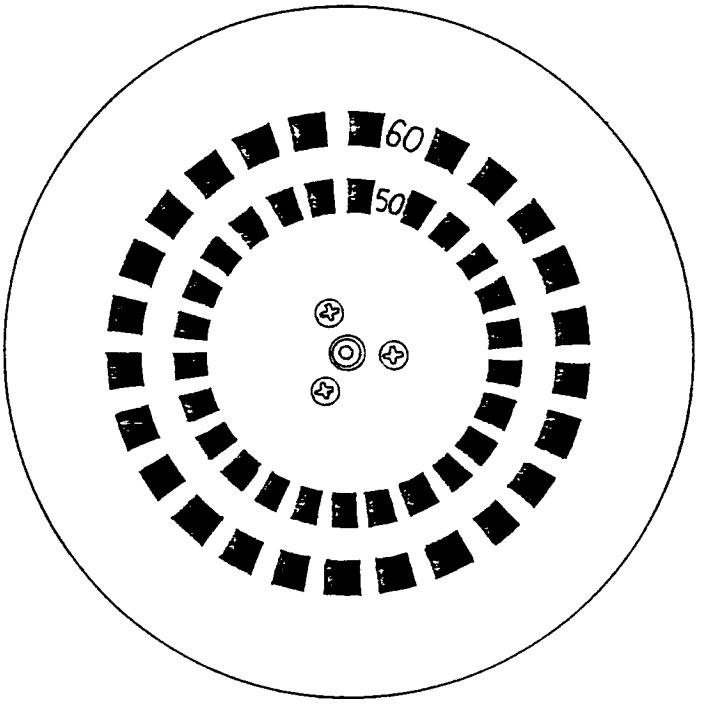
$$M \leqq 10\%$$

$$M = \left(\frac{Vmax. - Vmin.}{Vmax. + Vmin.} \right) \times 100\%$$

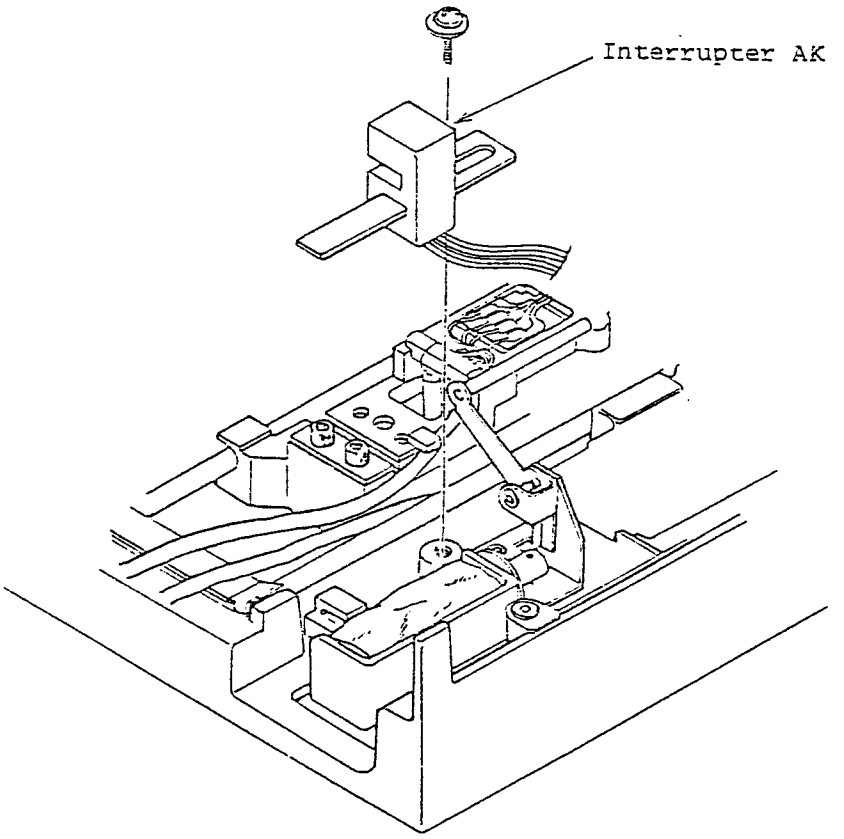
3.5 Motor Speed Adjustment

(1) Insert the media after the motor ON signal is inputted.

(2) Adjust VR1 on the DD motor control PC board so that the balck stripe of the stroboscope of the DD motor looks stationary under a 50Hz- or 60Hz-fluorescent lamp.
The DD motor used is shown below.



3.6 Track 00 Adjustment



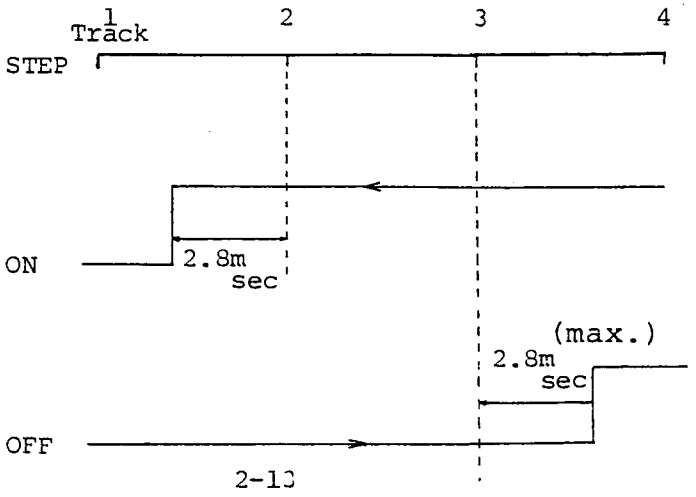
* Adjustment of Track 00

- o Make this adjustment after the CE is adjusted.
- o Points to Which Probes Are Connected

  Connect CH-2 to pin 3 of TP-1, and CH-1 to pin 5 of TP-1. Pin 4 of TP-1 is connected to GND. The rise of the STEP signal emitted from pin 3 of TP-1 is synchronized.

- o Adjustment Points

  Set the carrier so that it will run between Track 4 and Track 1. Make adjustments by moving the interrupter until the following timing is obtained.



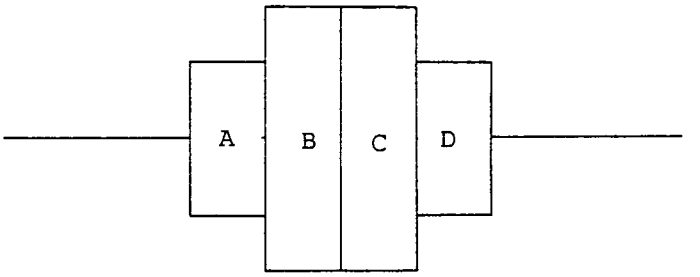
3.7 Adjustment of Head Azimuth

1. This adjustment is possible only for side 1 (upper head).

2. Points to Which Probes Are Connected

   Connect the probe of CH-1 to pin 2 (INDEX) of TP-1 for synchronization. Connect the probe of CH-2 to pin 3 or pin 4 of TP-2.

3. Move the carrier to track 34 (68 in the case of double track) on the alignment disk, and make adjustments so that the following waveform will be obtained.



$C/B \geqq 73.5\%$

$B \geqq C$

$A \leqq B$ and $D \leqq C$

$B/C \geqq 73.5\%$

$B \leqq C$

$A \leqq B$ and $D \leqq C$

More than 73.5% will be accepted.

- Since the index burst, azimuth, and CE for side 1 must be adjusted by moving the head, move the head to a position where these three conditions are met.

4. SPECIAL MAINTENANCE TOOLS

The following special tools are used for maintenance.

	Tool Name	
a.	Osilloscope	30MHz
b.	Simulator	(Example: BRIKON)
c.	DC supply	+12V, +5V
d.	Alignment Diskette	

5. MAINTENANCE

5.1 PROCEDURE FOR CLEANING THE READ/WRITE HEAD

In the FB-501, 502, 503 and 504, only the floppy disk head cannot be replaced. because it is completely bonded to the carrier. The head should be cleaned only when accumulated oxide compounds ($r\text{-}Fe_2O_2$) are noticeable. Note that any other cleaning method than the one described below may cause scratches on the head.

1. Slightly damp a cotton swab with isopropyl alchohol.
2. Part the load arm from the head without touching the load button.
3. Softly wipe the head with the dampened part of the cotton swab.
4. After the alchohol has fully evaporated, softly polish the head with a clean cotton swab.
5. Place the load arm on the head. At this time, extream caution should be exercised to avoid shocks to the head.

5.2 Caution on Handling Disks

- Avoid directly touching the mylar.
- Avoid storing disks in locations with high temperature or high humidity.
- A disk should be taken out from or inserted into the drive while the power is on (while the DD motor is operating).
- Acways ensure that the disk is inserted properly.

CHAPTER 3 CIRCUIT EXPLANATION

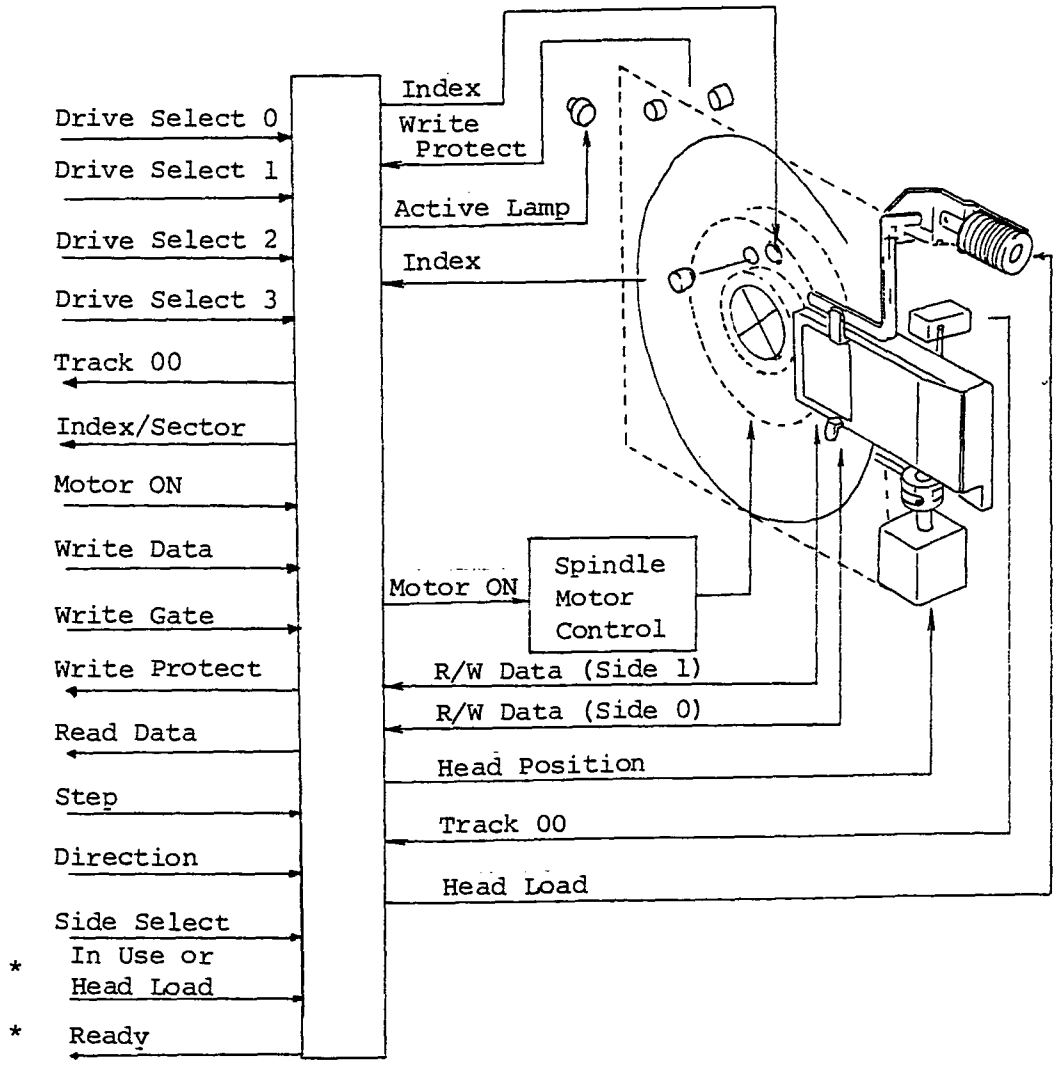
(FB-500 SERIES)

CONTENTS

1. GENERAL DESCRIPTION

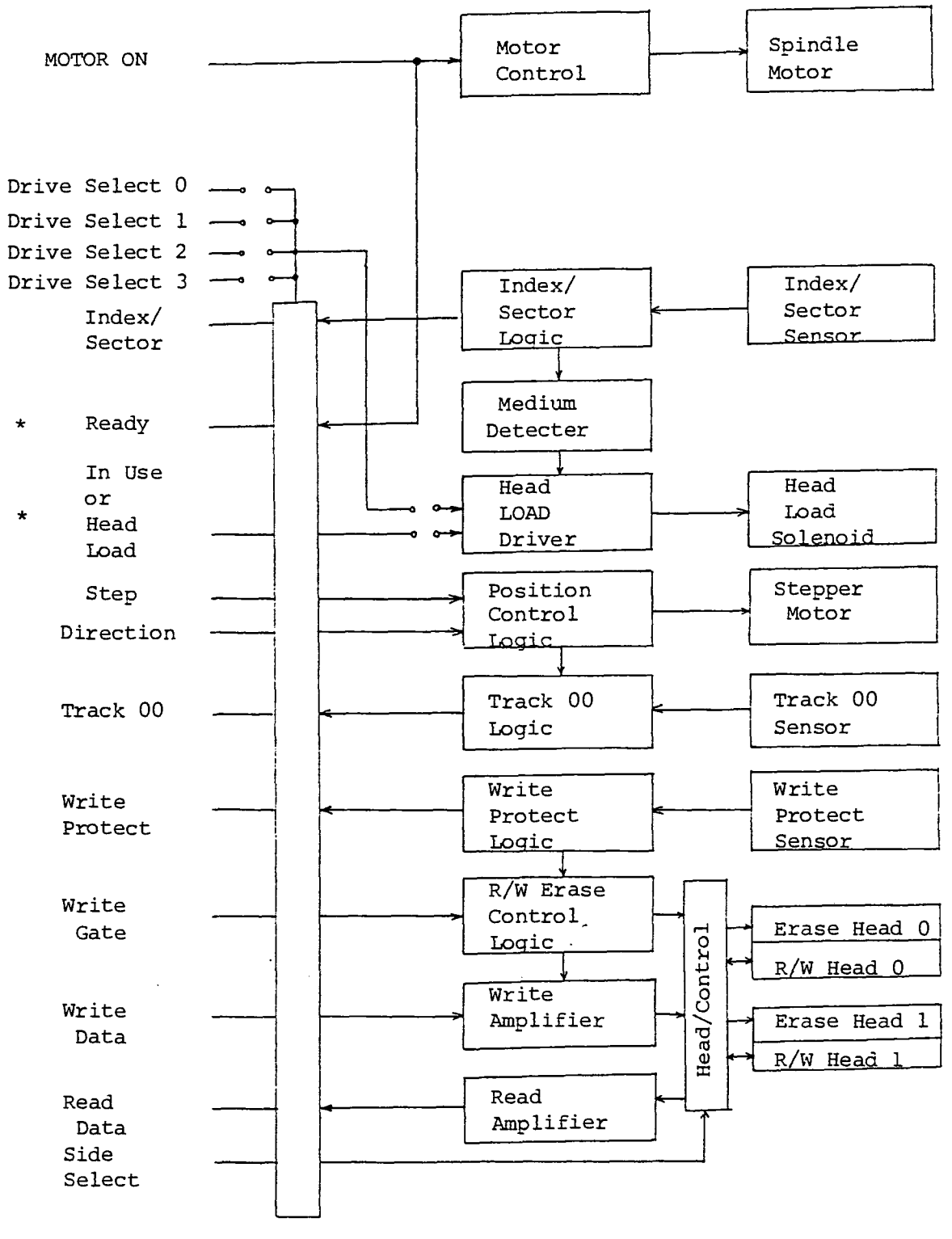
This circuit uses two independent LSIs: the LSI that controls the signals from the pulse motor, DD motor, and the sensors and the LSI for the read circuit, thus realizing an increase in packaging density, compaction of the unit, power-saving and improvement of the reliability.

2. BLOCK DIAGRAM



* Option

3. ELECTRICAL DIAGRAM



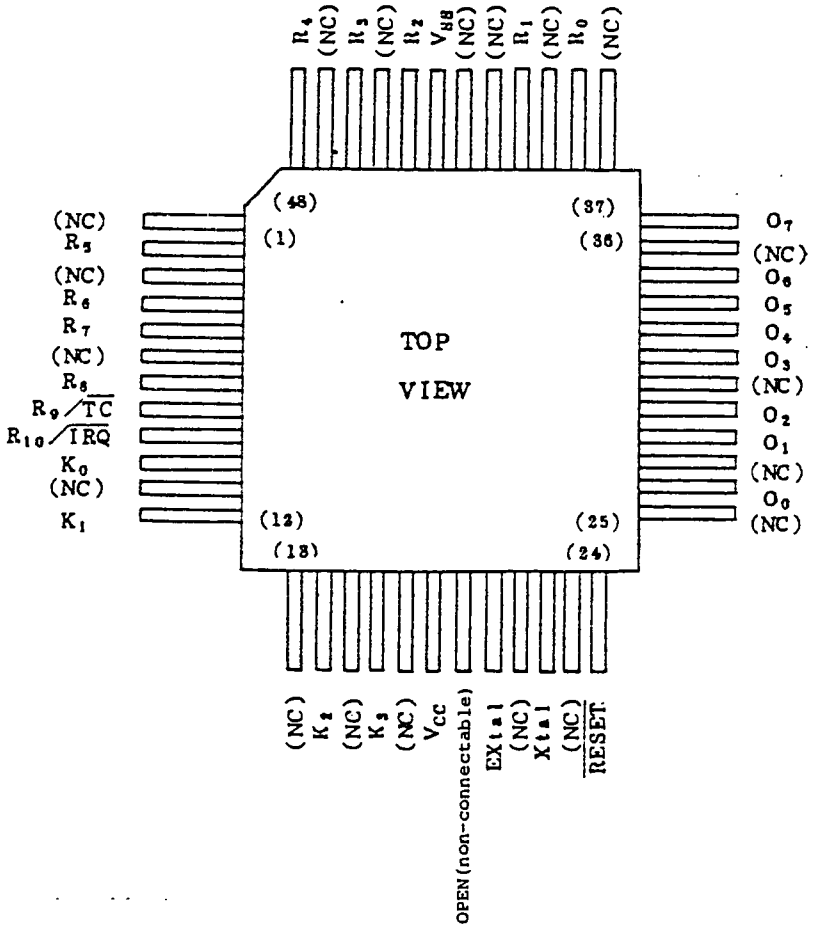
* Option

4. INDEPENDENT LSI CONFIGURATION AND PIN NAMES

4.1 Control LSI

Provided with the same functions as a one-chip CPU, this independent LSI is designed considering the hard timing required by the flexible disk drive (hereinafter referred to as "FDD").
The package is made compact and operated from a single +5V supply.
All the pins are TTL-compatible.
This LSI mainly controls the logic system.

Pin Configuration



Pin Names

Pin Number	Symbol	Function
2	R5	———
4	R6	———
5	R7	External Motor Rotation Signal
7	R8	———
8	R9	Write Gate Signal
9	R10	Write Gate Edge
10	K0	Write Protect Signal
12	K1	Drive Select Signal
14	K2	Direction Signal
16	K3	Side One Select Signal
26	O0	Pulse Motor Phase A
28	O1	Pulse Motor Phase B
29	O2	Pulse Motor Phase C
31	O3	Pulse Motor Phase D
32	O4	Track 00 External Output Signal
33	O5	Ready Signal
34	O6	Erase Gate Signal
36	O7	Write Gate Signal Start and End Judgement Signal
38	R0	For Pulse Motor Voltage Switching
40	R1	Track 00 Position
44	R2	Index Pulse
46	R3	Step Pulse
48	R4	———

4.2 Read LSI Configuration and Pin Names

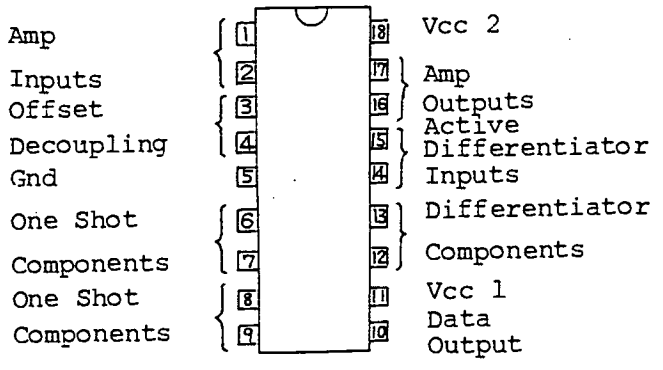
This LSI is a monolithic read amplifier that outputs signals recorded on the floppy disk in the form of digital signals. The LSI amplifies signals from the magnetic head and passes them through the filter. Then, it passes them through the differentiator, zero volt comparator and waveform shaper to obtain pulse outputs.

Features

Floppy Disk read processing is performed by one IC.

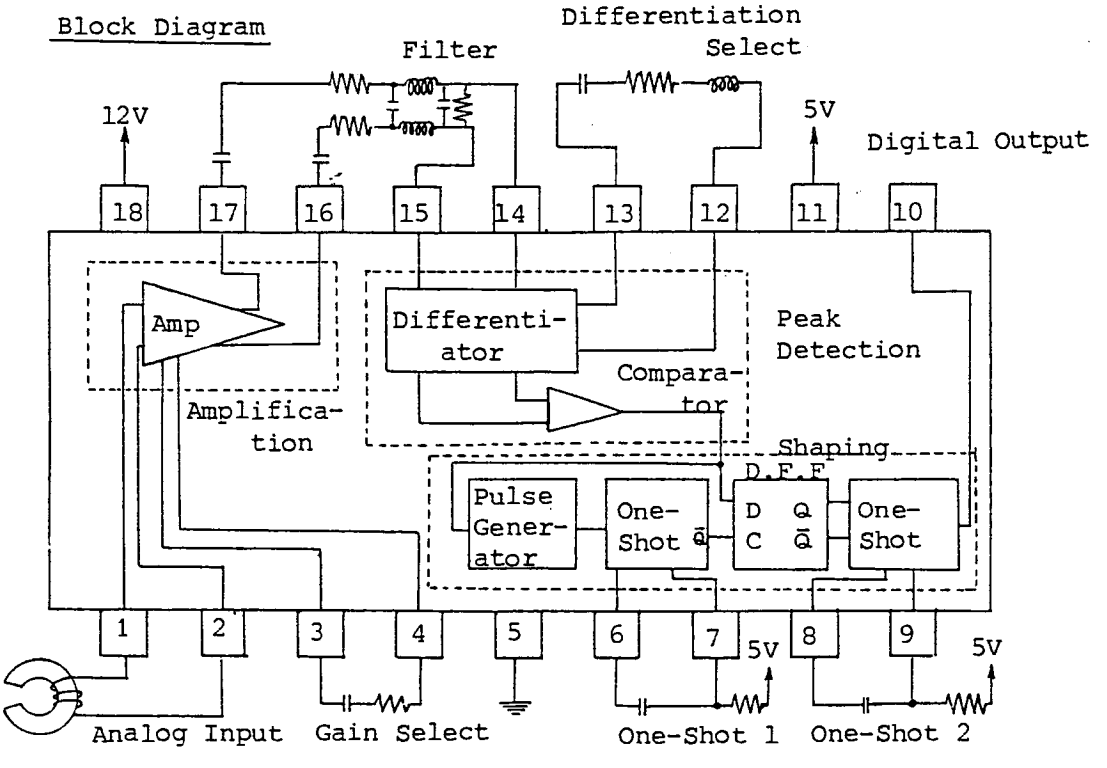
The outputs can be directly connected a TTL device.

Pin Configuration



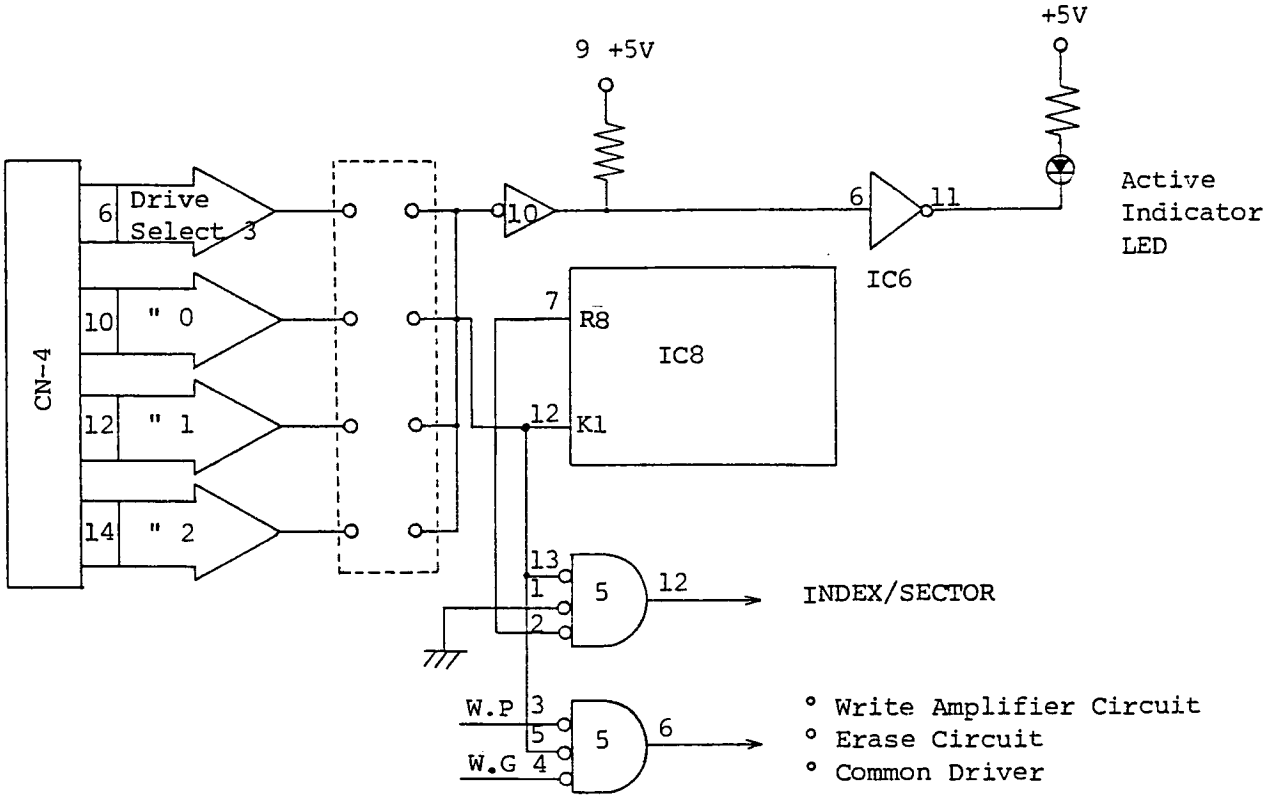
(Top View)

Block Diagram



5. INPUT SIGNAL LINES (CPU to FDD)

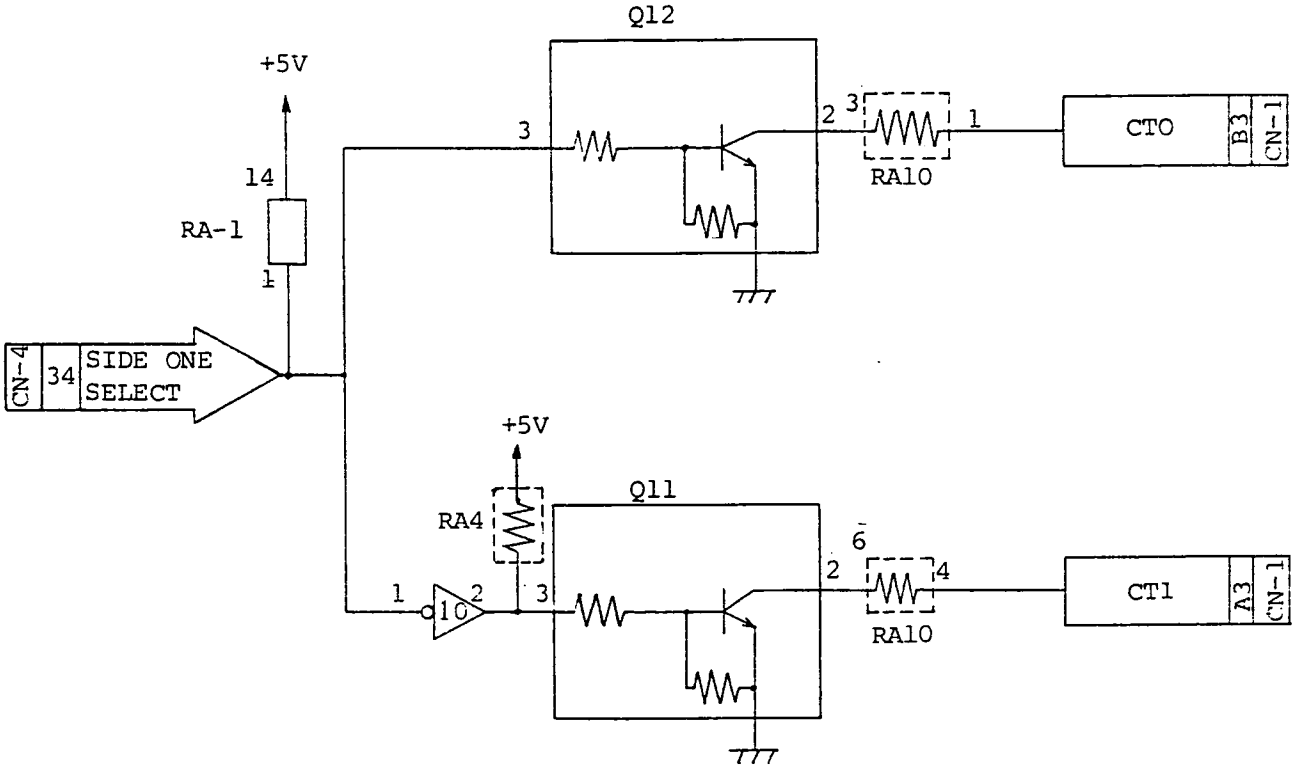
5.1 Drive Select Circuit



When one of these four signal lines goes low, the FDD corresponding to the low level line responds to other input signals, and further the gate of the output signal line of the FDD opens.

Up to four FDDs are controllable. Which of DRIVE SELECT 0~3 the FDD corresponds to is selected by inserting one short plug in the FDD. When selected by the shorting jumper, the "Low" level DRIVE SELECT signal is input to pin 12 of IC8 to place the CPU (control LSI) in a selected state. Also, this signal allows the LED on the front panel to illuminating through the motor driver (IC6).

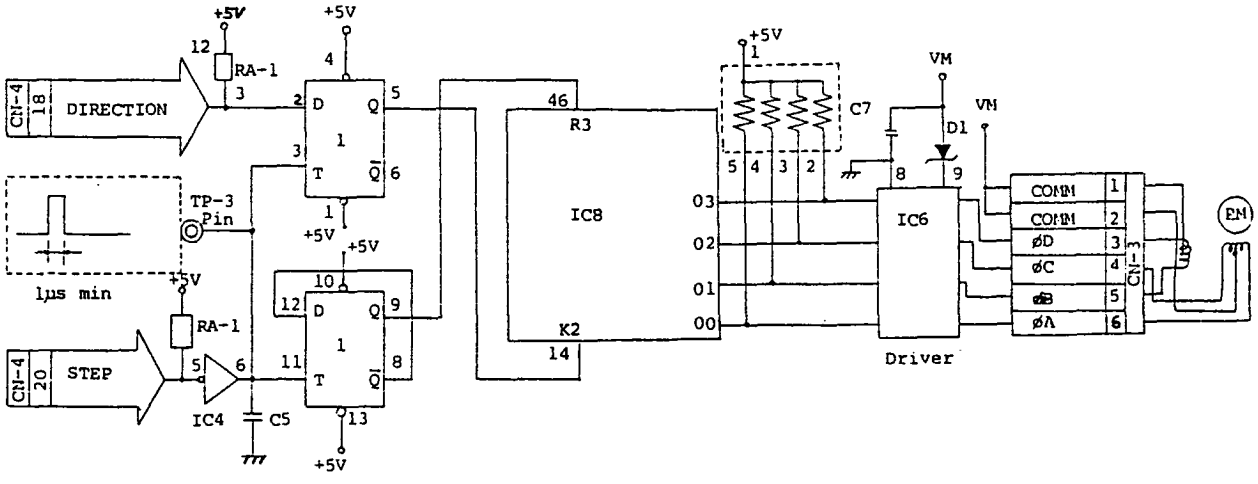
5.2 Side Select Circuit



This circuit is used to select either side 0 or side 1 head.

A low on this input signal line causes side 1 head to be selected and a high on this line causes side 0 head to be selected. Waiting time is required between the instance at which the selection is completed upon the change of the SIDE SELECT signal and the instance at which write/read is enabled. However, this signal must not be changed until the erasing is completed after the completion of writing because of the tunnel erase system employed. For the tunnel erase system, refer to (2) in section 5.6 Erase Circuit.

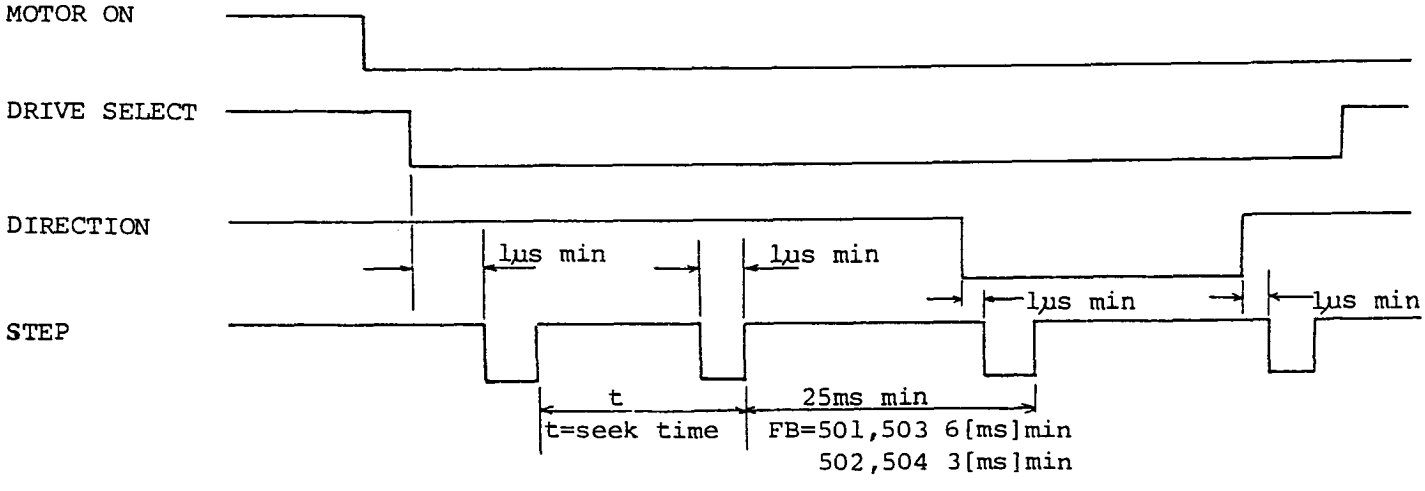
5.3 Head Positioning Circuit



The head positioning circuit is configured as shown above.

This circuit is used to move the head using step pulses, after the head stepping direction (inner or outer direction) is determined by the Direction signal. When the Direction signal from the host computer goes low and a step pulse signal is inputted, the head steps one track in the inner direction. When the Direction signal goes high, the head steps in the outer direction.

The timing chart for the Direction signal and Step signal is shown below.



In writing or reading data, it is necessary to wait for seek + setting time after the final step signal to stabilize the head.

5.4 WRITE GATE Signal

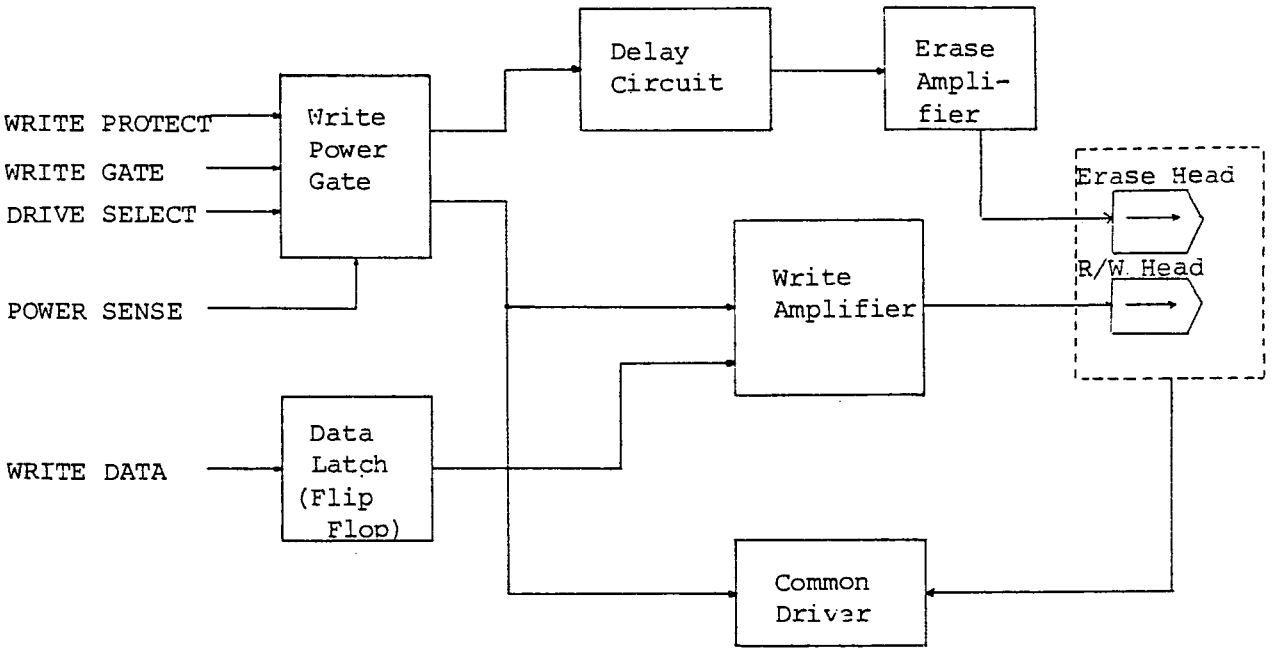
When the WRITE GATE input signal line of this circuit is low, the write circuit is made operable. However, writing will not occur, When the WRITE PROTECT output signal line is low (in a write desable state) or the corresponding FDD is not selected by the DRIVE SELECT signal line. When this input signal line is high, the FDD is in the read mode.

5.5 WRITE DATA Signal

This input signal line is used to transfer data to be written on the disk.

When the FM- or MFM-modulated signal turns from "High" to "Low" level, reverse current flows through the head to generate magnetic flux changes in it to write data on the disk. This input signal line is valid only when the WRITE GATE and DRIVE SELECT input signal lines are low and the WRITE PROTECT output signal line is high.

5.6 Write Circuit and Erase Circuit



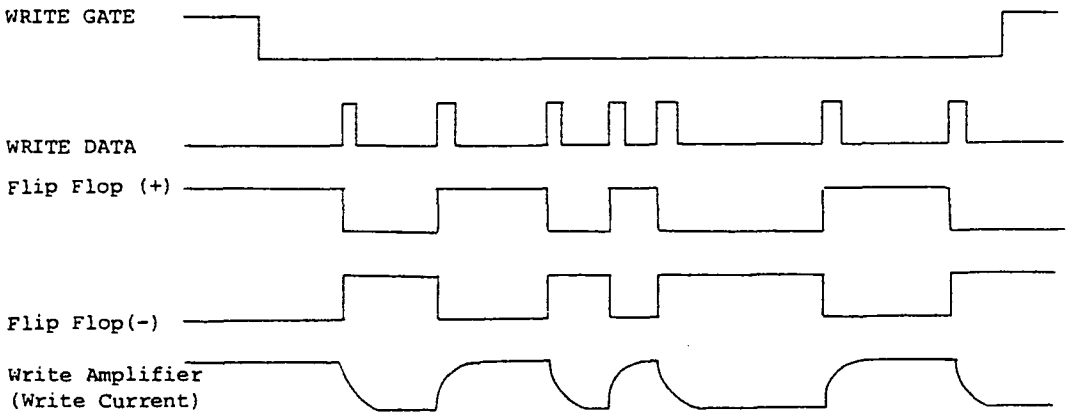
(1) Write Circuit

The block diagram for the write circuit and erase circuit is shown above.

The write data modulated in the FM or MFM system is divided by the data latch (flip flop) to become a WRITE DATA pulse. The write amplifier output signal becomes a rectangular signal that is inverted by this WRITE DATA pulse. In other words, the write amplifier inverts the polarity of the head current through this signal to cause the magnetic flux synchronized with the WRITE DATA pulse to be generated in the gap of the read/write head and the media is saturation-magnetized and recorded.

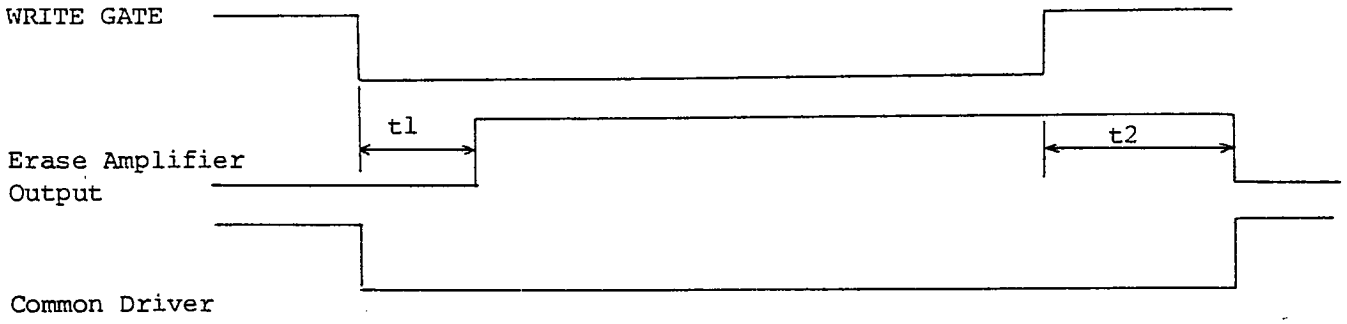
The write power gate opens only when the WRITE PROTECT output signal line is high and the WRITE GATE and DRIVE SELECT input singal lines are low, enabling writing and erasing.

The timing chart for the write circuit is shown below.

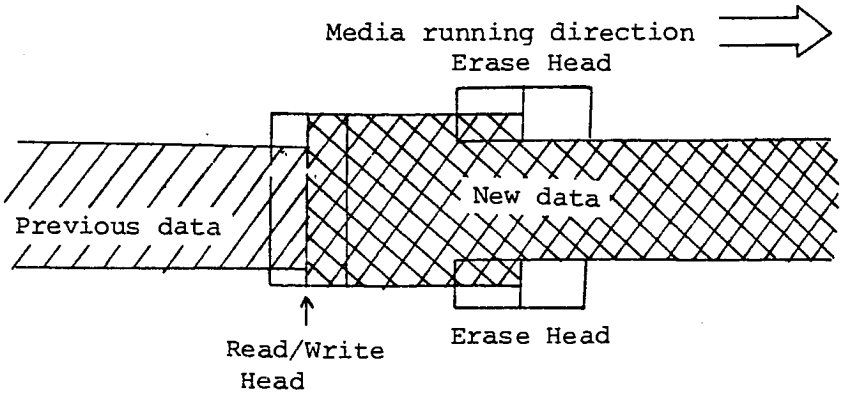


(2) Erase Circuit

The timing chart for the erase circuit is shown below.



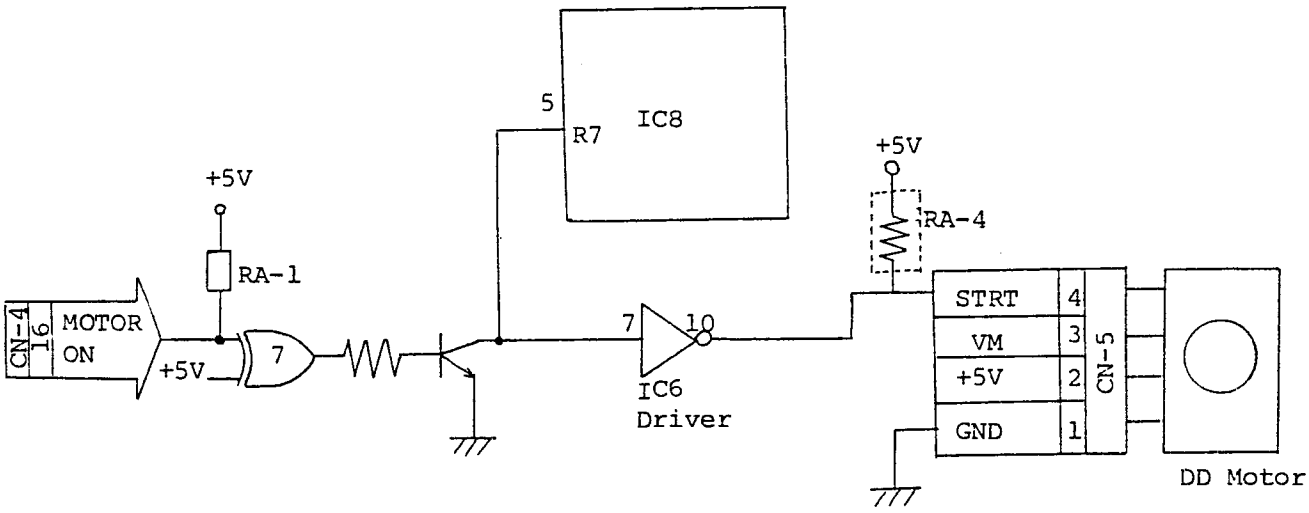
The tunnel erase system is adopted for this FDD. It consists of a broad-width read/write head followed by a tunnel earse head designed to allow the inner dimension to have the recording information track width. The information once recorded through the read/write head is trimmed at both edges by the tunnel erase head to be shaped to the desired track width. By doing this, even if track divergence occurs, it will not interfere with the adjacent track because the signals for the information track width are efficiently secured by the broad-width read/write head, thus securing the S/N ratio and improving the track density.



For this reason, the erase amplifier output signal rises t1 seconds (minimum time required for the location written on the disk by the read/write head to reach the erase head) after the WRITE gate signal turns from "High" to "Low" level, causing current to flow through the erase head to perform DC erasing. Then, the erase amplifier output signal falls t2 seconds (maximum value of time difference of above t1) after the completion of writing on the media (when the WRITE GATE signal rises), thereby completing the DC erasing.

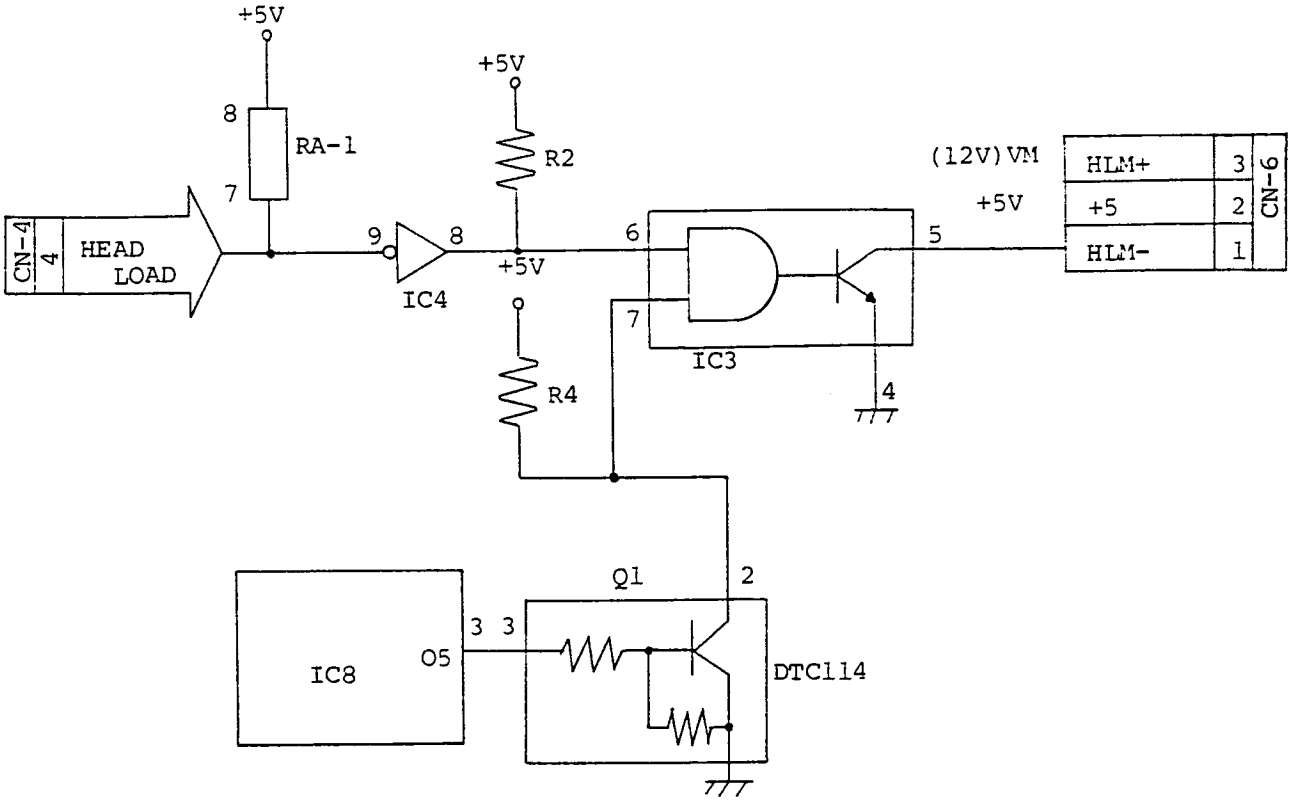
T1 and T2 seconds are software-determined by the delay circuit.

5.7 MOTOR ON Signal



A spindle motor drive signal appears on this input signal line. When the input signal is low, the spindle motor turns. The disk should be inserted or taken out while the spindle motor is turning. Conversely, when the signal is high, the motor stops. This signal line responds regardless of the DRIVE SELECT signal. The start-up time for the spindle motor requires 0.5 seconds.

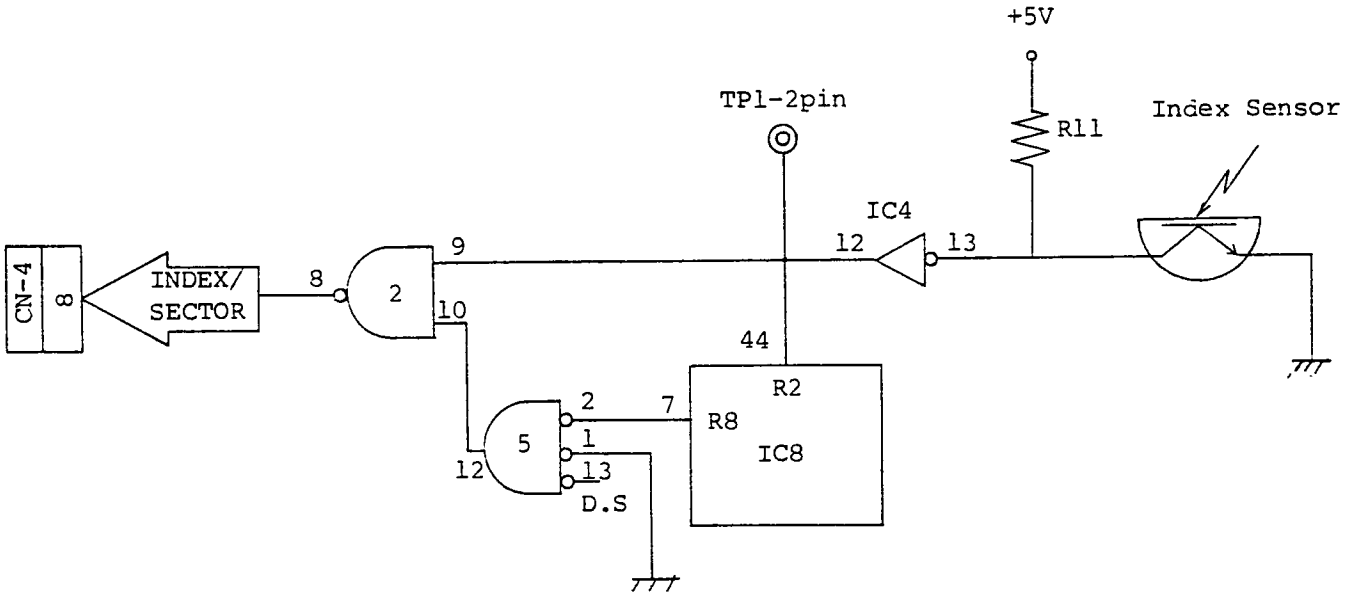
5.8 Head Load Circuit (Option)



This circuit assumes the head load state only when the HEAD LOAD signal is low, LSI (IC8) is ready (the media is turning), and signal 05 is low, enabling reading or writing of data. The use of this input signal line requires a setup time for the magnet. This function is available in the two-side type only. When no media is set, head loading is not performed.

6. OUTPUT SIGNAL LINE

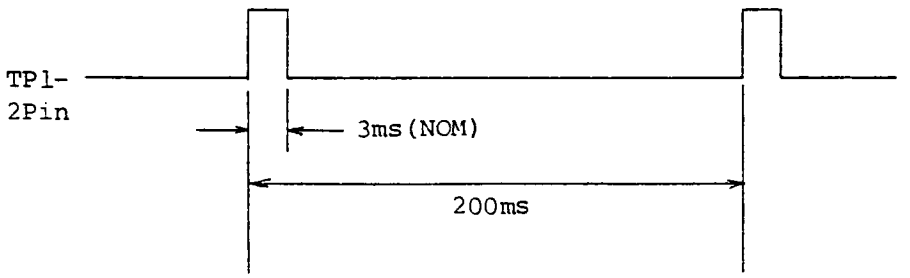
6.1 Index/Sector Circuit



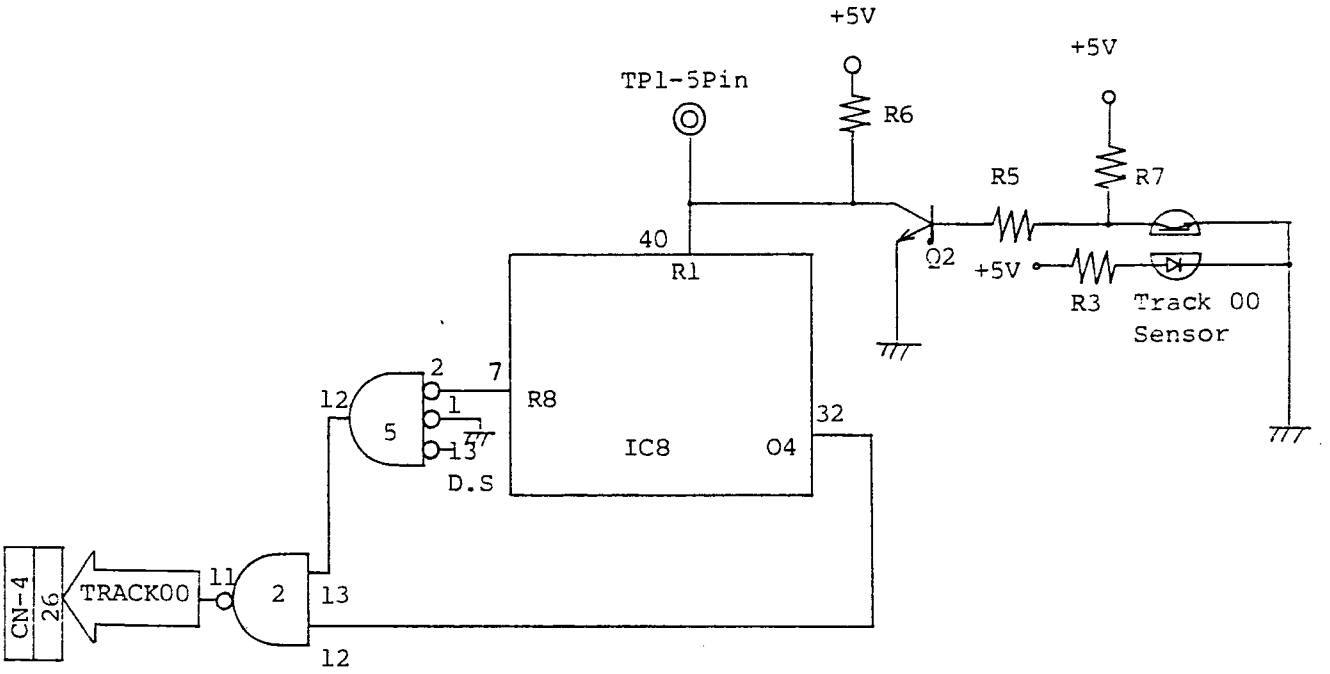
The index/sector circuit is configured as shown above.

When the index sensor detects the index hole in the disk, this output signal line goes low indicating the beginning of a track.

The waveform of TP1, pin 2, while the media is turning is shown below.



6.2 Track 00 Detection Circuit

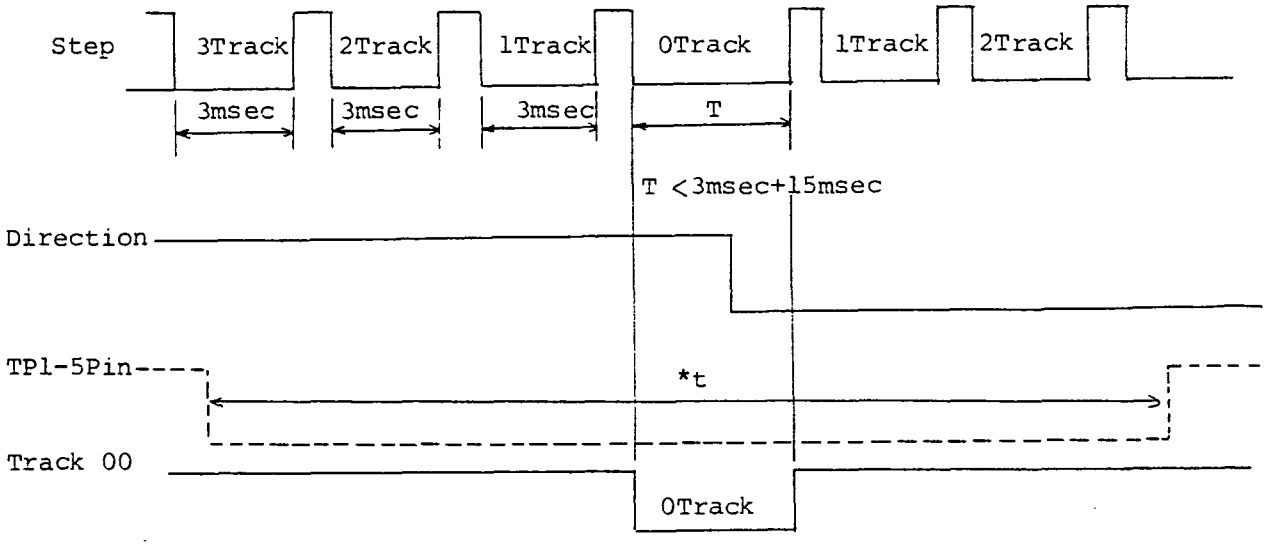


The track 00 detection circuit is configured as shown above.

This circuit detects track 00 which is the outermost track of the disk, and the detected signal is loaded into IC8. The "Low" level signal at the time of track 00 is inputted to R1 of IC8. the "High" level signal in other cases.

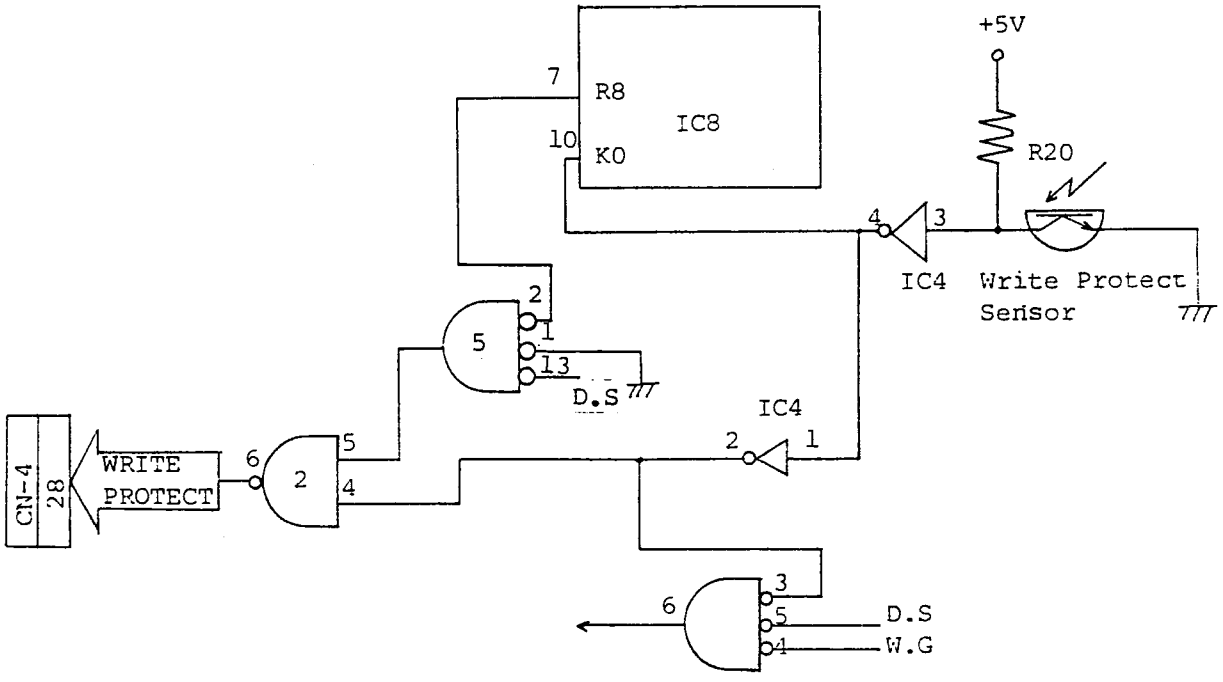
When the carrier is at a track other than track 00, the light of the interrupter LED strikes the phototransistor, causing the output signal line to be at a "High" level.
When the carrier is positioned over track 00, the light of the LED is cut off, the "Low" signal is inputted to IC8.

The waveform at TP1, pin 5, is shown below.



* The t varies according to the specification.

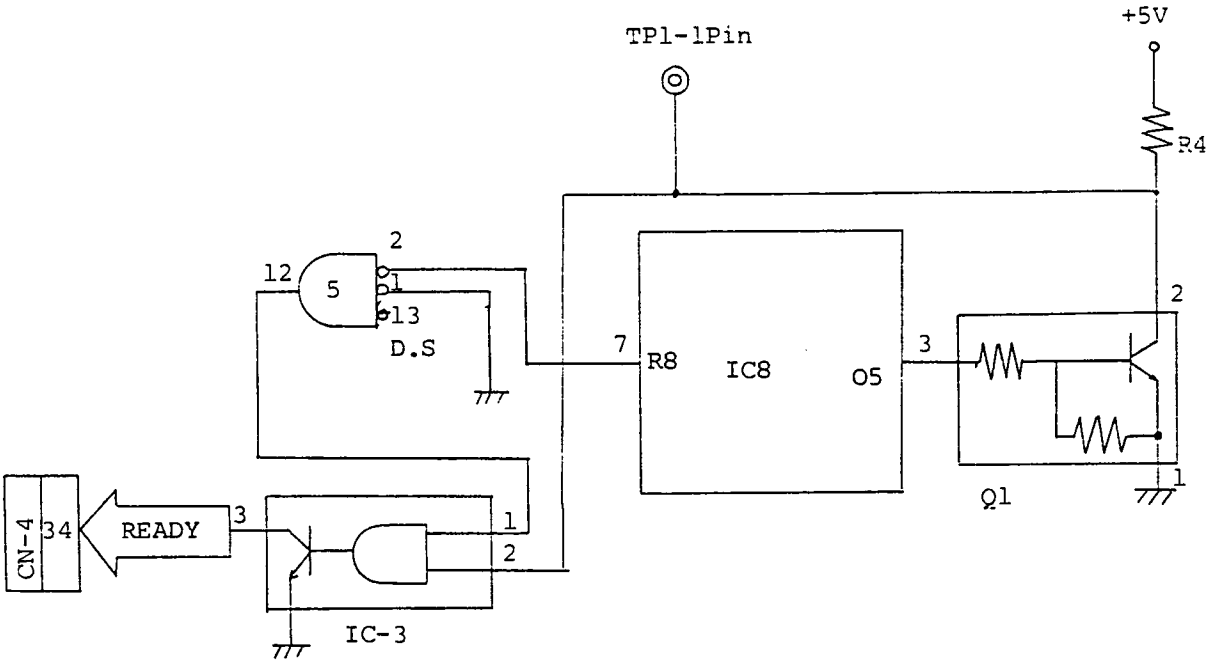
6.3 Write Protect Circuit



This circuit is provided to prevent erroneous erasing of protected data recorded on the disk.

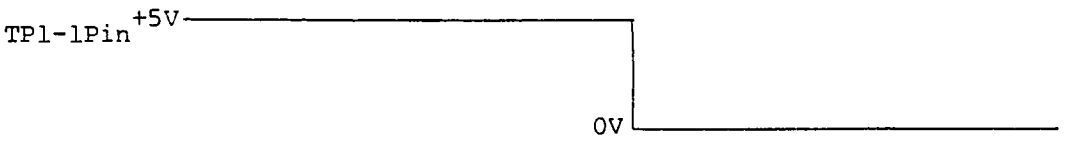
The "Low" level signal is outputted when the write enable notch of the disk, inserted into the FDD, is covered with a label, thus disabling writing to the disk. Conversely, when the "High" level signal is outputted, the write enable state is assumed.

6.4 READY Signal (Option)

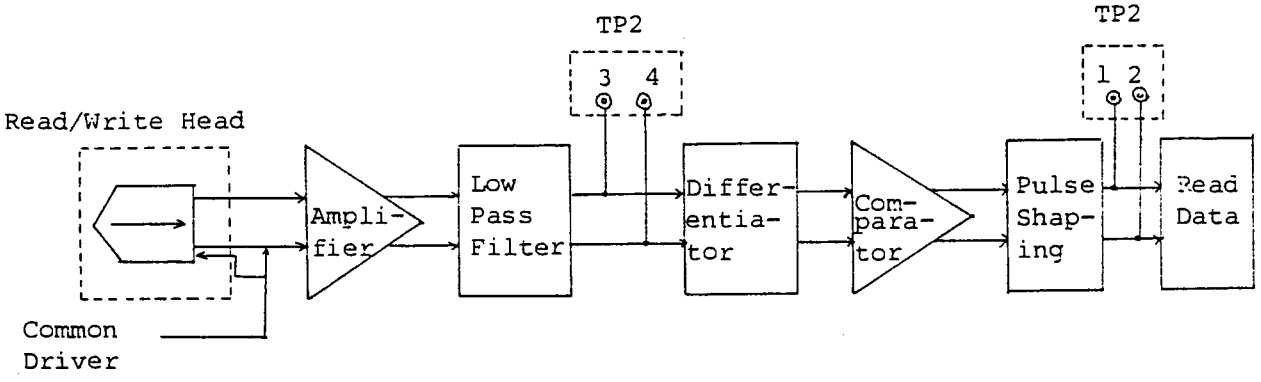


This READY signal line is optional in the FB-503-504.
When the inserted disk is turning, the output signal line goes low. Consequently, two items, the disk inserted and turning conditions, can be checked by this signal line.

The following waveform appears at check pin TP1, pin 1.
The "High" levle of this waveform indicates the Busy state, and the "Low" level the Ready state. When the index detection circuit detects the index, the signal turns from a "High" to a "Low" level.



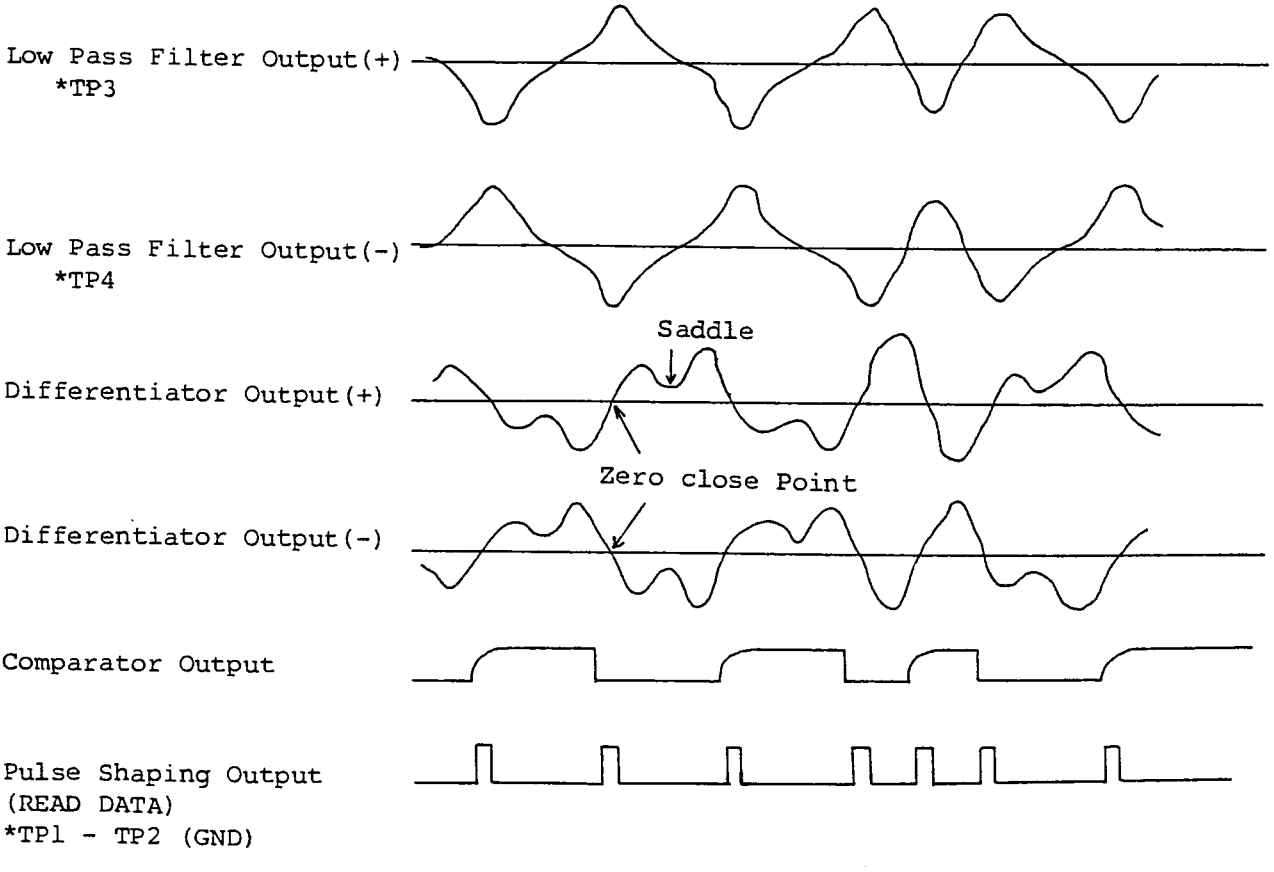
6.5 Read Amplifier Circuit



The block diagram for the read amplifier is shown above.

This circuit picks up data recorded on the media through the magnetic head, and outputs read data close to the recorded signals by amplifying, although it slightly deviates time-wise, identifying, and pulse-shaping the data.

The timing chart for the read amplifier circuit is shown below.



CHAPTER 4 Circuit Diagram

(FB-500 Series)

Chapter 5 Troubleshooting

(FB-500 Series)

CONTENTS

1. Soft Error Processing

1.1 General

The following soft errors are often mistakenly for errors caused by troubles or mis-adjustments of the disk drive.

- o Errors caused by improper operational procedure, incorrect programming or damaged disk.
- o Software error caused by dust in the air, random electric interference or other external cause.

Unless a defective assembly point or damage point is clearly found in visual inspection, check to see whether the error repeats with the current diskette and also whether the same error is caused with other diskette.

1.2 Detection and Correction and Read Error

Read errors are usually caused by the following conditions.

(1) Dust between the read/write head and disk; usually dirt resulting from dust is eliminated by the self-cleaning wiper in the diskette.

(2) Fine track divergence which is not detected during writing.

(3) Wear of damaged load pad or wear of disk caused by side 0 or side 1 of double-side head.

(4) Improper grounding of the power supply of the disk drive in the host computer.

(5) Improper motor speed.

To correct soft errors as above (1) to (5), follow the steps below.

(1) Re-read the error-occurred track about 10 times.

(2) If the data is not restored in step 1, allow the head to move to track 00 and make sure that the head is at track 00.

(3) Move the head to the error-occurred track.

(4) Repeat step (1).

(5) Errors which cannot be corrected by repeating the above steps are unrecoverable errors.

1.3 Write Error

An error which has occurred during writing is detected during a subsequent reading of the data written.

(1) To eliminate the error, write and read again.

(2) If the error still occurs after the above procedure is repeated a few times, perform reading using another track to determine whether the disk or drive is malfunctioning.

(3) If the error persists, change the disk and perform the above procedure.
If the error still persists, the drive is defective.

1.4 Seek Error

Possible Cause.

(1) The pulse motor or pulse motor drive circuit is defective.

(2) The carriage is defective.

There are two procedures to correct seek errors.

(1) Readjust the belt tension. —— Refer to Chapter 2.

(2) Readjust track 00. ———— Refer to Chapter 2.

1.5 Interchange Error

Sometimes data written by a disk drive cannot be read by another drive. This phenomenon is called "interchange error".
The points to be checked are:

(1) Head alignment is defective ... Refer to Head/Radial Adjustment.

(2) Head output is not enough ... Refer to Head Output Adjustment.

(3) The motor speed is incorrect ... Refer to Motor Speed Adjustment.

(4) Check the center hole of the disk.
If the center hole of the disk is damaged, check the clamp mechanism.

2. FLOPPY DISK DRIVE FOR REPAIR

2.1 Have the user send you the defective floppy disk drive together with the diskette which was used when the user found it defective. Without this diskette, you may fail to locate the trouble.

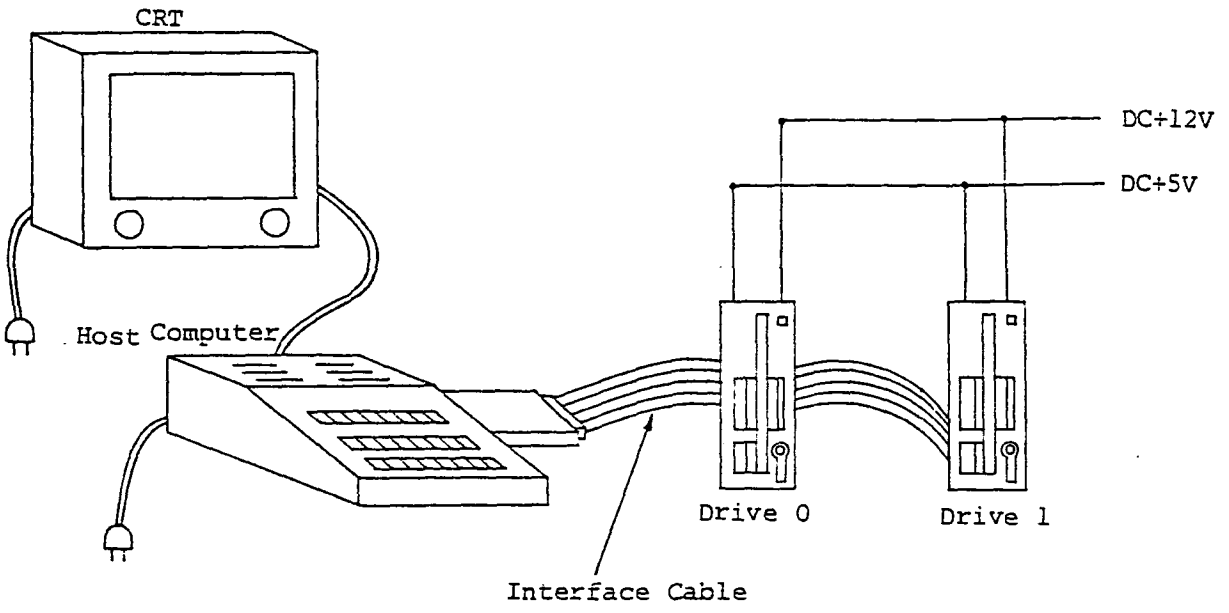
2.2 Be sure to get information from the user about the operating conditions at the time the user found the floppy disk drive defective. This will help in troubleshooting later.

a) If the Active lamp will not light and the unit does not operate at all, check the DC Power Supply.

b) If the Active lamp lights but an operating sound is not heard inside the unit, proceed to section 2.1.

c) If stepper motor turns without causing carriage movement, proceed to section 2.

d) If the drive executes continuously but fails to read and write, proceed to sections 2.2 and 2.3.

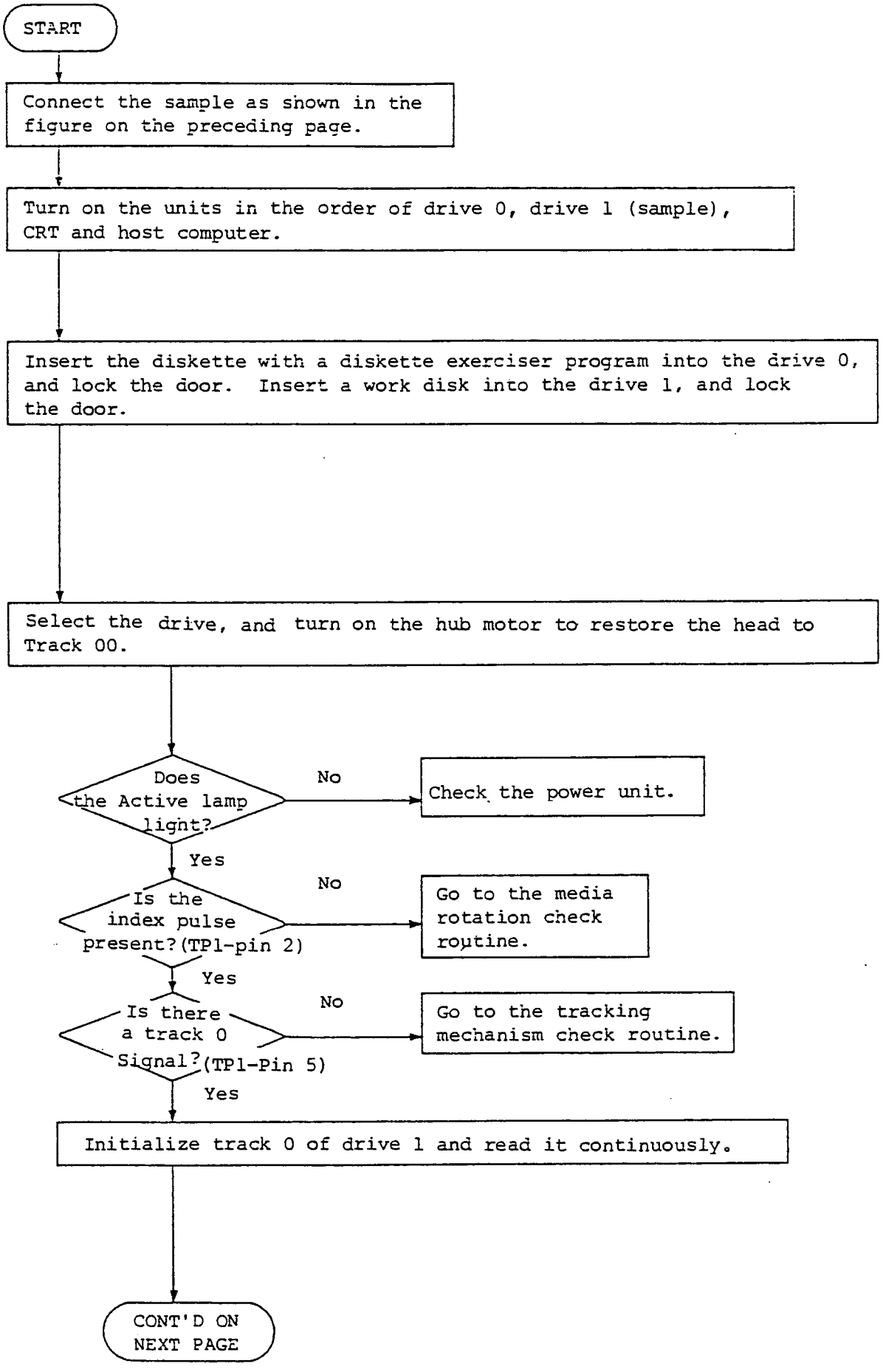


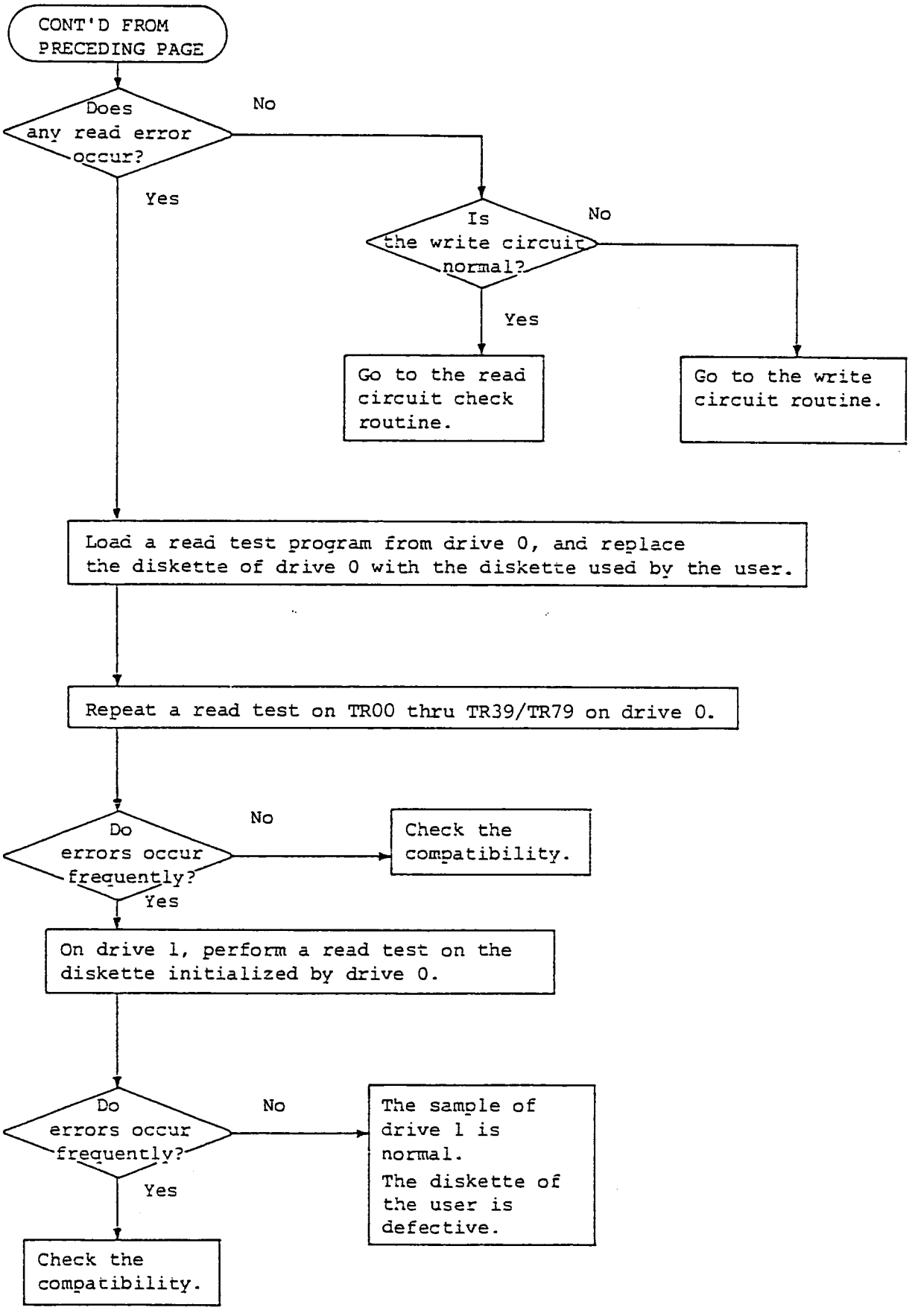
Sample Test Connection

Drive 0: Normal Drive

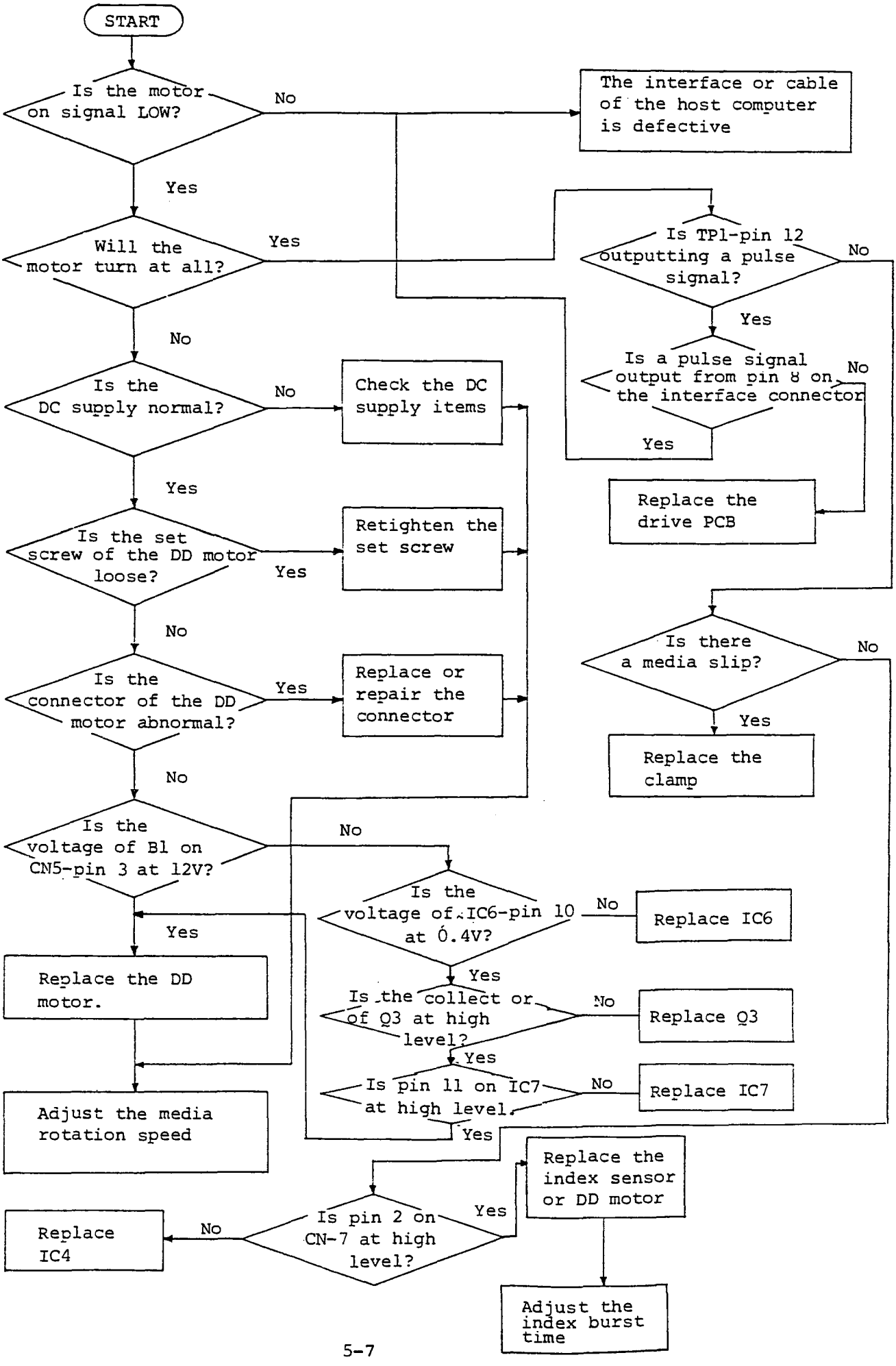
Drive 1: Sample Drive

3. TROUBLESHOOTING PROCEDURES

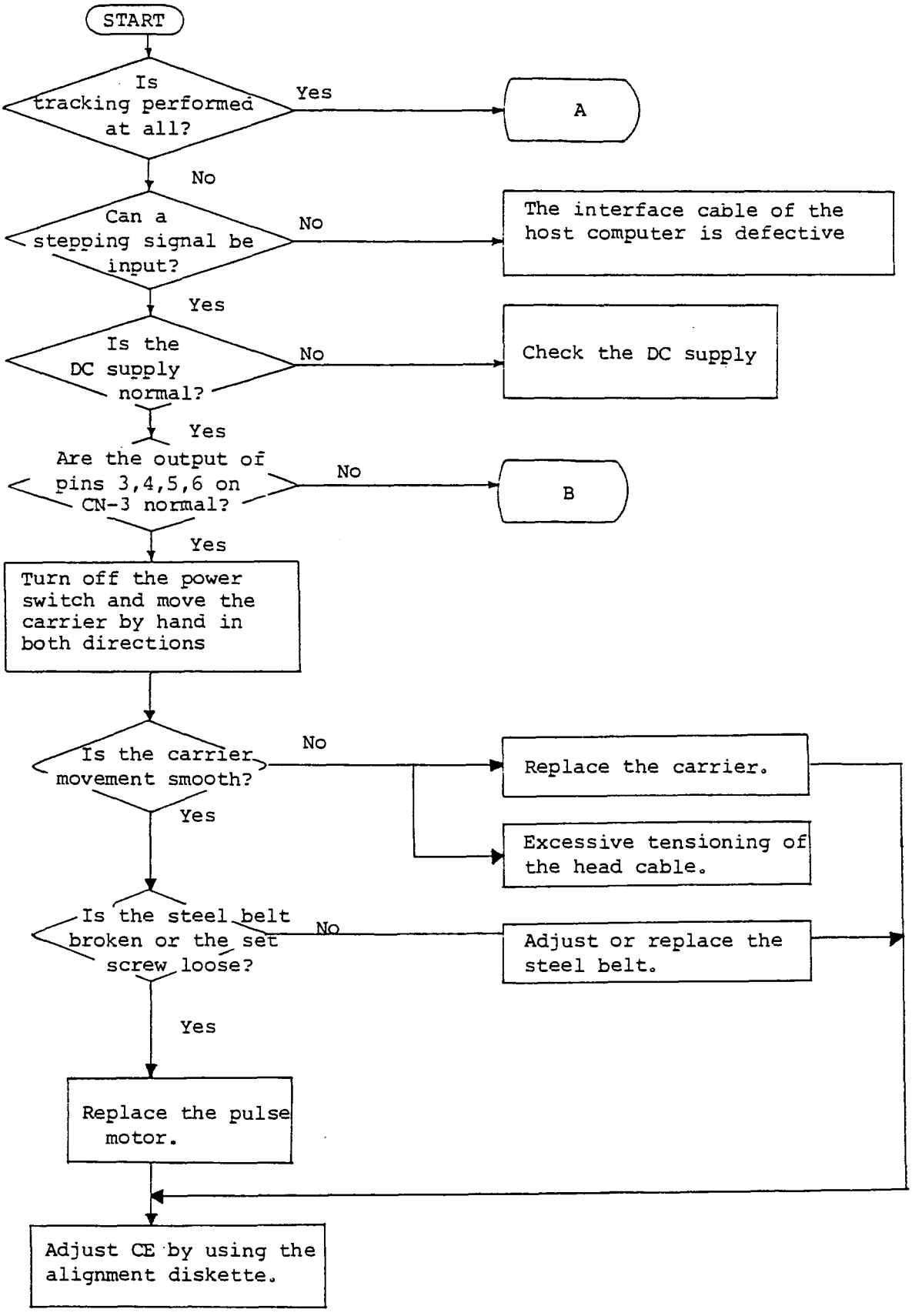


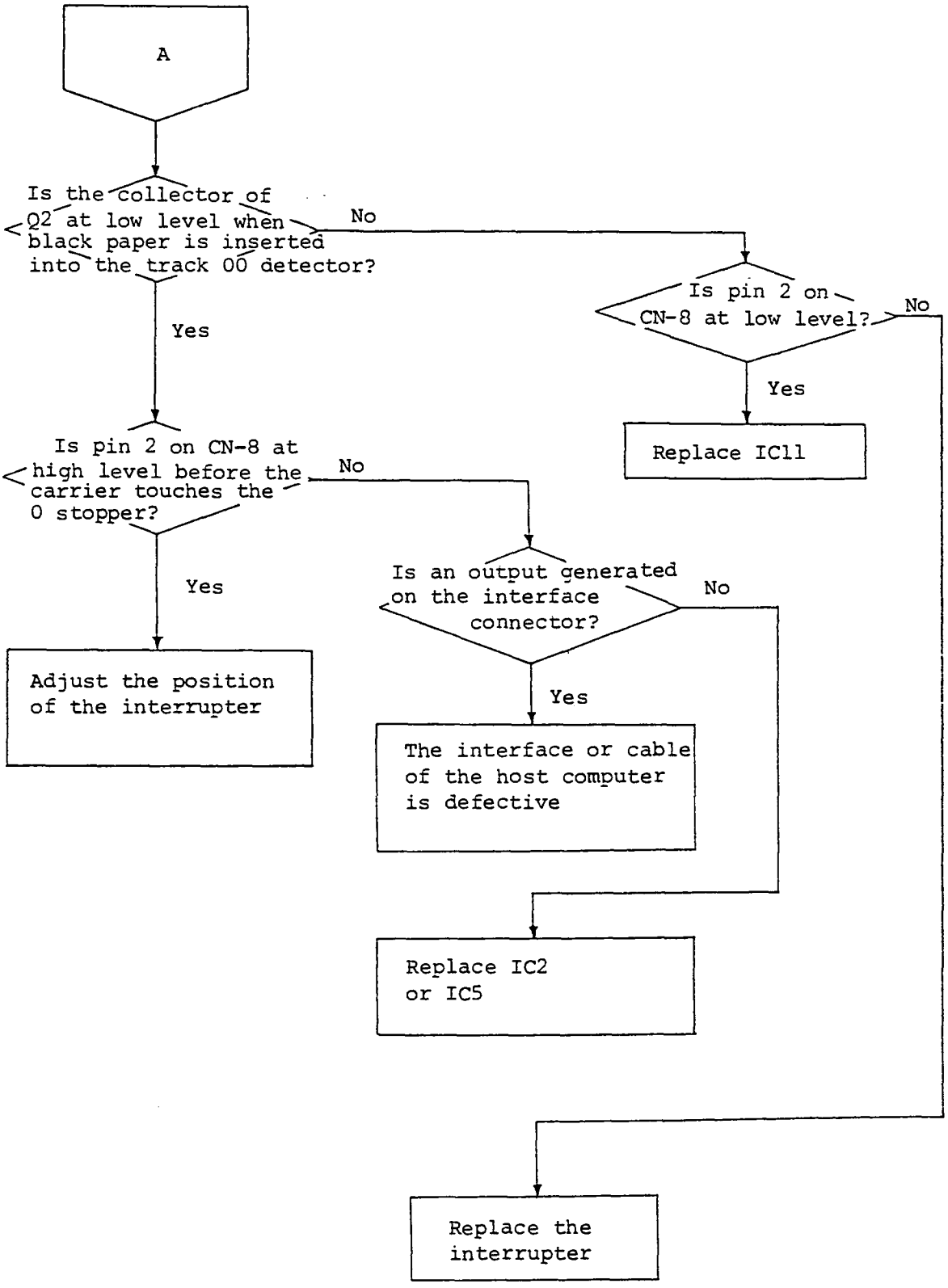

CONT'D FROM PRECEDING PAGE
Does any read error occur?
No
Yes
Is the write circuit normal?
No
Yes
Go to the read circuit check routine.
Go to the write circuit routine.
Load a read test program from drive 0, and replace the diskette of drive 0 with the diskette used by the user.
Repeat a read test on TR00 thru TR39/TR79 on drive 0.
Do errors occur frequently?
No
Check the compatibility.
Yes
On drive 1, perform a read test on the diskette initialized by drive 0.
Do errors occur frequently?
No
The sample of drive 1 is normal.
The diskette of the user is defective.
Yes
Check the compatibility.

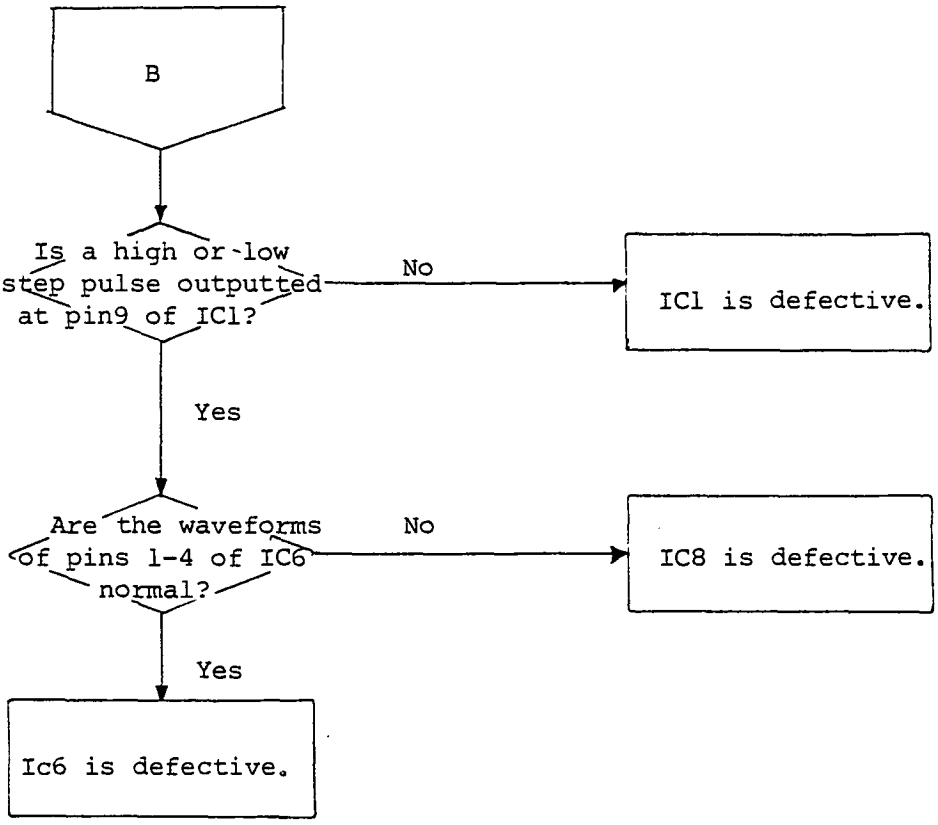
MEDIA ROTATION CHECK



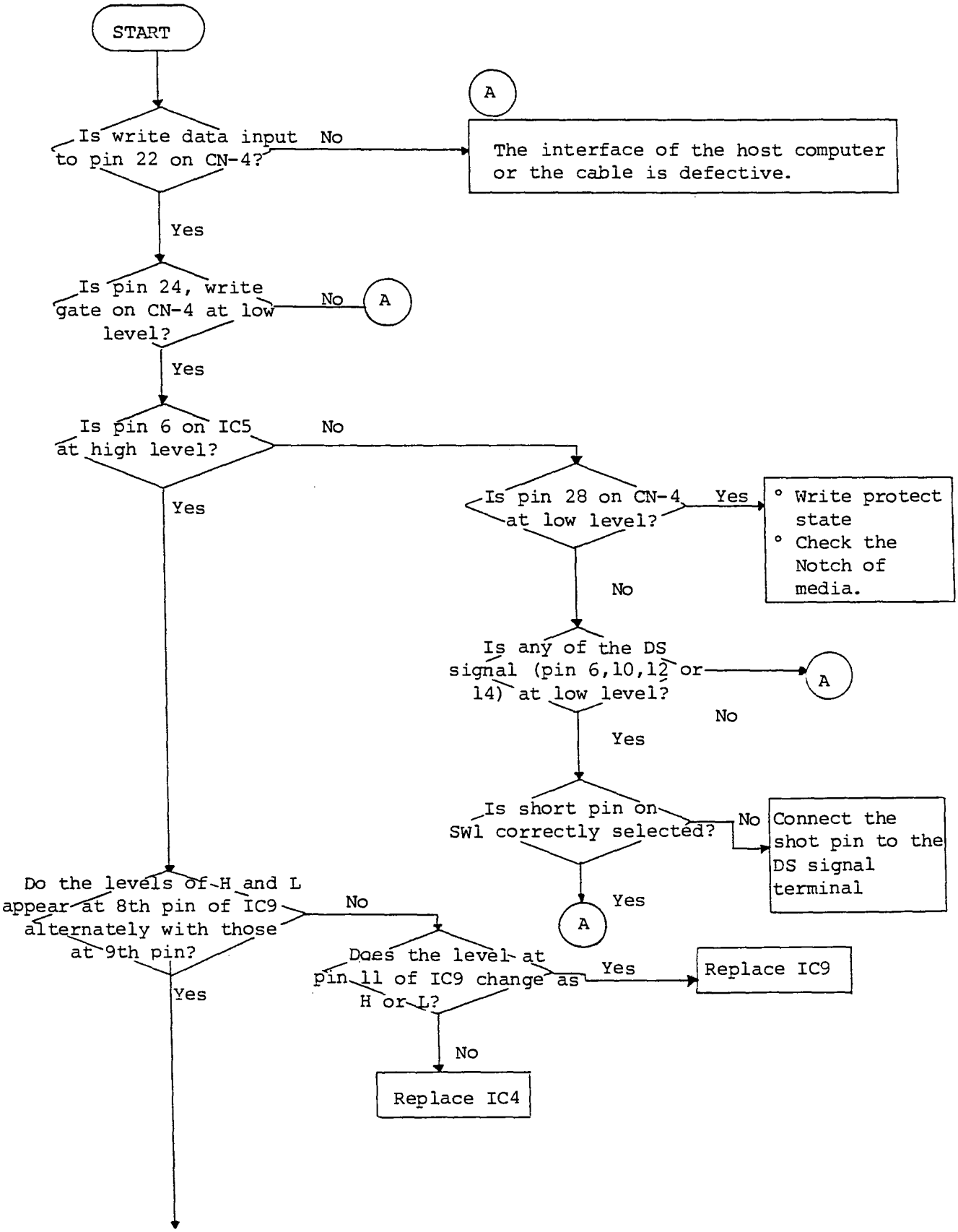
3.1 Tracking Mechamism (Track 0 Signal Won't Be Generated)

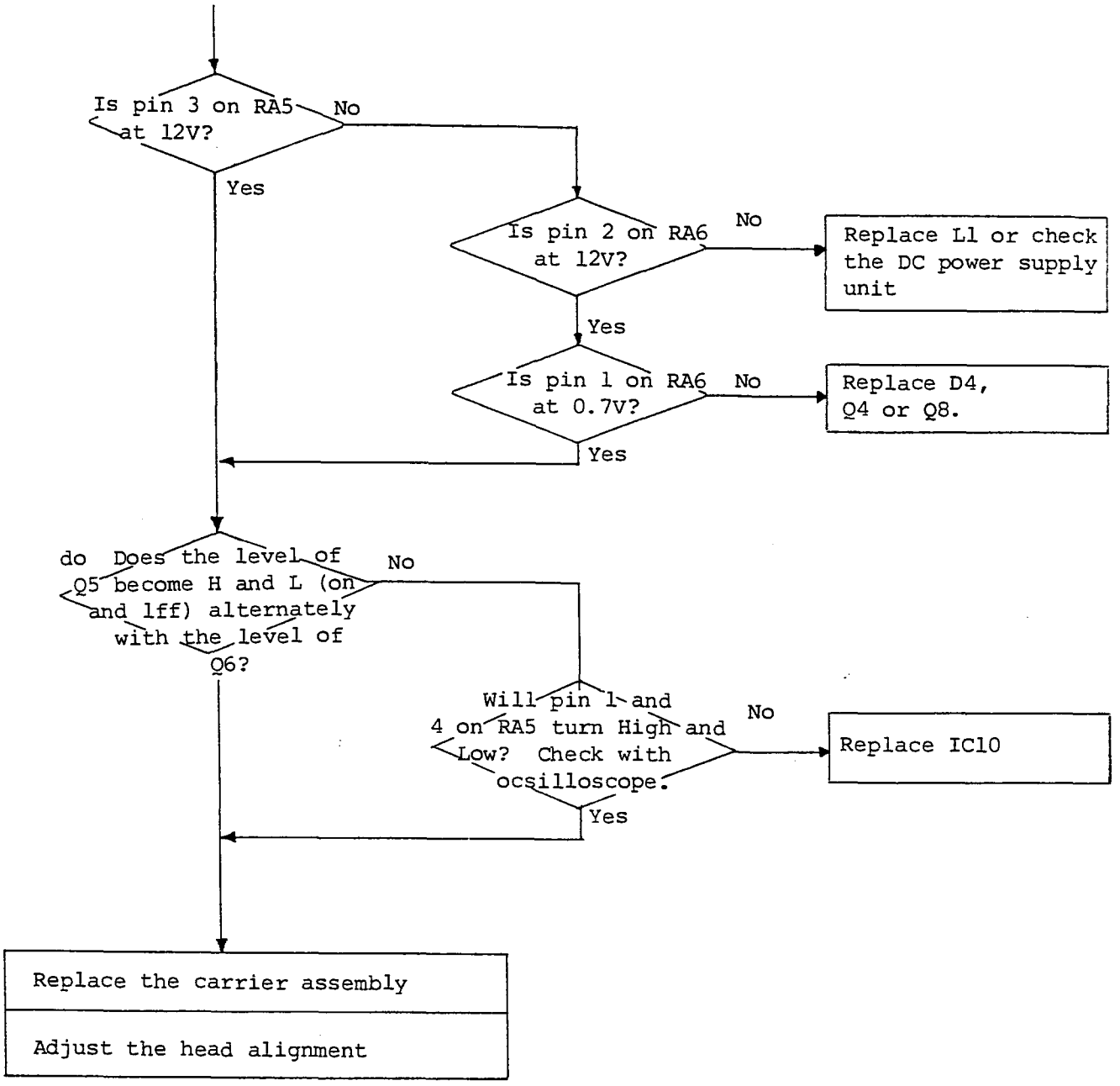



A
Is the collector of Q2 at low level when black paper is inserted into the track 00 detector?
No
Yes
Is pin 2 on CN-8 at low level?
No
Yes
Replace IC11
Is pin 2 on CN-8 at high level before the carrier touches the 0 stopper?
No
Yes
Adjust the position of the interrupter
Is an output generated on the interface connector?
No
Yes
The interface or cable of the host computer is defective
Replace IC2 or IC5
Replace the interrupter

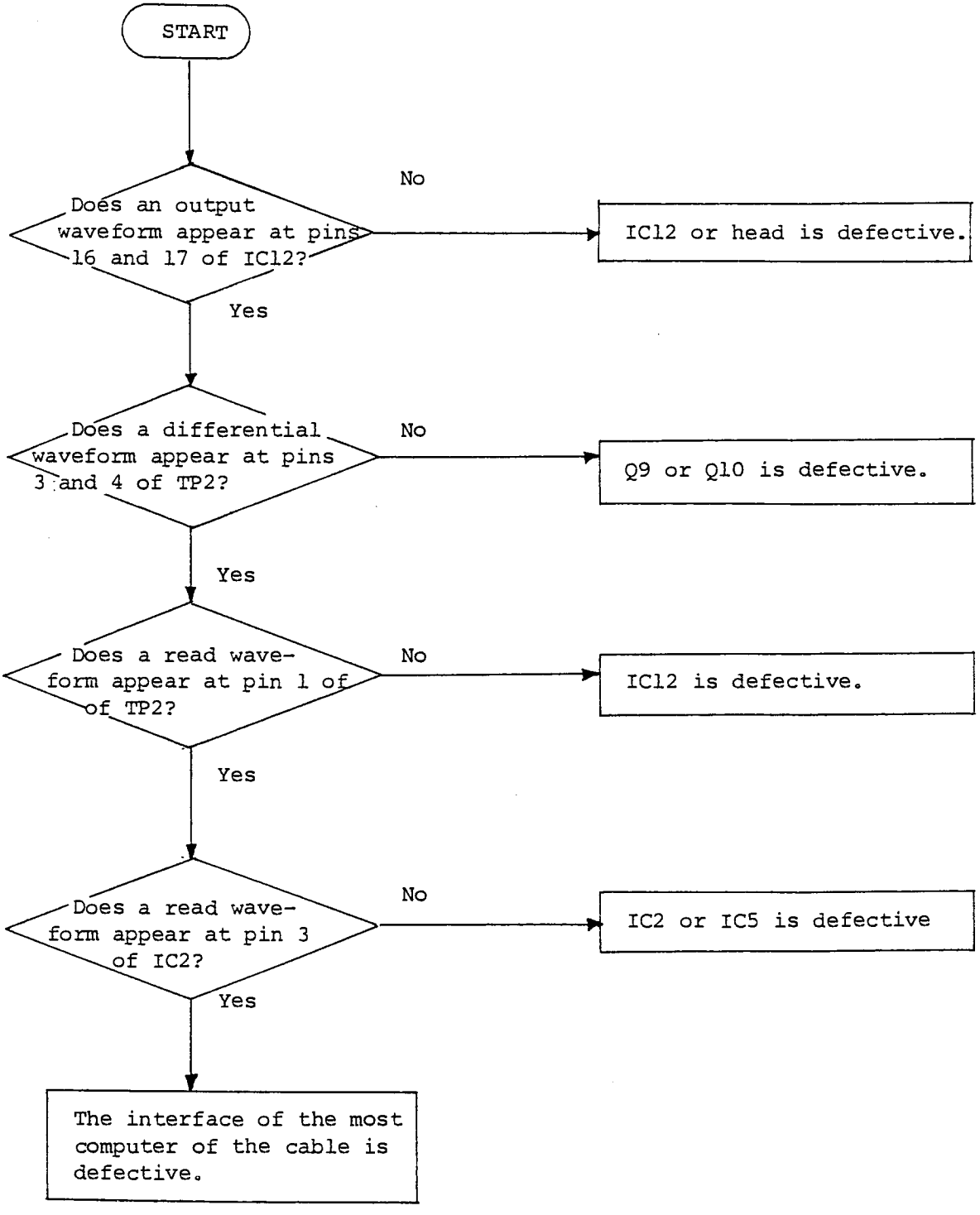

B
Is a high or low step pulse outputted at pin9 of IC1?
No
IC1 is defective.
Yes
Are the waveforms of pins 1-4 of IC6 normal?
No
IC8 is defective.
Yes
Ic6 is defective.

3.2 Write Circuit Check




Is pin 3 on RA5 at 12V?
No
Yes
Is pin 2 on RA6 at 12V?
No
Replace L1 or check the DC power supply unit
Yes
Is pin 1 on RA6 at 0.7V?
No
Replace D4, Q4 or Q8.
Yes
do Does the level of Q5 become H and L (on and lff) alternately with the level of Q6?
No
Will pin 1 and 4 on RA5 turn High and Low? Check with ocsilloscope.
No
Replace IC10
Yes
Replace the carrier assembly
Adjust the head alignment

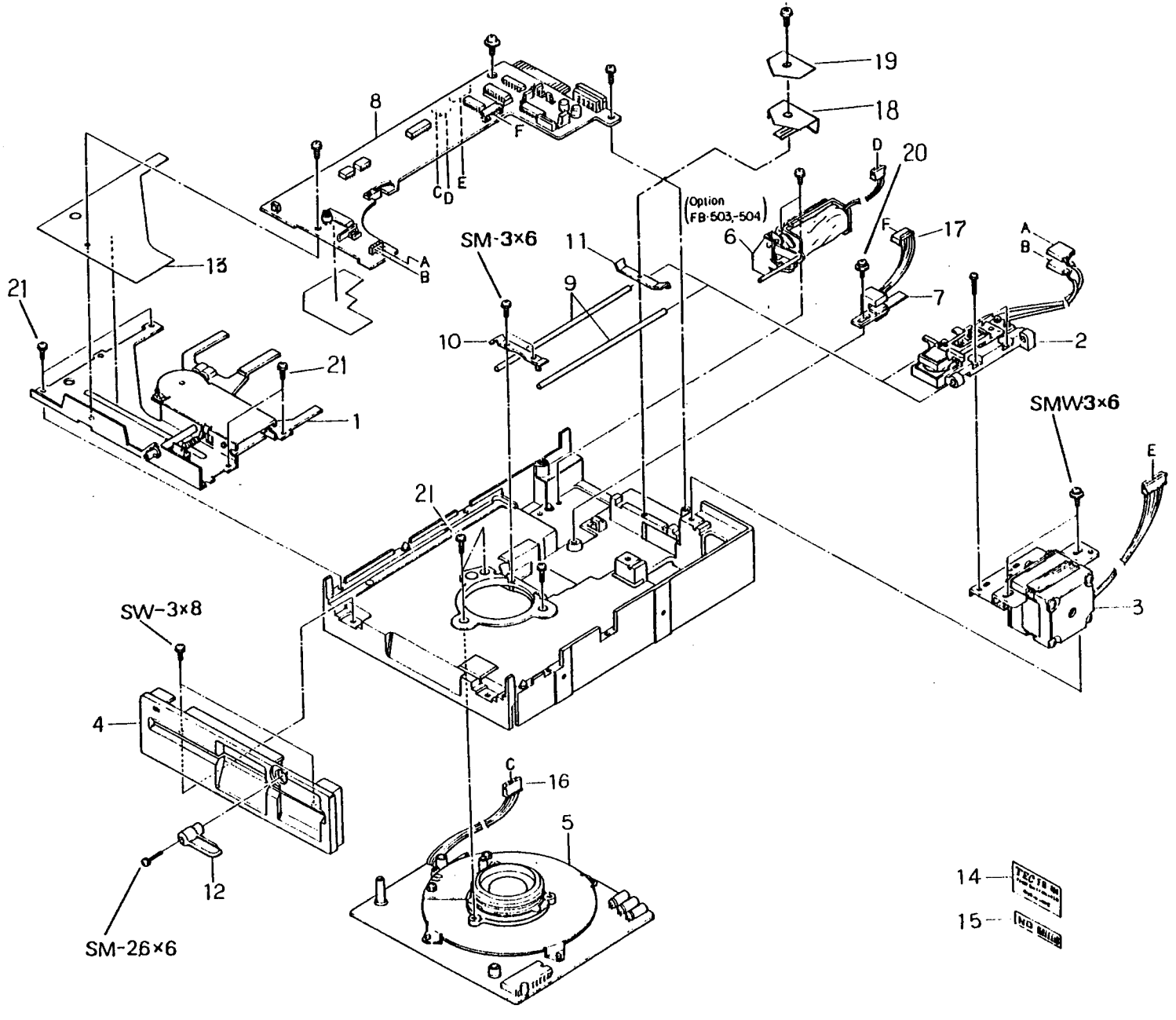
Read Circuit Malfunction



CHAPTER 6 Parts List

(FB-500 Series)

DOCUMENT NO.E5-2125

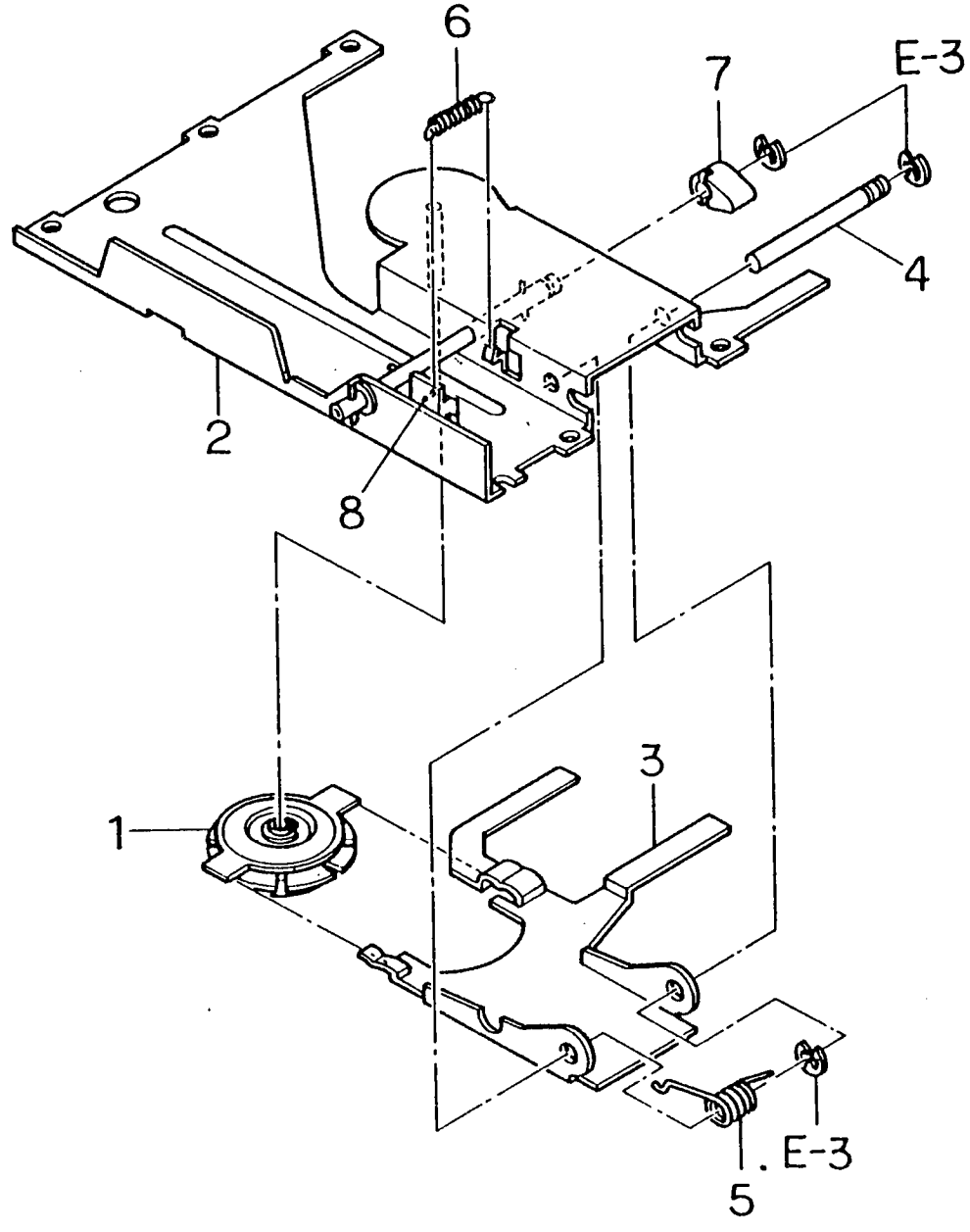

19
18
20
8
F
C
D
E
A
B
(Option
FB-503,-504)
6
D
F
17
A
B
SM-3×6
11
9
10
7
2
13
21
21
1
21
SMW3×6
E
3
SW-3×8
4
C
16
5
12
SM-26×6
14
15
NO MIL

1 MAIN UNIT 1/2

Ref. No.	Part No.	Part Name	Remarks	
1- 1	CFABK-60101	Clamp Base BK	501, 502, 503HL, 504HL	
	CFABK-60102	Clamp Base BK	503, 504ST	
1- 2	CFABK-60201	Carrier A BK	501	
	CFABK-60202	Carrier A BK	502	
	CFABK-60301	Carrier B BK	503	
	CFABK-60302	Carrier B BK	504	
1- 3	CFABK-60401	Pulse Motor BK	502, 504	
	CFABK-60402	Pulse Motor BK	501, 503	
1- 4	CFAAK-60801	Front Cover K		
1- 5	CFAAK-60301	DD Motor K		
1- 6	CFABK-60501	Head Load BK	503, 504 Option	
1- 7	CFAAK-61201	Interrupter AK		
1- 8	CFEAK-05701	Drive AK	501	
	CFEAK-05702	Drive AK	502	
	CFEAK-05703	Drive AK	503	
	CFEAK-05704	Drive AK	504	
	CFEAK-05705	Drive AK	503HL	
	CFEAK-05706	Drive AK	504HL	
1- 9	CFA10-61201	Carrier Shaft		
1-10	CFA20-60601	Shaft Support IN		
1-11	CFA20-60701	Shaft Support OUT		
1-12	CFA35-60601	Clamp Lever		
1-13	CFA45-60901	Insulator		
1-14	CFA45-02605	Name Plate	501	

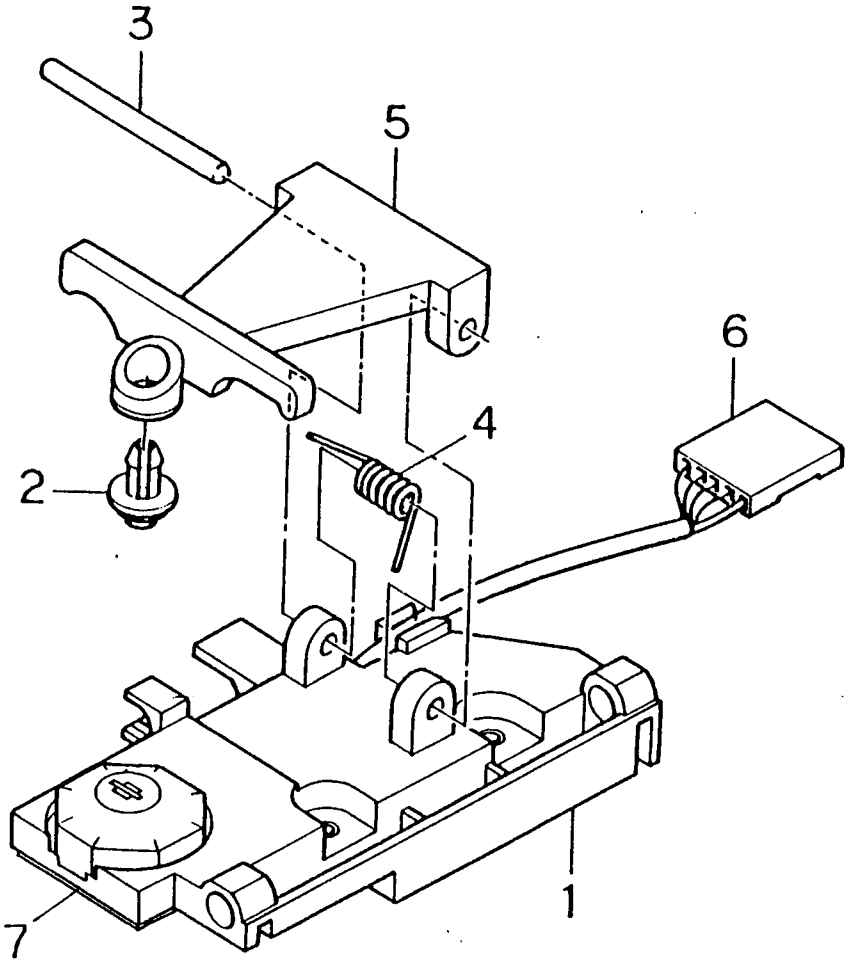
1 MAIN UNIT 2/2

Ref. No.	Part No.	Part Name	Remarks	
1-14	CFA45-02603	Name Plate	502	
	CFA45-02604	Name Plate	503	
	CFA45-02606	Name Plate	504	
1-15	CFA45-02503	PC Board Label	501	
	CFA45-02504	PC Board Label	502	
	CFA45-02505	PC Board Label	503	
	CFA45-02606	PC Board Label	504	
1-16	EEA00-87200	Connector 4-Pin Female		
1-17	EEA00-87300	Connector 5-Pin Female		
1-18	CFAAK-61301	Cable Guide K		
1-19	CFA45-61301	Inslating Plate B		
1-20	SSJ230060A2	Washer Screw		
1-21	CFA45-61401	Bind Machine Screw		


6
7
E-3
4
2
8
1
3
E-3
5

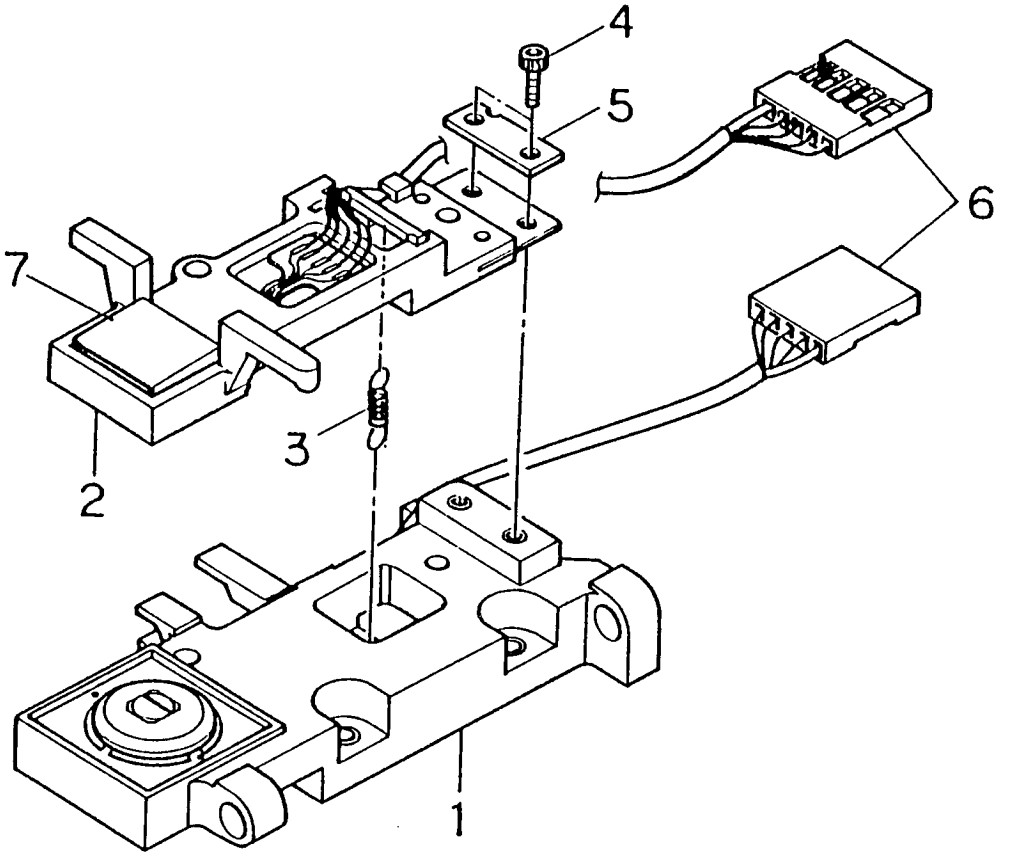
2 CLAMP BASE BK

Ref. No.	Part No.	Part Name	Remarks	
2- 1	CFABK-60601	Clmap BK		
2- 2	CFAAK-60101	Clamp Base K	501, 502, 503HL, 504HL	
	CFAAK-60102	Clamp Base K	503, 504	
2- 3	CFAAK-60201	Clamp Arm K		
2- 4	CFA10-60301	Clamp Lever Shaft		
2- 5	CFA30-60301	Clamp Lever Spring		
2- 6	CFA30-60601	Lock Cam Spring	503, 504	
2- 7	CFA35-60501	Clamp Cam		
2- 8	CFA35-60901	Clamp Lock Cam	503, 504	


3
5
6
4
2
1
7

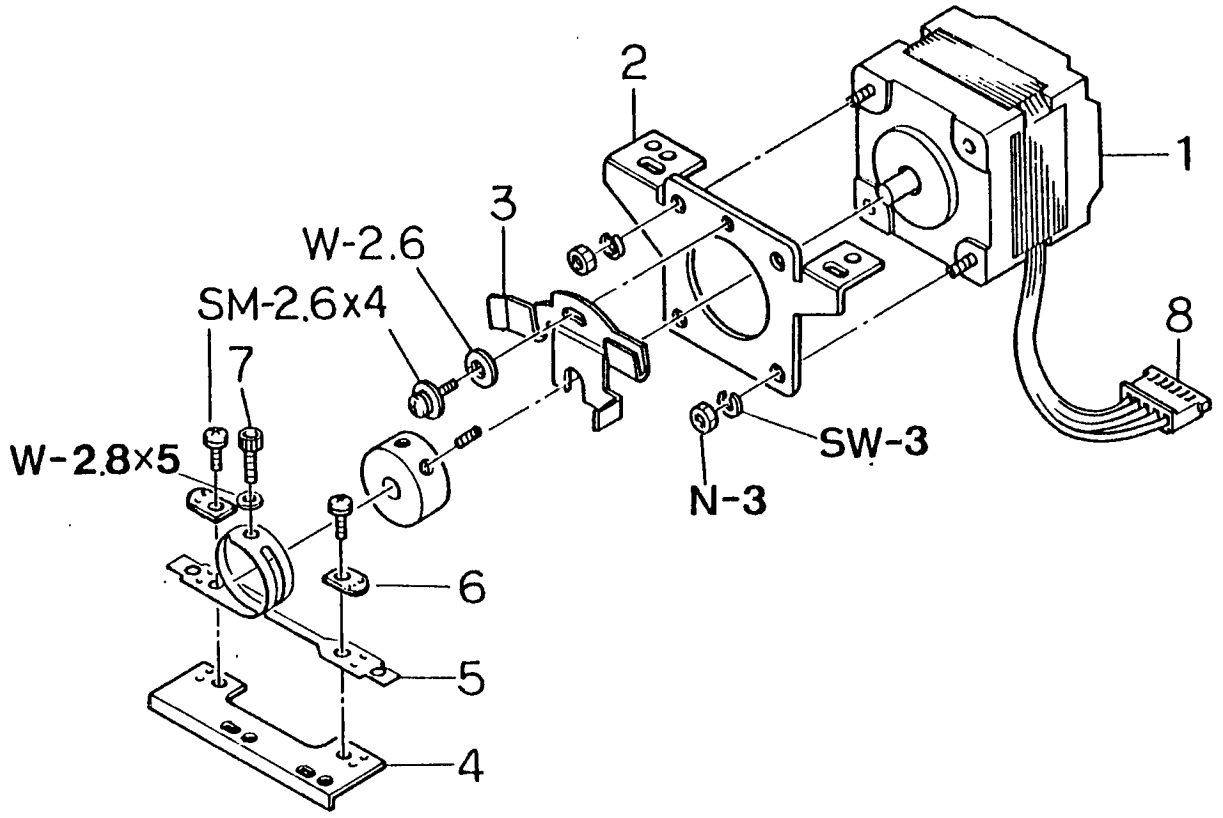
3 CARRIER A BK (FB-501, -502)

Ref. No.	Part No.	Part Name	Remarks	
3-1	CFAAK-60401	Carrier A-K	501	
	CFAAK-60402	Carrier A-K	502	
3-2	CFAAK-02101	Pad K	501, 502	
3-3	CFA10-00201	Load Arm Shaft	501, 502	
3-4	CFA30-00201	Load Arm Spring	501, 502	
3-5	CFA35-02801	Load Arm III	501, 502	
3-6	CFEAK-02201	Head Cable AK	501, 502	
3-7	CFA45-61901	Shield Plate A		


4
5
6
7
3
2
1

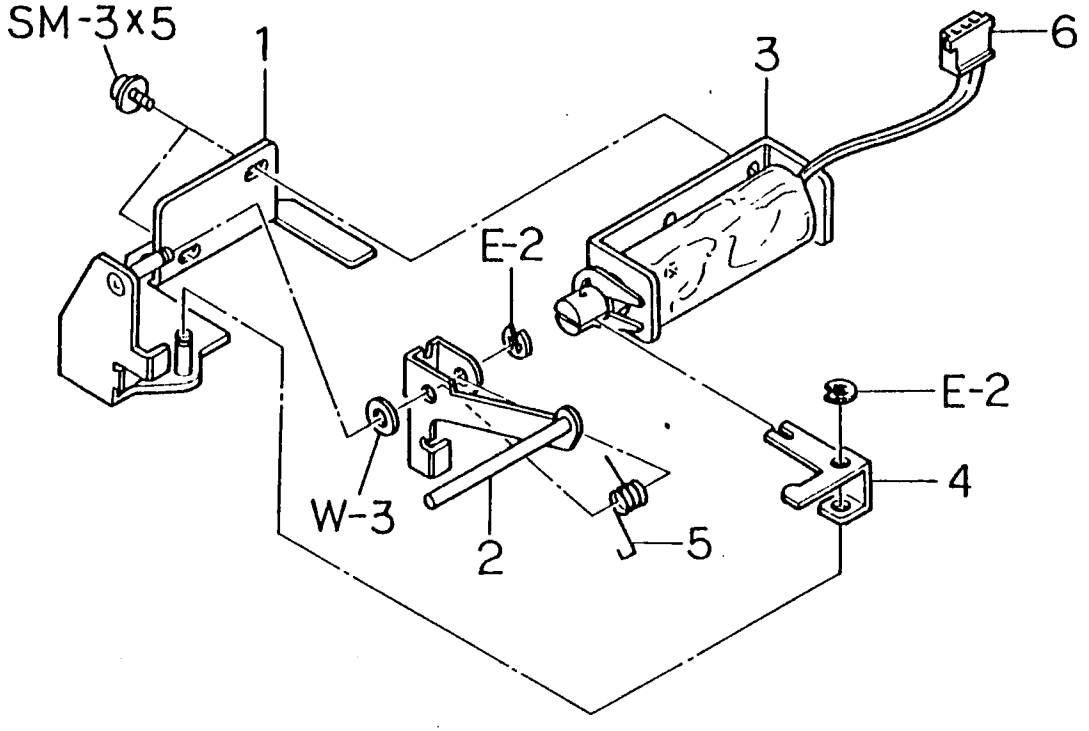
4 CARRIER B BK (FB-503, -504)

Ref. No.	Part No.	Part Name	Remarks	
4-1	CFAAK-60501	Carrier B-K	503	
	CFAAK-60502	Carrier B-K	504	
4-2	CFAAK-60601	Head Arm K	503	
	CFAAK-60602	Head Arm K	504	
4-3	CFA30-60201	Head Pressure Control Spring	503, 504	
4-4	CFA45-61001	Bolt	503, 504	
4-5	CFA20-61701	Head Arm Support	503, 504	
4-6	CFEAK-02201	Head Cable AK	503, 504	
4-7	CFA45-61701	Shield Plate B-L		


2
1
3
W-2.6
SM-2.6x4
8
7
W-2.8x5
SW-3
N-3
6
5
4

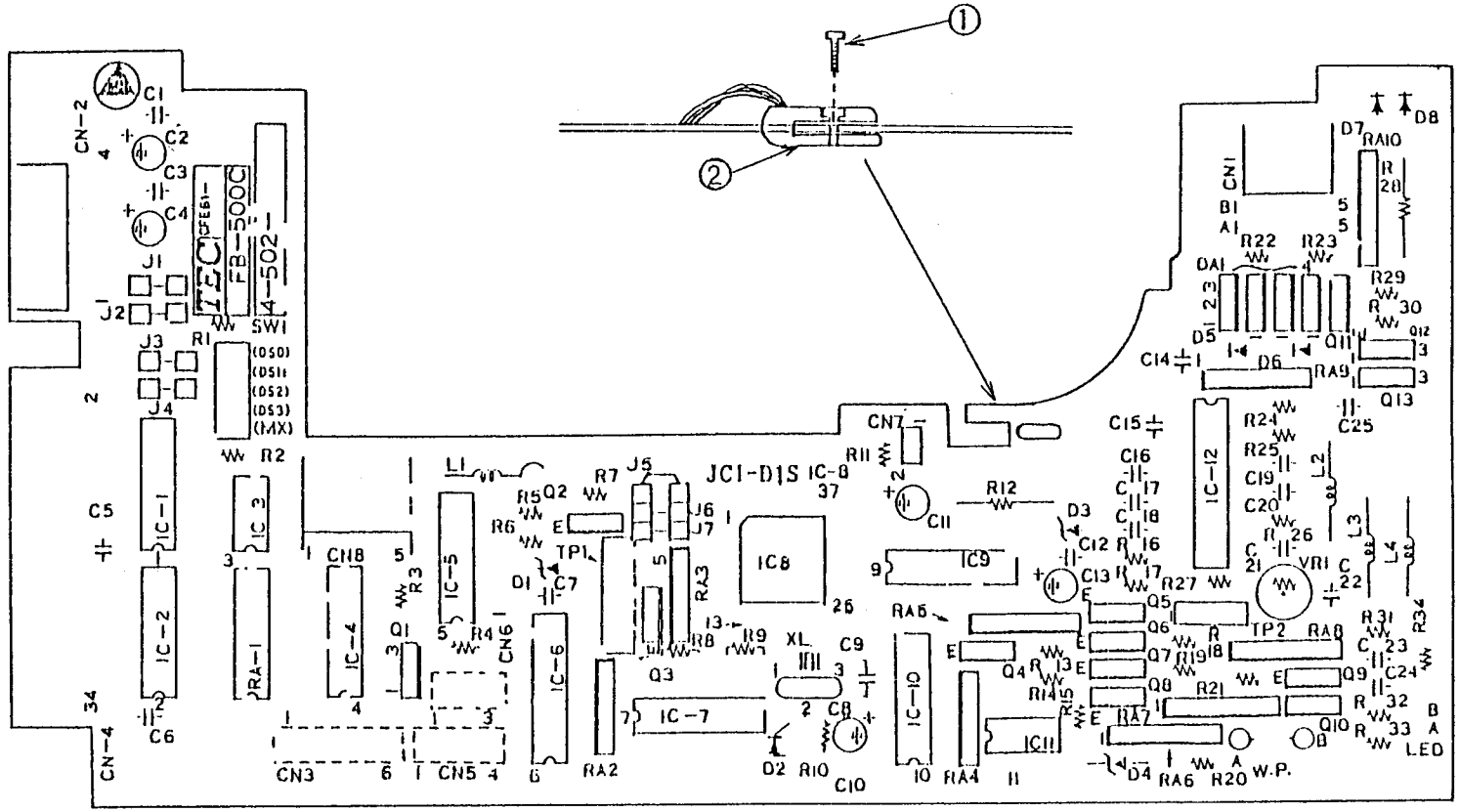
5 PLUSE MOTOR BK

Ref. No.	Part No.	Part Name	Remarks	
5- 1	CFAAK-60701	Pulse Motor K	502ST, 504ST, 504HL	
	CFAAK-60702	Pulse Motor K	501ST, 503ST, 503HL	
5- 2	CFA20-62501	ST Motor Frame		
5- 3	CFA20-61901	TR 00 Stopper		
5- 4	CFA20-61001	Belt Supporter		
5- 5	CFA45-60701	Belt		
5- 6	CFA20-60501	Belt Fastening Plate		
5- 7	CFA45-61001	Bolt		
5- 8	EEA00-87400	Connector 6-Pin Female		


SM-3x5
1
3
6
E-2
E-2
4
W-3
2
5

6 HEAD LOAD BK (OPTION FB-503, -504)

Ref. No.	Part No.	Part Name	Remarks	
6-1	CFAAK-60901	Head Load Base K	503, 504	
6-2	CFAAK-61001	Load Arm A-K	503, 504	
6-3	CFAAK-61101	Head Load Solenoid K	503, 504	
6-4	CFA20-61501	Load Arm B	503, 504	
6-5	CFA30-60401	Head Load Spring	503, 504	
6-6	EEA00-87100	Connector 3-Pin Female	503, 504	


①
②
FB-500C
FB-502
SW1
(DS0)
(DS1)
(DS2)
(DS3)
(MX)
JCI-D1S
IC-8
37
IC-1
IC-2
IC-3
IC-4
IC-5
IC-6
IC-7
IC8
IC9
IC-10
IC11
IC-12
CN1
CN2
CN3
CN4
CN5
CN6
CN7
CN8
RA1
RA2
RA3
RA4
RA5
RA6
RA7
RA8
RA9
RA10
XL
TP1
TP2
VR1
LED
W.P.

Ref. No.	Part No.	Part Name		Remarks	
RA3,4	EAC00-09300	Diode Array	DAN201		
LED	EAH00-06200	LED LN25CP			
CN-4	CFA45-60301	Sensor ID			
W.P.	CFA45-60401	Sensor W			
R1	ECC1GT151JB	Carbon Resistor	R20 150Ω J		
R2,4	ECC1GT102JB	Carbon Resistor	R20 1KΩJ		
R3	ECC1GT181JB	Carbon Resistor	R20 1KΩJ		
R5,R13	ECC1GT471JB	Carbon Resistor	R20 470Ω J		
R6,8	ECC1BT472JB	Carbon Resistor	R20 4.7KΩJ		
R7,15,27,30	ECC1GT103JB	Carbon Resistor	R20 10KΩJ		
R9	ECC1GT242JB	Carbon Resistor	R20 2.4KΩJ		
R10	ECC1GT473JB	Carbon Resistor	R20 47KΩJ		
R11,20	ECC1GT393JB	Carbon Resistor	R20 39KΩJ		
R12	ECI01H151JA	Metal-Oxide Resistor	RS1BJ150Ω F		
R14	ECC1GT751JB	Carbon Resistor	R20-750ΩJ	504	
R16,17,22	ECC1GT562JB	Carbon Resistor	R20 5.6KΩJ		
R0,18,19	ECC1GTP22JB	Carbon Resistor	R20 2.2KΩJ		
R21,29	ECC1GT821JB	Carbon Resistor	R20 820ΩJ		
R23	ECC1GT562JB	Carbon Resistor	R20 5.6KΩJ	503,504,	
R24,25	ECC1GT271JB	Carbon Resistor	R20 270Ω J		
R26	ECC1GT820JB	Carbon Resistor	R20 82Ω J		

Ref. No.	Part No.	Part Name		Remarks	
R28	ECI1AH470JA	Metal-Oxide Resistor	RS1/2BJ 47Ω F	501,503	
R28	ECI1AH101JA	Metal-Oxide Resistor	RS1/2BJ 100Ω F	502,504	
R31	ECC1GT561JB	Carbon Resistor	R20 560Ω J	501,502,503	
R32,33	ECC1GT104JR	Carbon Resistor	R20 100KΩ J		
R34	ECC1GT221JB	Carbon Resistor	R20 220Ω J		
J2	ECC1GT000JR	Carbon Resistor	R20 0Ω J	503,504	
R16,17	ECC1GT562JB	Carbon Resistor	R20 5.6KΩ J		
RA2,3	ECM00-00300	Resistor Array	EXB-P84472K		
RA4	ECM00-00100	Resistor Array	EXB-P83102K		
RA5	ECM00-18200	Resistor Array	RM0493		
RA6	FCM00-17900	Resistor Array	RM0490		
RA7	ECM00-18100	Resistor Array	RM0492		
RA8	ECM00-18300	Resistor Array	RM0495		
RA9	ECM00-18000	Resistor Array	RM0491		
RA10	ECM00-18400	Resistor Array	RM0496		
VR1	ECA00-13400	Variable Resistor	TM64K2(PV)203K		
C1,12,19,20,23,24	EBJT0-05200	Ceramic Capacitor	DD600-959 13C104 350V		
C2	EBB00-34900	Electrolytic Capacitor	ECEADJK101		
C3,7,15,16	EBIT0-00900	Laminated Capacitor	ZPE122F104Z50V		
C4,10,11	EBB00-34800	Electrolytic Capacitor	ECEA1CJ470		
C5,21	EBJT0-07100	Ceramic Capacitor	DD104-959B102K50V		
C6,9,26	EBJT0-05600	Ceramic Capacitor	CC107-959F103Z50V		

Ref. No.	Part No.	Part Name		Remarks	
C13	EBB00-53800	Electrolytic Capacitor	ECEA1CK-100		
C14	EBJT0-03100	Ceramic Capacitor	DD105-959SL121J50V	502,504	
C14	EBJ00-03500	Ceramic Capacitor	DD106-63SL181J50V	501,503	
C17	EBJ00-11500	Ceramic Capacitor	DD109-63SL561J50V		
C18	FBJ00-13900	Ceramic Capacitor	DD107-63SL301J50V		
C22,25	EBJ00-11400	Ceramic Capacitor	DD109-63SL511J50V		
Addition	EBJ00-00800	Ceramic Capacitor	DD104-63SL100D50V	Between Pin14 and 15 of IC12	
XL,C8	EKH00-04600	Cerarock Capacitor	KMFC1001S		
L1	EDD00-06700	Choke Coil	ELEBD470KA		
L2	EDD00-06600	Choke Coil	ELEBD150KA		
L3,4	EDD00-06800	Choke Coil	ELEBD331KA		
RA1	EED00-05600	IC Socket	DILB14P-8J		
CN1	EEA00-63600	Connector 5P Plug	65532-44P	501,502	
CN1	EEB00-45700	Connector 10P Plug	655625-410	503,504	
CN2	EEB00-45900	Connector 4P Plug	172P94-1		
CN3	EEB00-50600	Connector 6P Plug	67094-006		
CN5	EEB00-50500	Connector 4P Plug	67094-004		
CN6	EEB00-50400	Connector 3P Plug	67094-003	503	
CN8	EEB00-50700	Connector 55 Plug	67095-005		
TP1	EEB00-51300	Connector 5P Plug	W-P5005#01		
TP2	EEB00-51200	Connector 4P Plug	W-P5004#01		

Ref. No.	Part No.	Part Name	Remarks	
CN-2	EEE00-01400	Connector Retainer 172296-1		
SW1	EEF00-20800	Short Pin FFC-(10)FMEP2		
DSO	EEF00-20900	Short Pin Jack DIC-S252		
1	CFA45-61002	Hexagonal Socket Head Screw		
	RPM45-10701	Seal C		
2	CFA45-60301	Sensor ID		

CHAPTER 7 RECOMMENDED SPARE PARTS LIST

(FB-500 Series)

FB-500 Series RECOMMENDED SPARE PARTS LIST

No.	Ref. No.	Part No.	Part Name	Remarks	Quantity	Quantity/ 1000 units
1	1-2	CFABK-60201	Carrier A BK		1	5
		CFABK-60202	Carrier A BK		1	5
		CFABK-60301	Carrier B BK		1	5
		CFABK-60302	Carrier B BK		1	5
2	1-5	CFAAK-60301	DD Motor K		1	5
3	1-7	CFAAK-61201	Interrupter AK		1	5
4	1-8	CFEAK-05701	Drive AK	501	1	10
		CFEAK-05702	Drive AK	502	1	10
		CFEAK-05703	Drive AK	503	1	10
		CFEAK-05704	Drive AK	504	1	10
5	2-1	CFABK-60601	Clamp BK		1	5
6	5-1	CFAAK-60701	Pulse Motor K	502, 504	1	5
		CFAAK-60702	Pulse Motor K	501, 503	1	5
7	5-5	CFA45-60701	Belt			